Analysis and Design of Analog Integrated Circuits
Lecture 22

Digital to Analog Conversion

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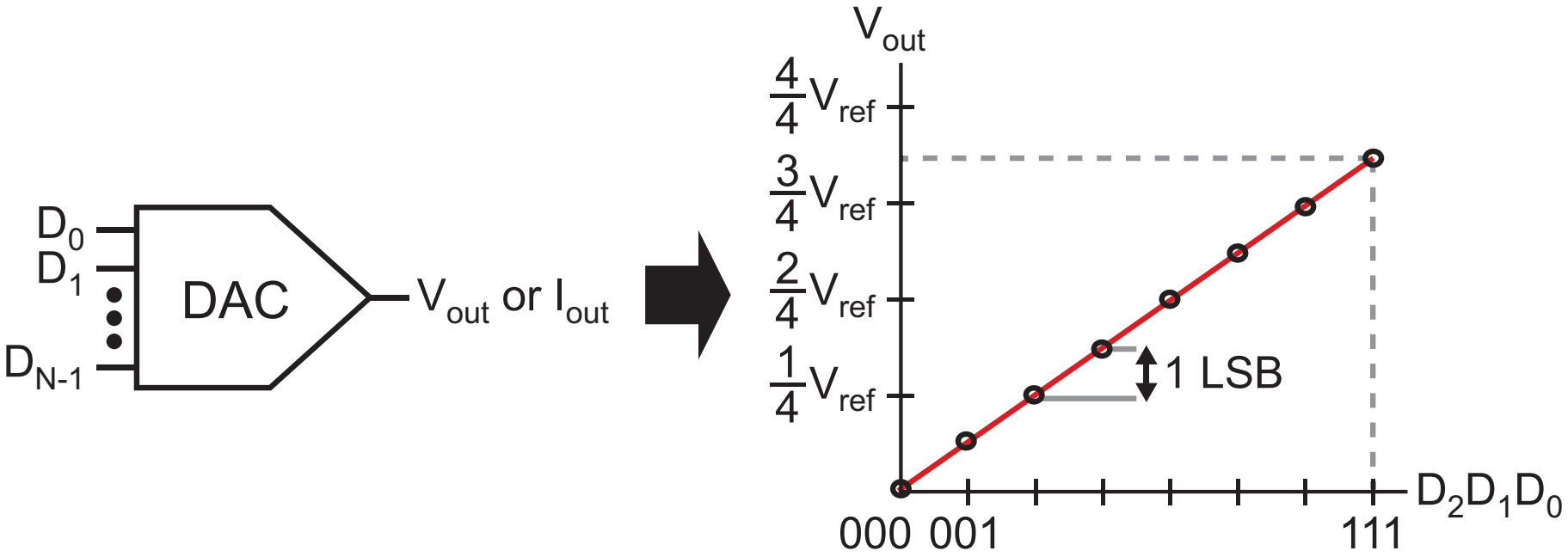
Outline of Lecture

- **Basic DAC Specifications**
- **Types of DACs (Resistive, Current, Capacitive)**
- **Impact of dynamic operation (NRZ, RZ)**
- **Sigma-Delta operation for high resolution**

Digital to Analog Conversion

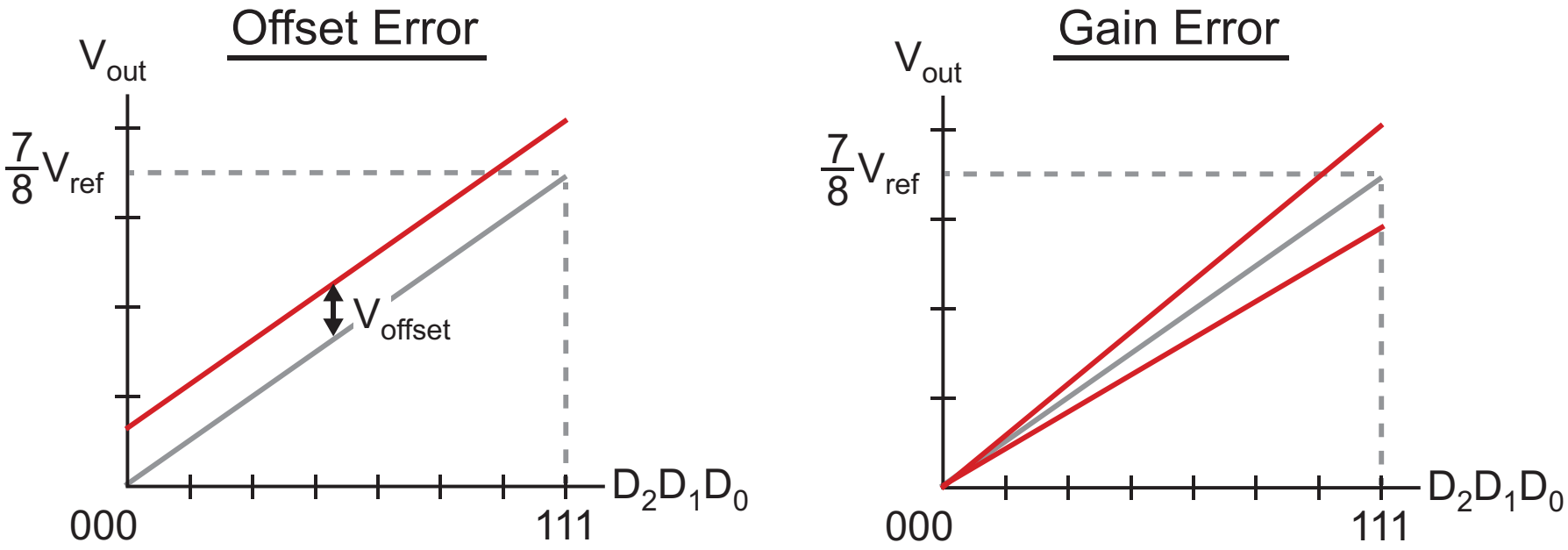


- **Digital input consists of bits, D_k, with values 0 or 1**
- **Analog output is either voltage or current**

$$V_{out} = \frac{V_{ref}}{2^N}(2^{N-1}D_{N-1} + 2^{N-2}D_{N-2} + \cdots 2^1 D_1 + 2^0 D_0)$$

- **Key characteristics**
  - **Full scale = V_{ref}**
  - **Resolution = $V_{ref}/2^N$ = 1 LSB**

Gain and Offset Errors

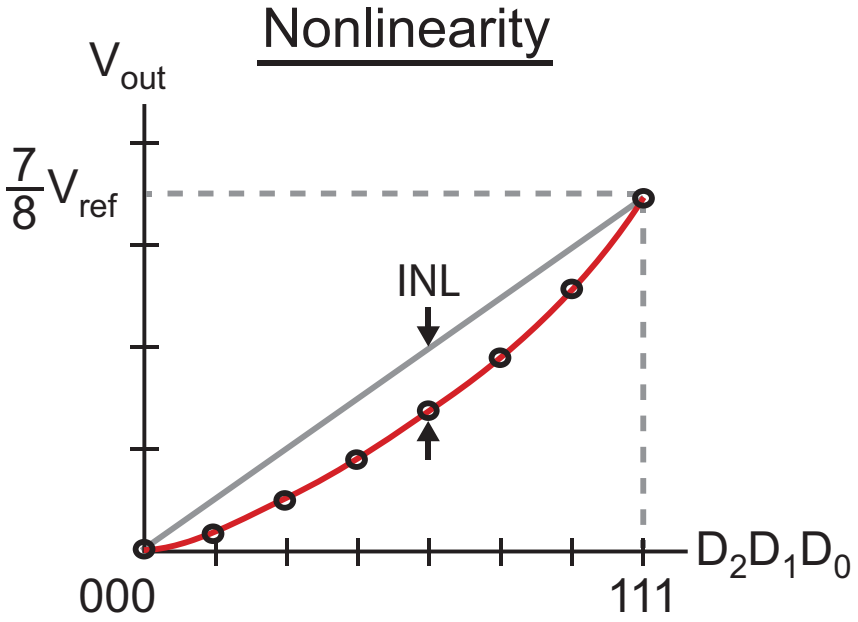


- **Offset is most easily characterized as**

$$V_{offset} = V_{out}|_{D_k=0}$$

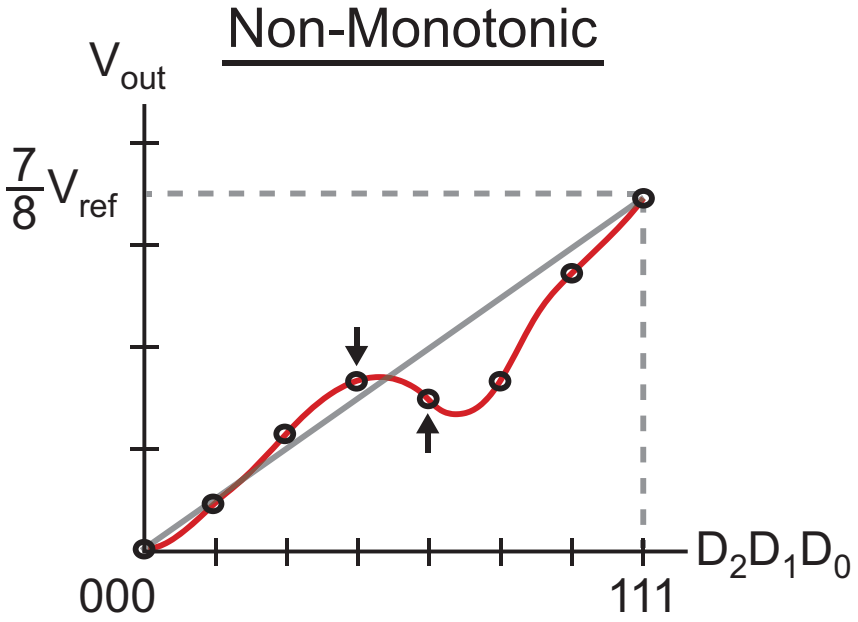
- **Gain error is characterized either as**
  - **Error at full scale (in LSBs)**
  - **Percentage of full scale**

Nonlinearity



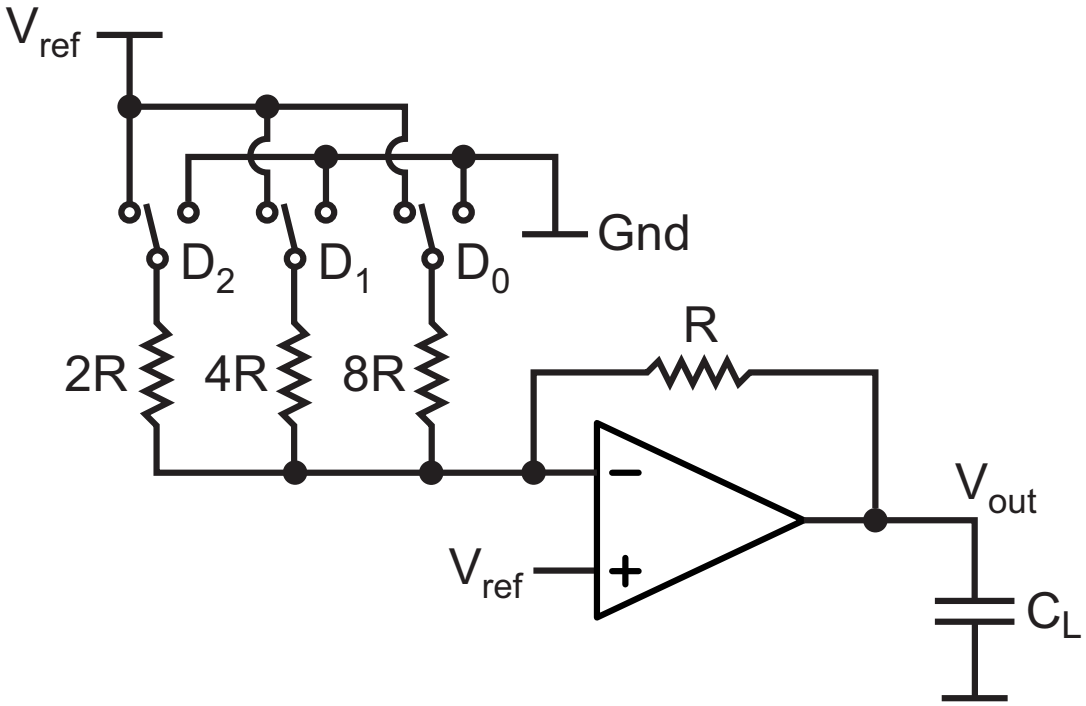
- **Integral Non-Linearity (INL)**
  - **Maximum deviation from the "ideal line" characterisitic**
    - Typically specified in units of LSBs
- **Differential Non-Linearity (DNL)**
  - **Maximum deviation of all codes from their ideal step size of 1 LSB**

Monotonicity



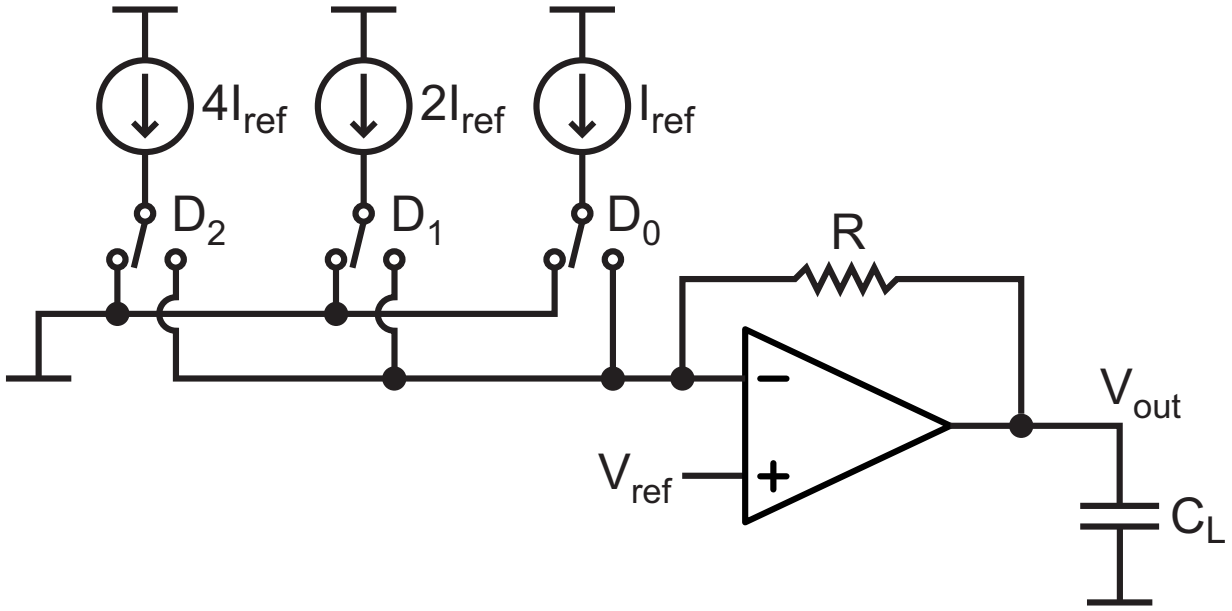
- **Monotonic behavior requires that stepping any code to the next code yields a step in the output that is always the same sign**
  - **Important in systems which utilize the D/A converter as part of a feedback**
    - Non-monotonicity yields changes in the sign of the gain, which can lead to small signal stability problems

Binary Resistor DAC



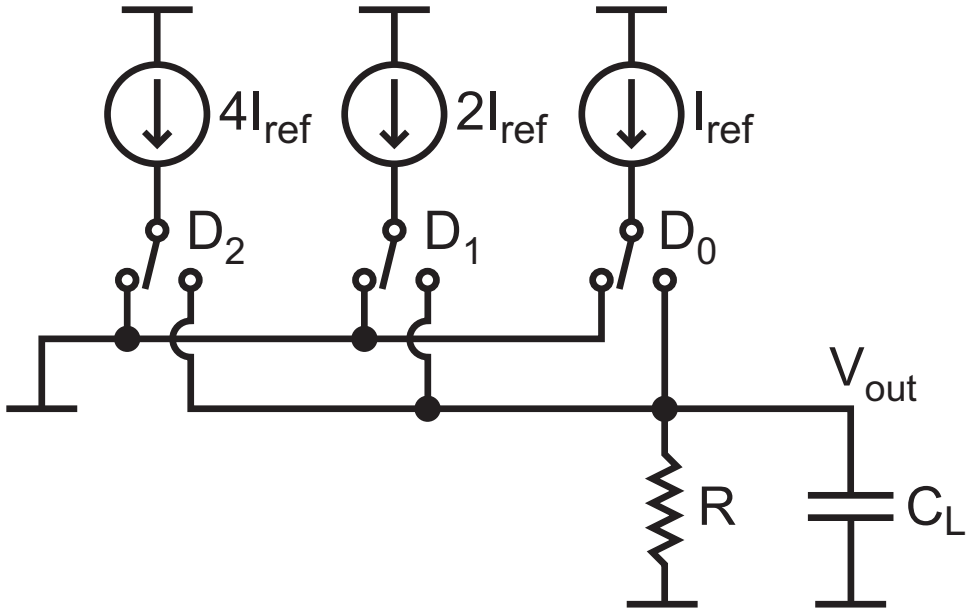
- **Relies on accurate resistor ratios for good INL/DNL**
- **Issues**
  - **Switches contribute resistance**
    - Can impact accuracy without clever design measures
  - **Resistors require significant area for a high resolution DAC**

Binary Current DAC



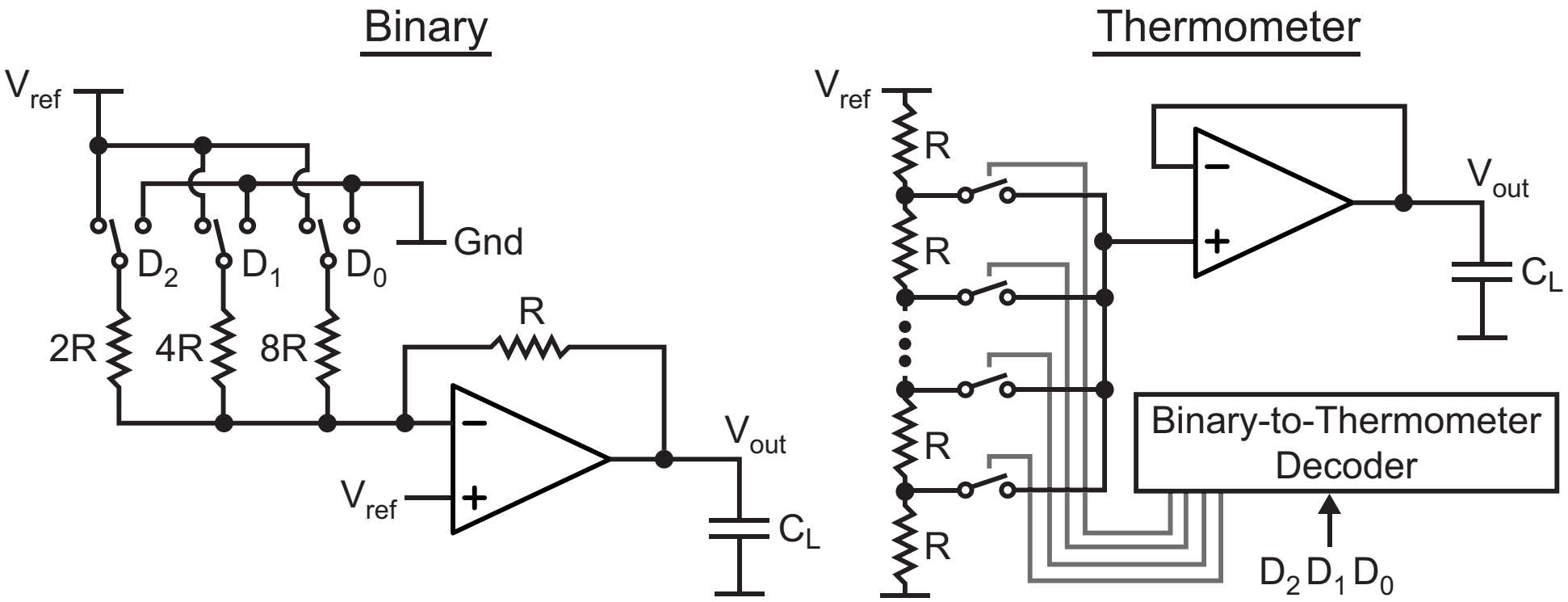
- Advantages
  - Switch resistance does not impact accuracy (to first order)
  - Scaled current sources are readily obtained using current mirror techniques
- Issues
  - Likely to have higher 1/f noise than resistor based DAC
  - Opamp limits bandwidth, adds noise

Binary Current DAC with Resistive Load



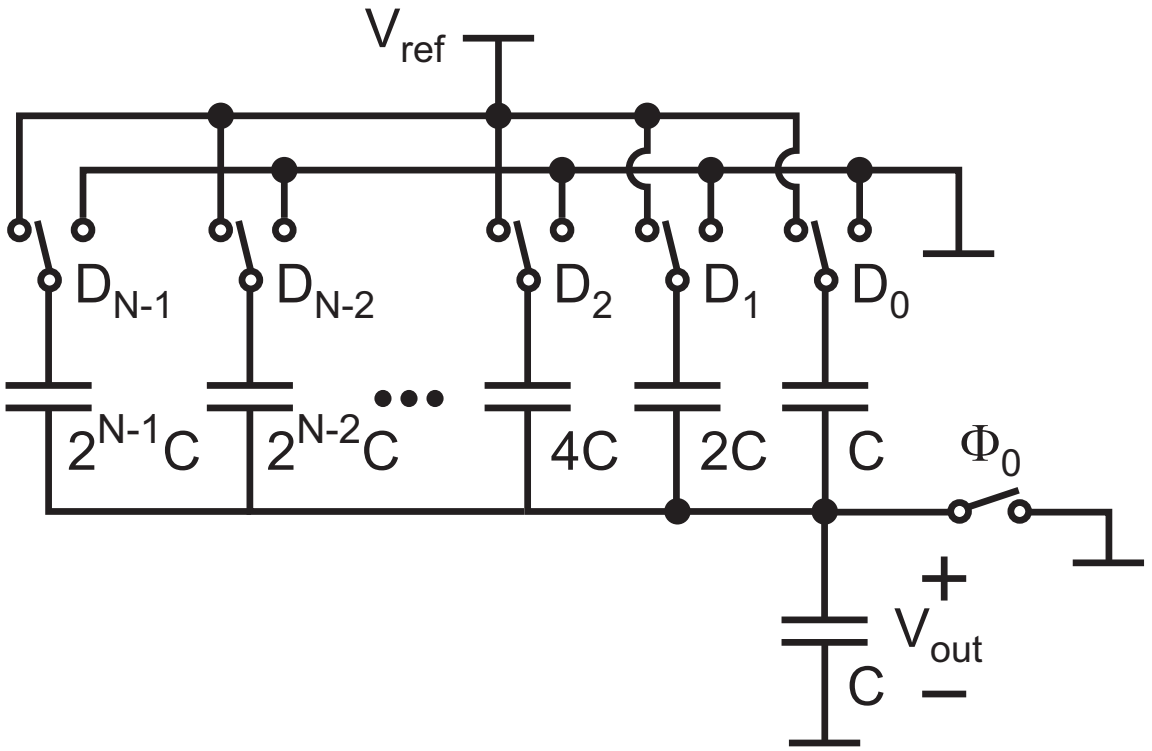
- **No opamp required**
  - **Useful for high speed applications**
- **Issues**
  - **Current sources must now bear the full output range**
    - Much harder to maintain constant current from them
      - Cascoding takes up headroom
    - Can lead to code dependent nonlinearity (i.e., poor INL, distortion)

Binary Versus Thermometer Encoding



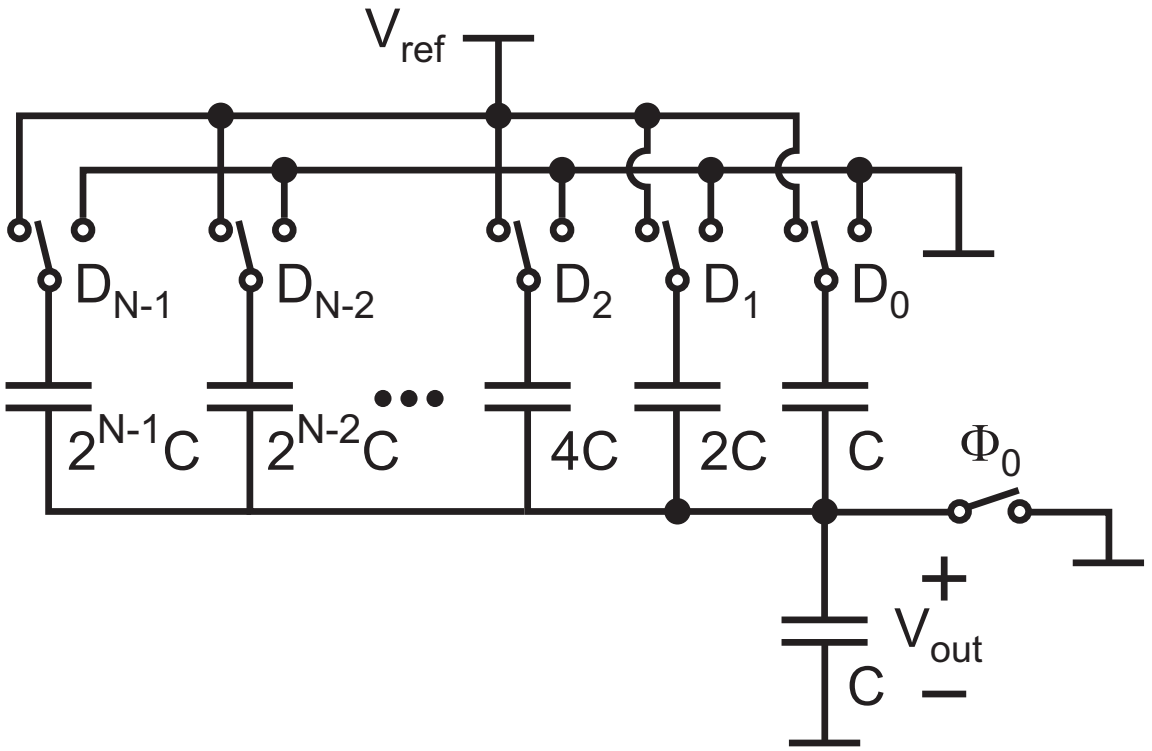
- **Thermometer encoded resistor ladder provides inherently monotonic behavior**
- **Issues for high resolution**
  - **Decoding becomes very complex**
  - **Area can be quite large**

Capacitor DAC



- **Uses charge re-distribution on a capacitor network to realize output voltages**
  - **Key advantage is that capacitor matching is quite good in CMOS processes**
  - **Has become the preferred approach for low to modest speed discrete-time ADCs**

Operational Details of Capacitor DAC

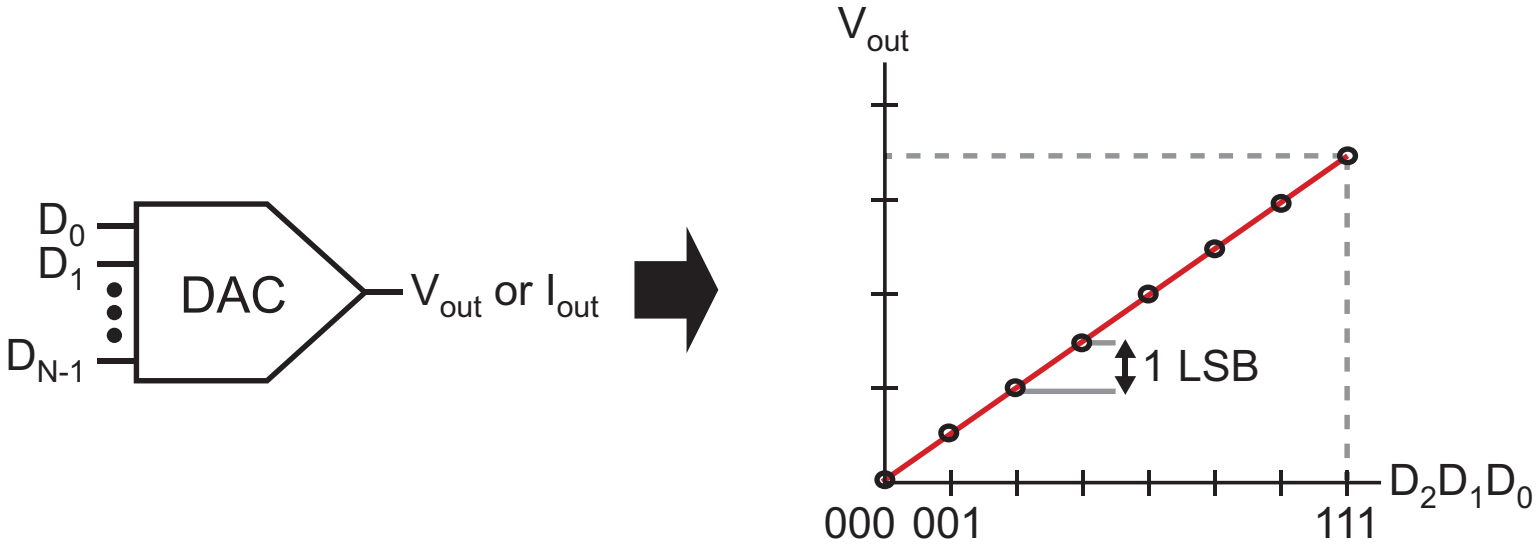


- First discharge all capacitors to zero ($D_k = 0$, $\Phi_0 = 1$)
- Set $P_0 = 0$ and then set D_k values

$$V_{out} = \frac{V_{ref}}{2^N C}\left(D_{N-1}2^{N-1}C + D_{N-2}2^{N-2}C^{N-2} + \cdots + D_1 2C + D_0 C\right)$$

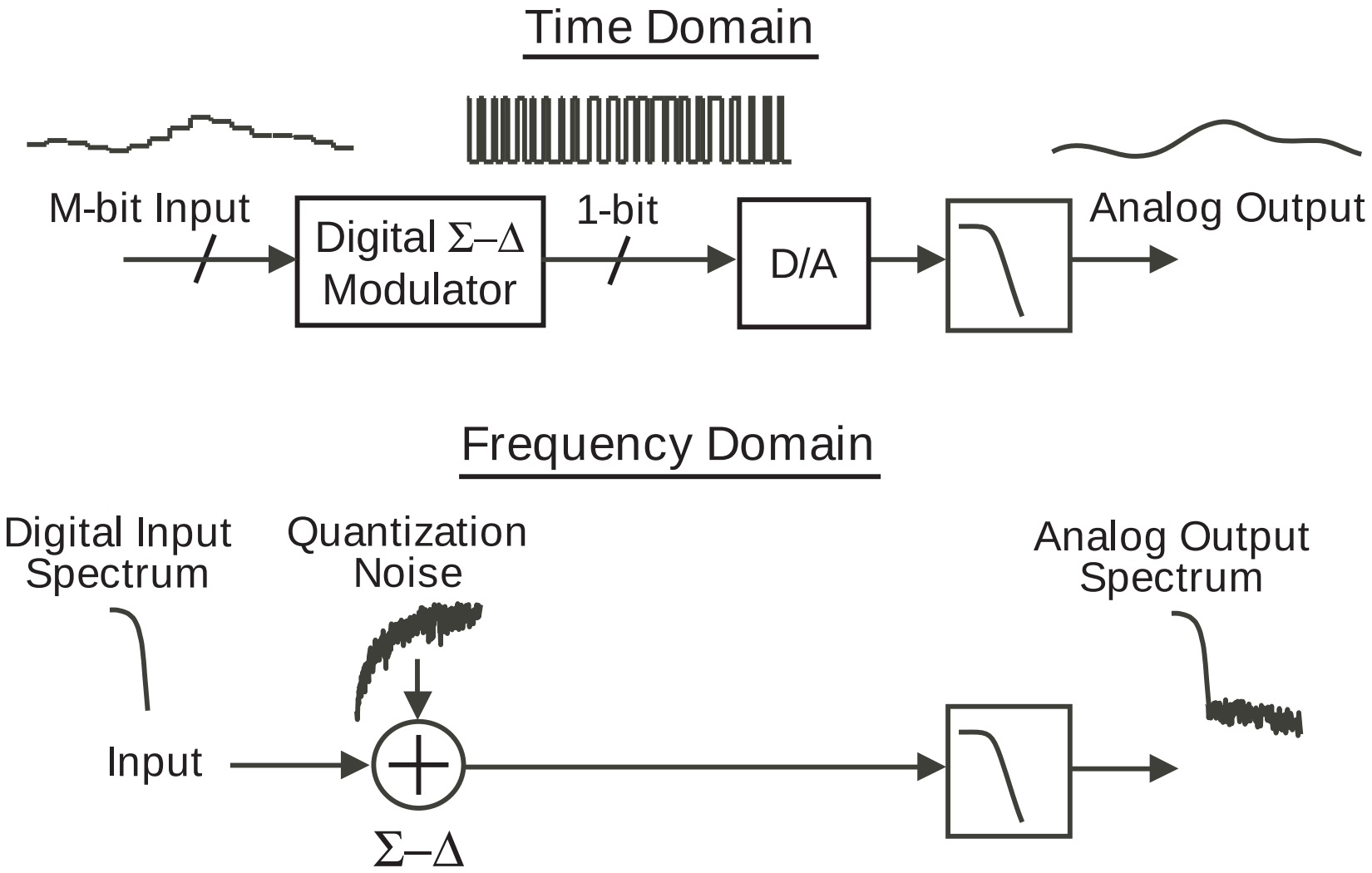
$$\Rightarrow \quad V_{out} = \frac{V_{ref}}{2^N}\left(D_{N-1}2^{N-1} + D_{N-2}2^{N-2} + \cdots + D_1 2 + D_0\right)$$

Seeking Higher Resolution



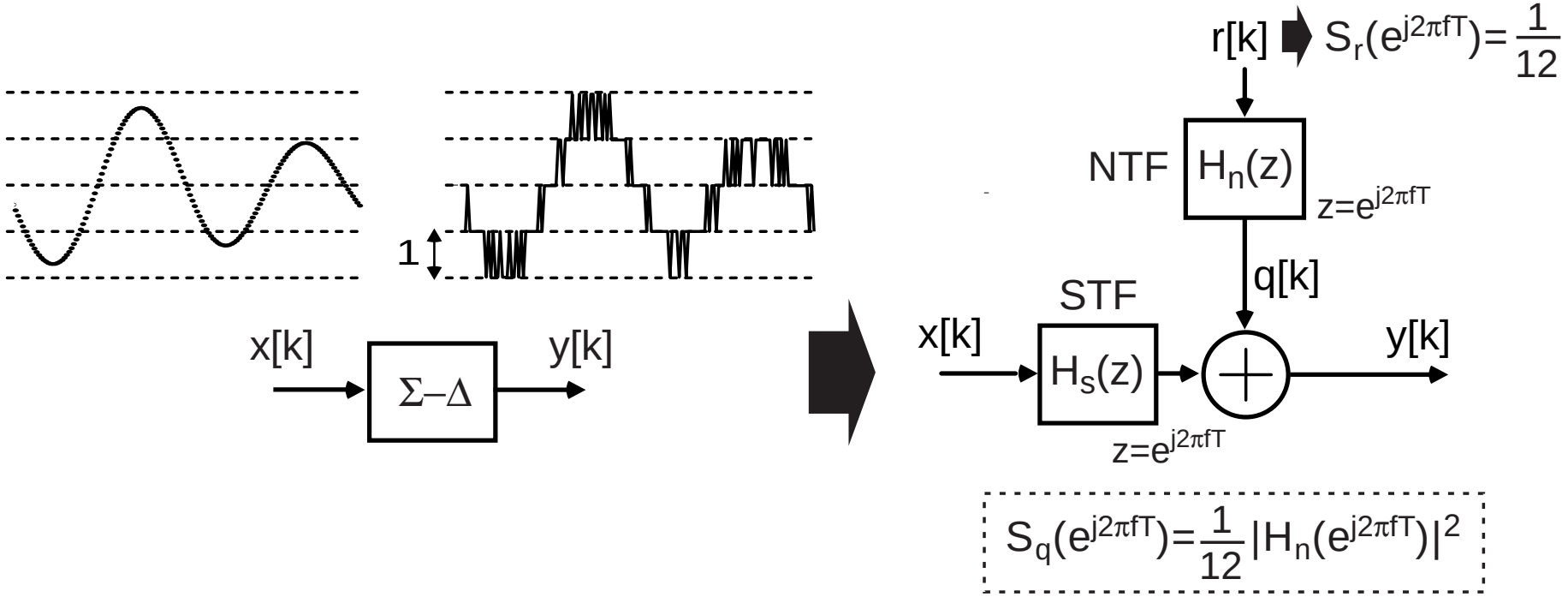
- Increasing the number of levels in the DAC achieves higher resolution at the cost of complexity and power
  - At some point, improved resolution becomes impractical with this approach
- An alternative approach is to consider dithering between levels of a coarse DAC
  - By averaging the output, we can obtain resolution finer than the LSB of the coarse DAC

Sigma-Delta Modulation



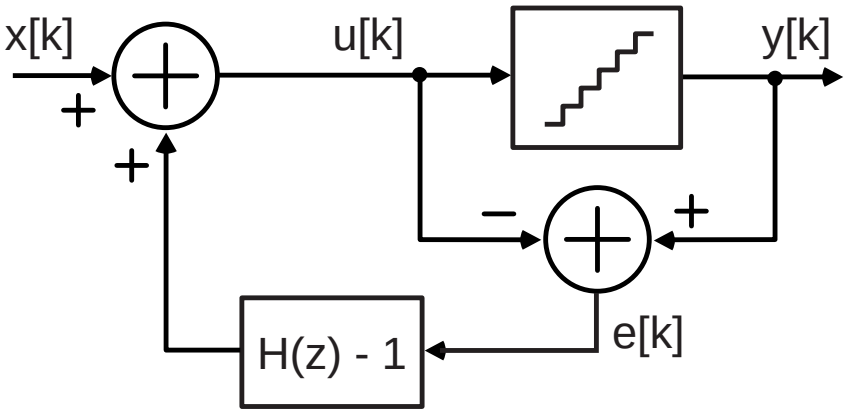
- **Sigma-Delta dithers in a manner such that resulting quantization noise is "shaped" to high frequencies**

Linearized Model of Sigma-Delta Modulator



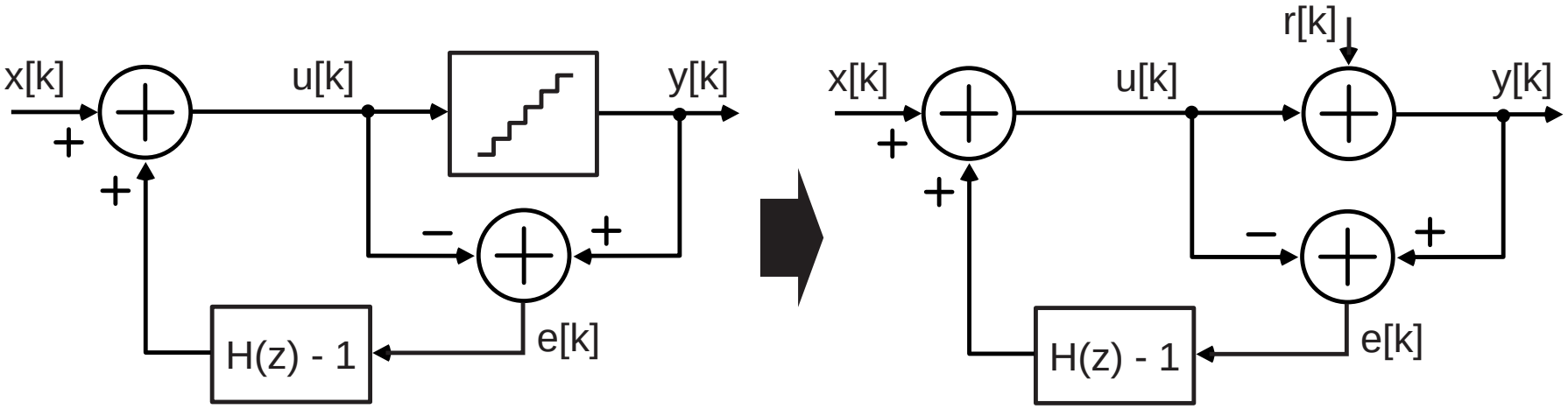
- **Composed of two transfer functions relating input and noise to output**
  - **Signal transfer function (STF)**
    - Filters input (generally undesirable)
  - **Noise transfer function (NTF)**
    - Filters (i.e., shapes) noise that is assumed to be white

Example: Cutler Sigma-Delta Topology



- **Output is quantized in a multi-level fashion**
- **Error signal, e[k], represents the quantization error**
- **Filtered version of quantization error is fed back to input**
  - **H(z) is typically a highpass filter whose first tap value is 1**
    - i.e., $H(z) = 1 + a_1 z^{-1} + a_2 z^{-2} \cdots$
  - **H(z) – 1 therefore has a first tap value of 0**
    - Feedback needs to have delay to be realizable

Linearized Model of Cutler Topology

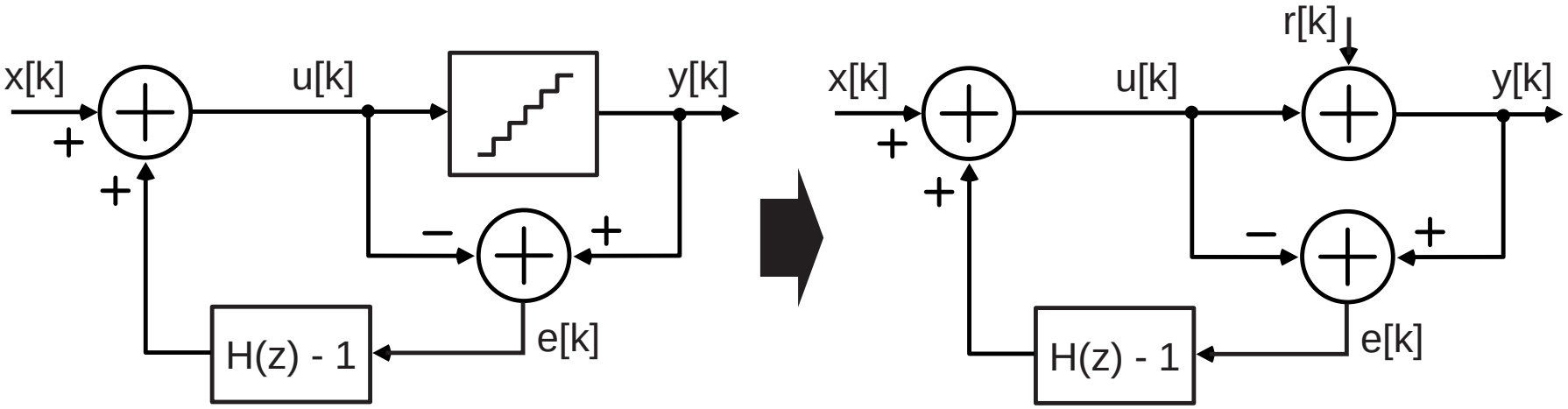


- **Represent quantizer block as a summing junction in which r[k] represents quantization error**
  - **Note:**

$$e[k] = y[k] - u[k] = (u[k] + r[k]) - u[k] = r[k]$$

- **It is assumed that r[k] has statistics similar to white noise**
  - **This is a key assumption for modeling – often not true!**

Calculation of Signal and Noise Transfer Functions



- **Calculate using Z-transform of signals in linearized model**

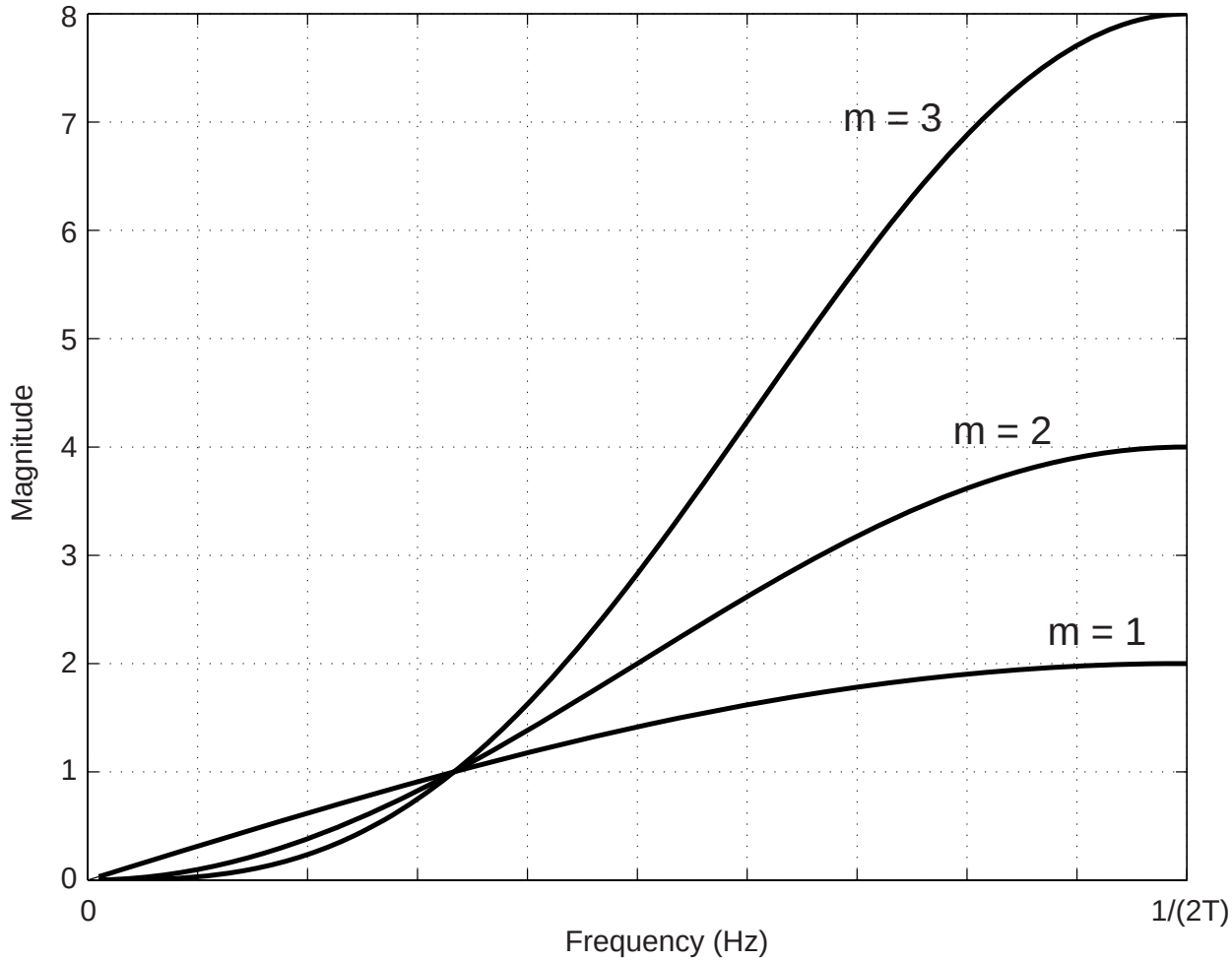
$$\begin{aligned} Y(z) &= U(z) + R(z) \\ &= X(z) + (H(z) - 1)E(z) + R(z) \\ &= X(z) + (H(z) - 1)R(z) + R(z) \\ &= X(z) + H(z)R(z) \end{aligned}$$

  - **NTF: $H_n(z) = H(z)$**
  - **STF: $H_s(z) = 1$**

A Common Choice for H(z)

$$H(z) = (1 - z^{-1})^m$$

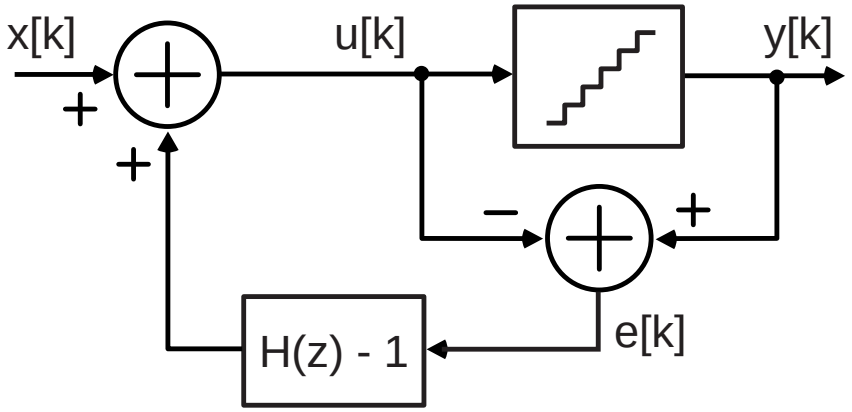
$$\Rightarrow \; |H(e^{j2\pi fT})| = |(1 - e^{-j2\pi fT})^m|$$



Example: First Order Sigma-Delta Modulator

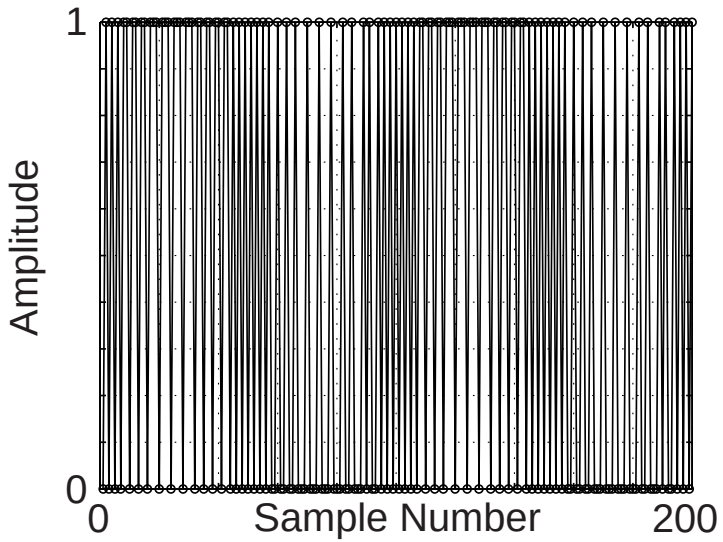
- **Choose NTF to be**

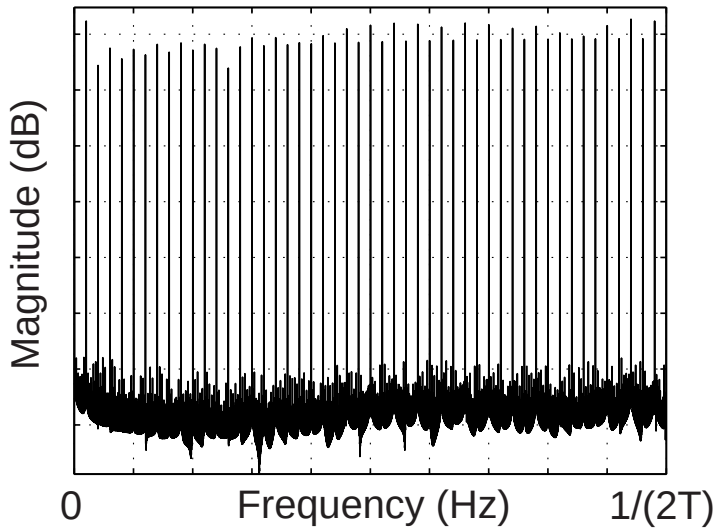
$$H_n(z) = H(z) = 1 - z^{-1}$$



- **Plot of output in time and frequency domains with input of**

$$x[k] = 0.5 + 0.25 \sin\left(\frac{2\pi}{100}k\right)$$

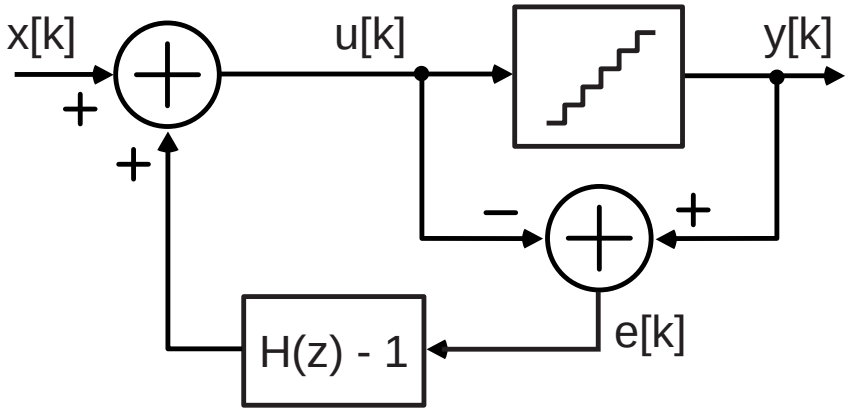




Example: Second Order Sigma-Delta Modulator

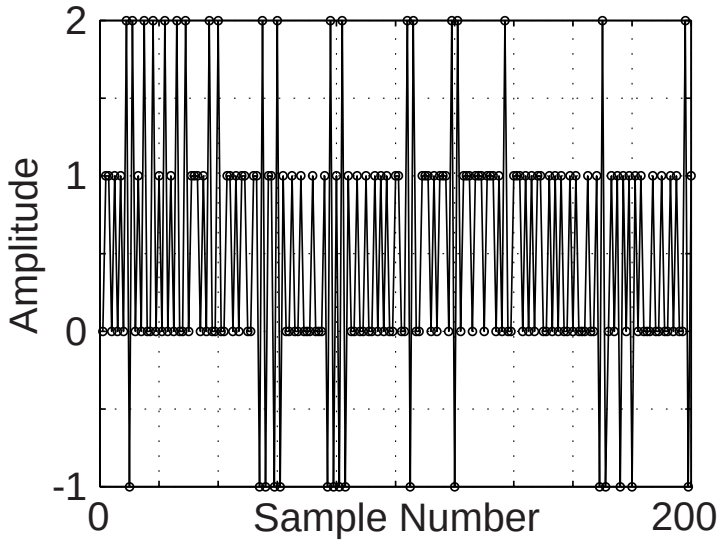
- **Choose NTF to be**

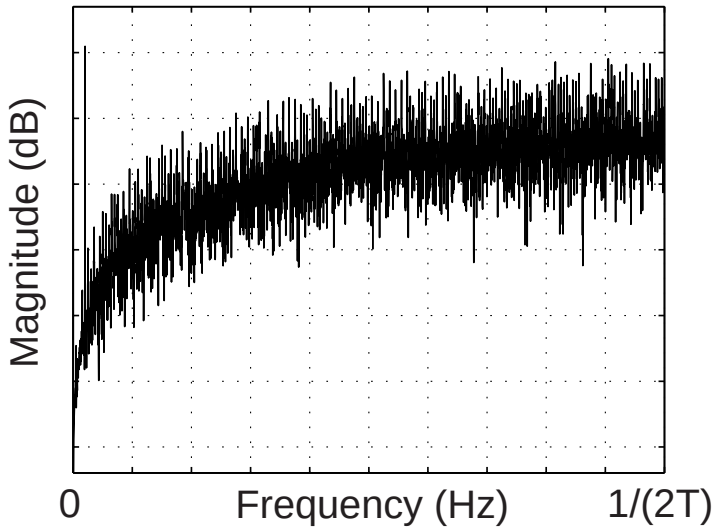
$$H_n(z) = H(z) = (1 - z^{-1})^2$$



- **Plot of output in time and frequency domains with input of**

$$x[k] = 0.5 + 0.25 \sin\left(\frac{2\pi}{100}k\right)$$

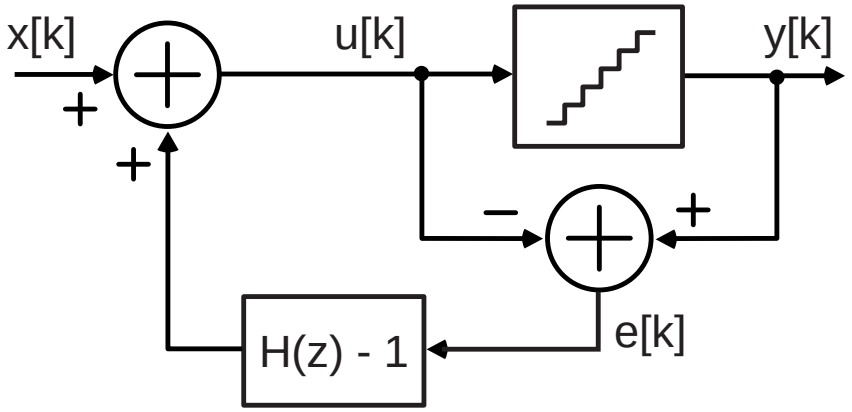




Example: Third Order Sigma-Delta Modulator

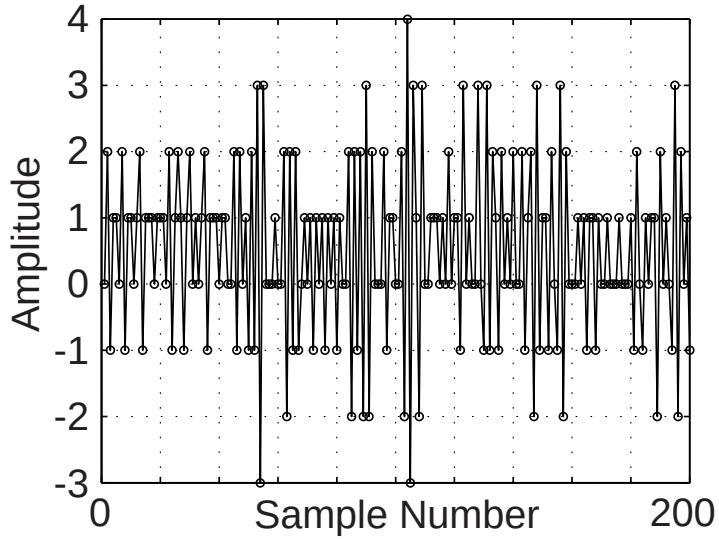
- **Choose NTF to be**

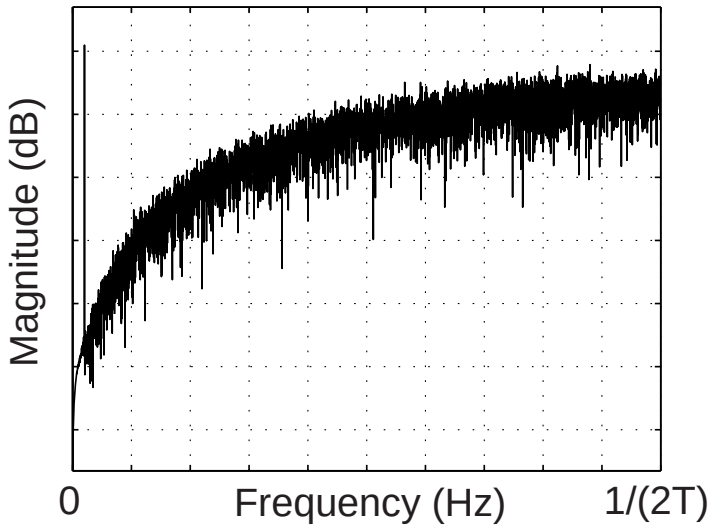
$$H_n(z) = H(z) = (1 - z^{-1})^3$$



- **Plot of output in time and frequency domains with input of**

$$x[k] = 0.5 + 0.25 \sin\left(\frac{2\pi}{100}k\right)$$



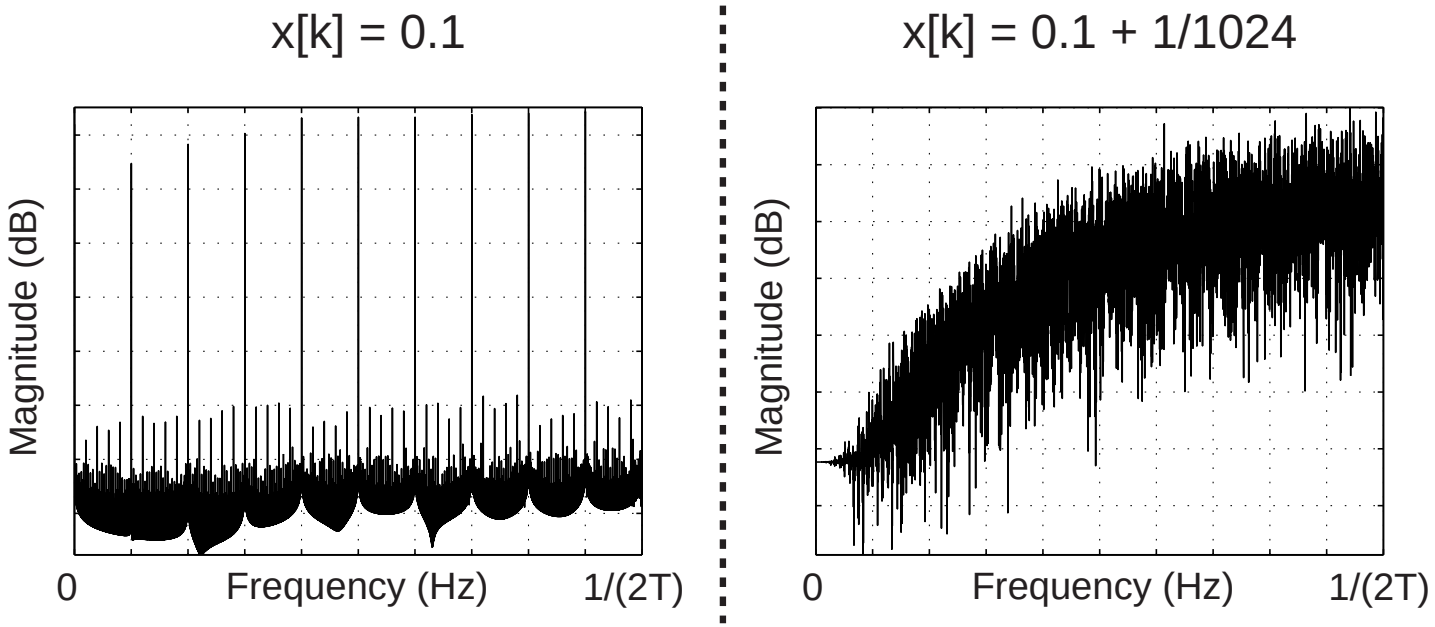


Observations

- **Low order Sigma-Delta modulators do not appear to produce “shaped” noise very well**
  - **Reason: low order feedback does not properly “scramble” relationship between input and quantization noise**
    - Quantization noise, r[k], fails to be white
- **Higher order Sigma-Delta modulators provide much better noise shaping with fewer spurs**
  - **Reason: higher order feedback filter provides a much more complex interaction between input and quantization noise**

Warning: Higher Order Modulators May Still Have Tones

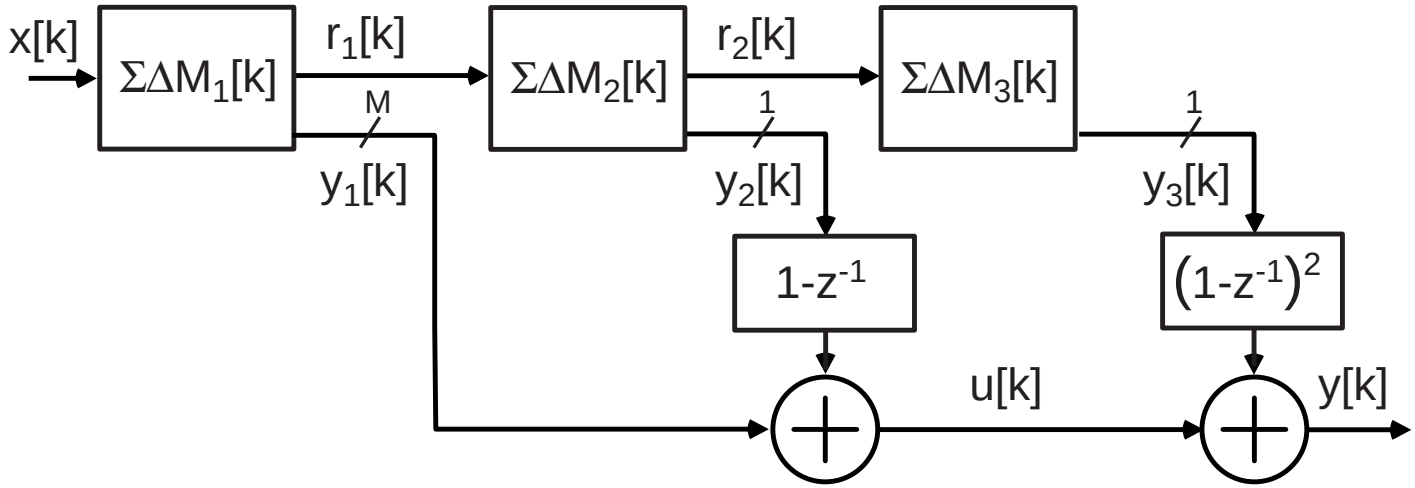
- **Quantization noise, r[k], is best whitened when a "sufficiently exciting" input is applied to the modulator**
  - **Varying input and high order helps to "scramble" interaction between input and quantization noise**
- **Worst input for tone generation are DC signals that are rational with a low valued denominator**
  - **Examples (third order modulator with no dithering):**



Fractional Spurs Can Be Theoretically Eliminated

- **See:**
  - **M. Kozak, I. Kale, “Rigorous Analysis of Delta-Sigma Modulators for Fractional-N PLL Frequency Synthesis”, *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 51, no. 6, pp. 1148-1162**
  - **S. Pamarti, I. Galton, "LSB Dithering in MASH Delta–Sigma D/A Converters", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 4, pp. 779 – 790, April 2007.**

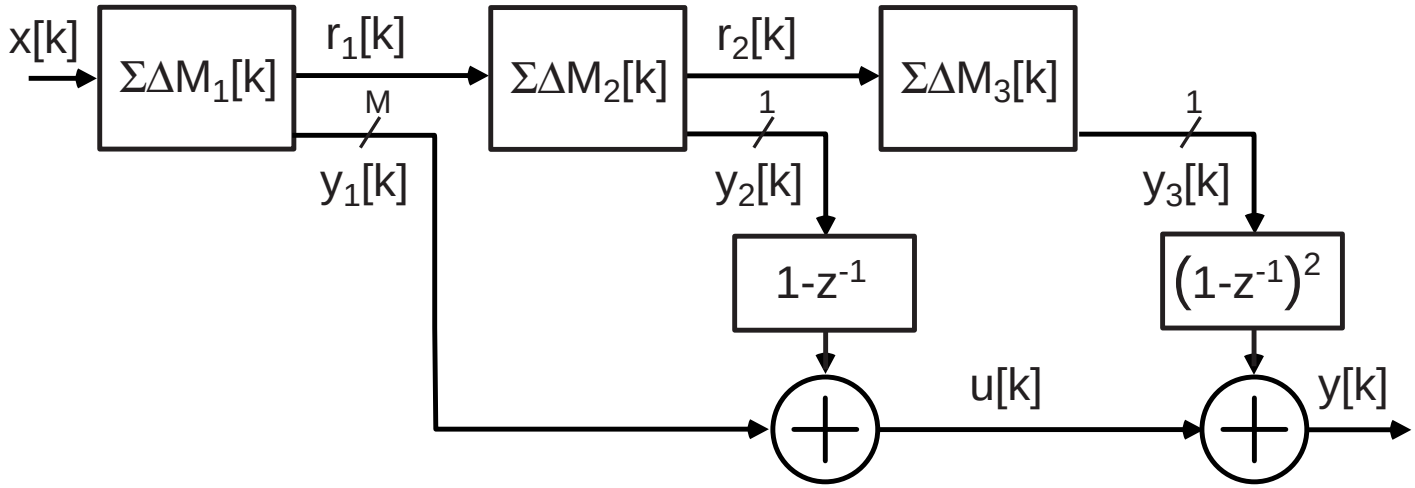
MASH topology



- **Cascade first order sections**
- **Combine their outputs after they have passed through digital differentiators**

- **Advantage over single loop approach**
  - **Allows pipelining to be applied to implementation**
    - High speed or low power applications benefit

Calculation of STF and NTF for MASH topology (Step 1)



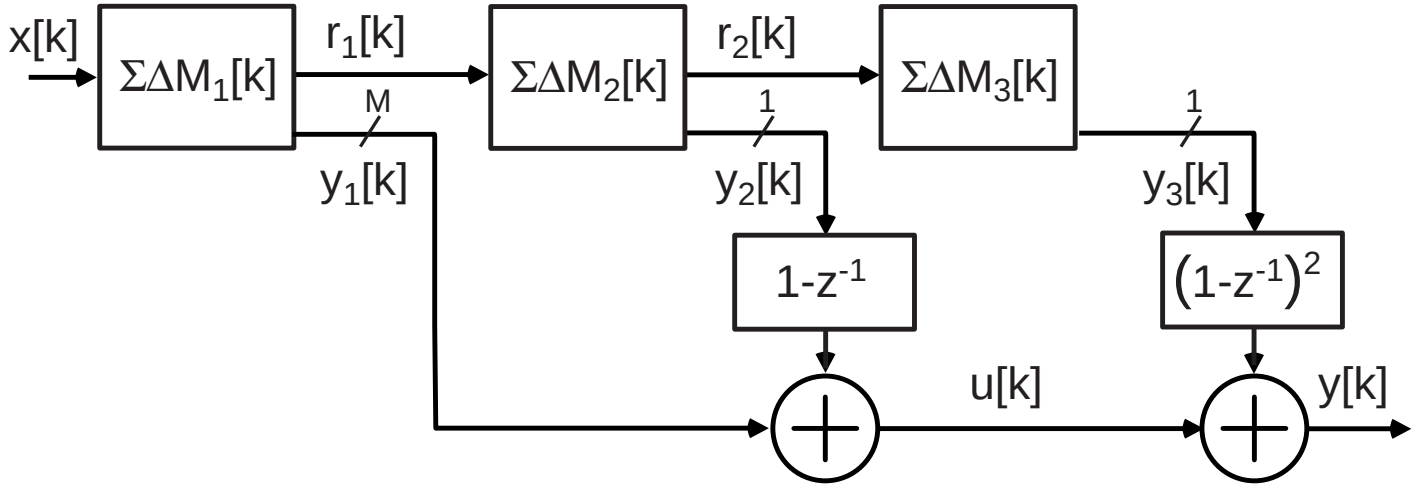
- **Individual output signals of each first order modulator**

$$
\begin{aligned}
y_1(z) &= x(z) - (1-z^{-1})r_1(z) \\
y_2(z) &= r_1(z) - (1-z^{-1})r_2(z) \\
y_3(z) &= r_2(z) - (1-z^{-1})r_3(z)
\end{aligned}
$$

- **Addition of filtered outputs**

$$
\begin{aligned}
& y_1(z) \\
+ \quad & (1-z^{-1})y_2(z) \\
+ \quad & (1-z^{-1})^2 y_2(z) \\
\hline
= \quad & x(z) - (1-z^{-1})^3 r_3(z)
\end{aligned}
$$

Calculation of STF and NTF for MASH topology (Step 1)

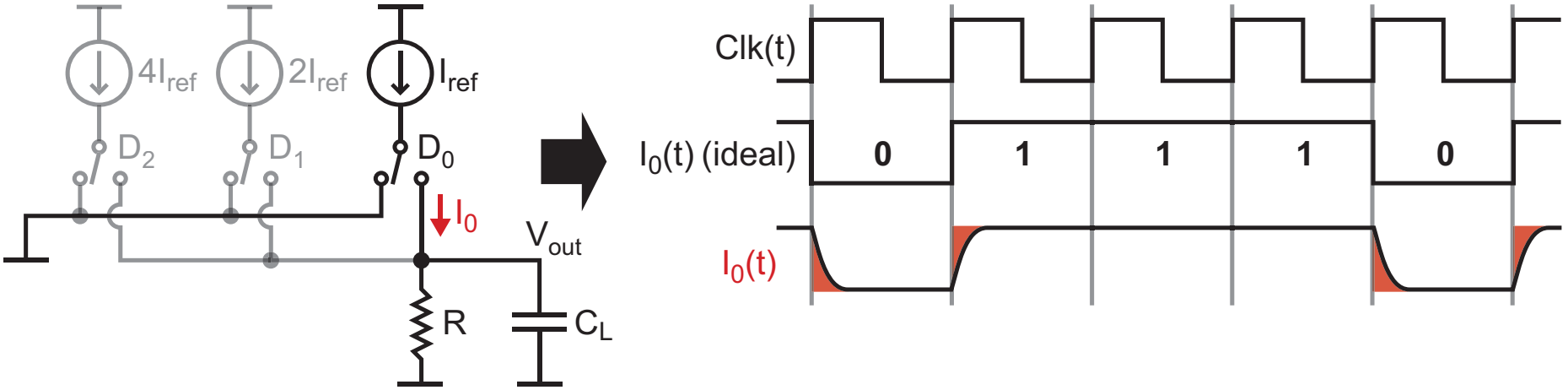


- **Overall modulator behavior**

$$y(z) = x(z) - (1 - z^{-1})^3 r_3(z)$$

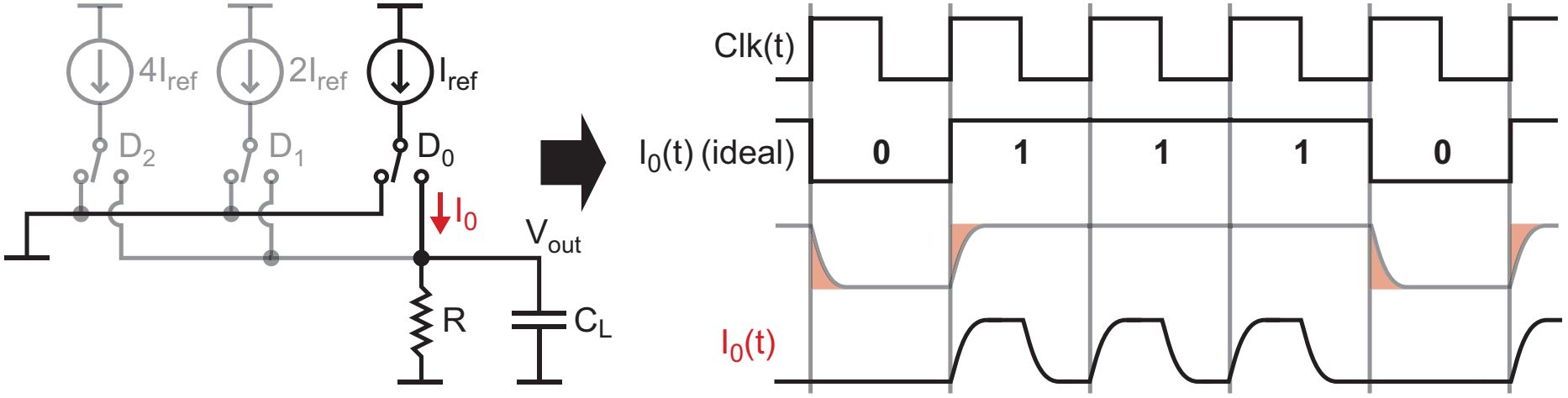
  - **STF: $H_s(z) = 1$**
  - **NTF: $H_n(z) = (1 - z^{-1})^3$**

The Issue of Intersymbol Interference



- **Dynamic operation of a non-return-to-zero (NRZ) DAC leads to inaccuracy due to transient effects**
  - **Transients only occur when the previous data is different**
    - We refer to this data dependent error as intersymbol interference
- **Intersymbol interference especially poses a problem when using the DAC for data communication**

Return-to-Zero (RZ) Signaling



- Dynamic operation RZ DAC yields consistent results regardless of the pattern
  - Essentially, it inserts transients into every `1' value
- Issue – half the signal swing is lost

Summary

- DAC structures can be implemented in a variety of ways
  - Resistors, currents, capacitors are all possible elements
  - Current-based DACS are the favorite for high frequency operation
  - Capacitor-based DACS are the favorite for low to modest frequency operation
- Key DAC specifications include offset, gain error, and non-linearity
  - Monotonocity is an import specification for DACs used within feedback loops
- Sigma-Delta modulators can be used to greatly increase the *effective* resolution of a DAC
- Dynamic operation of the DAC can lead to error due to intersymbol interference