Optical/Electronic Interface Architectures for Phase Locking and Downconversion/Digitization of Narrowband RF Signals

Workshop on Ultrafast Lasers
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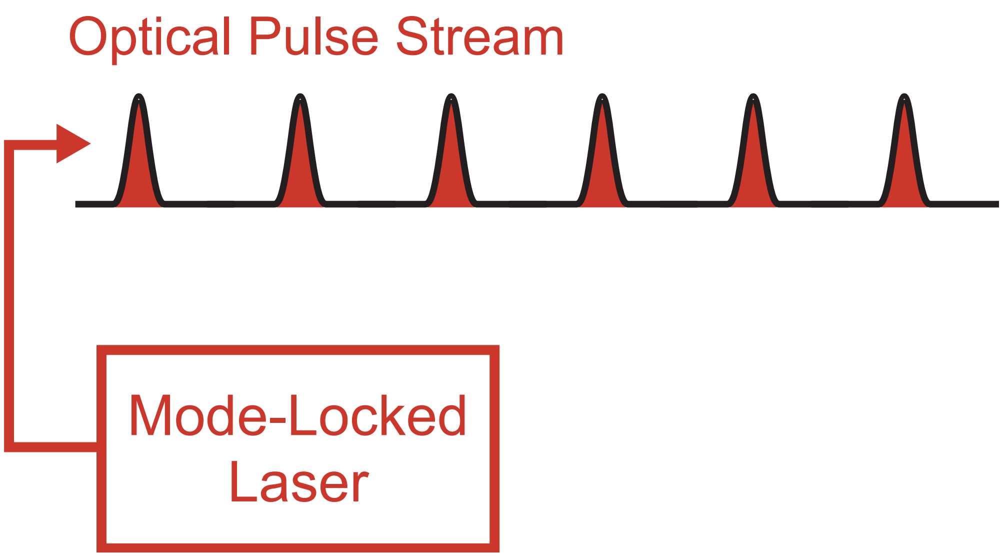
Our Starting Point

- **Questions:**
  - **What advantages do optical components bring to classical electronic applications?**
  - **When merging optical and electronic components for such applications, where are the best boundaries between the two?**

- **Focus areas:**
  - **Phase-locked loops**
  - **Sampling, downconversion and digitization of narrowband RF signals**

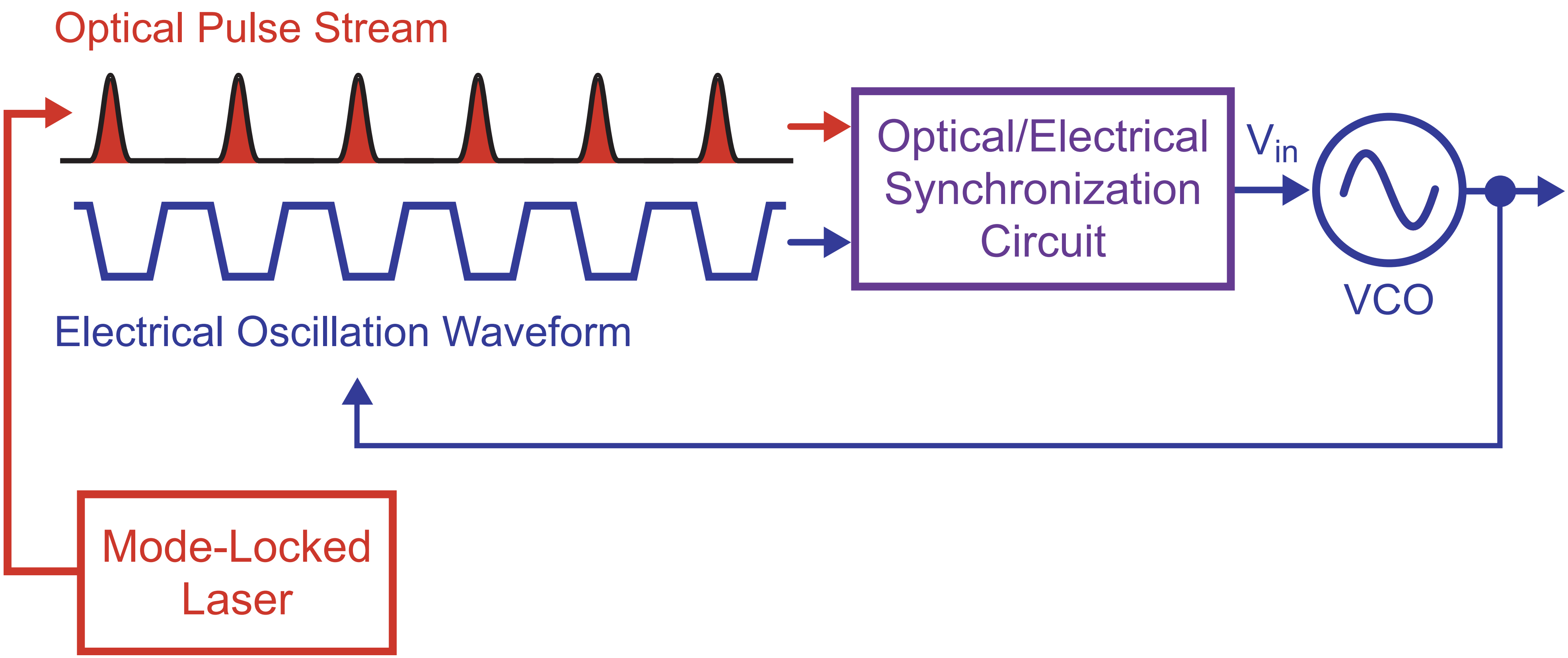
The Attraction of Optical Components for Phase Locking



- **Mode-locked lasers provide optical clock streams with excellent short term jitter characteristics**
  - **Short term jitter < 10 fs is achievable**

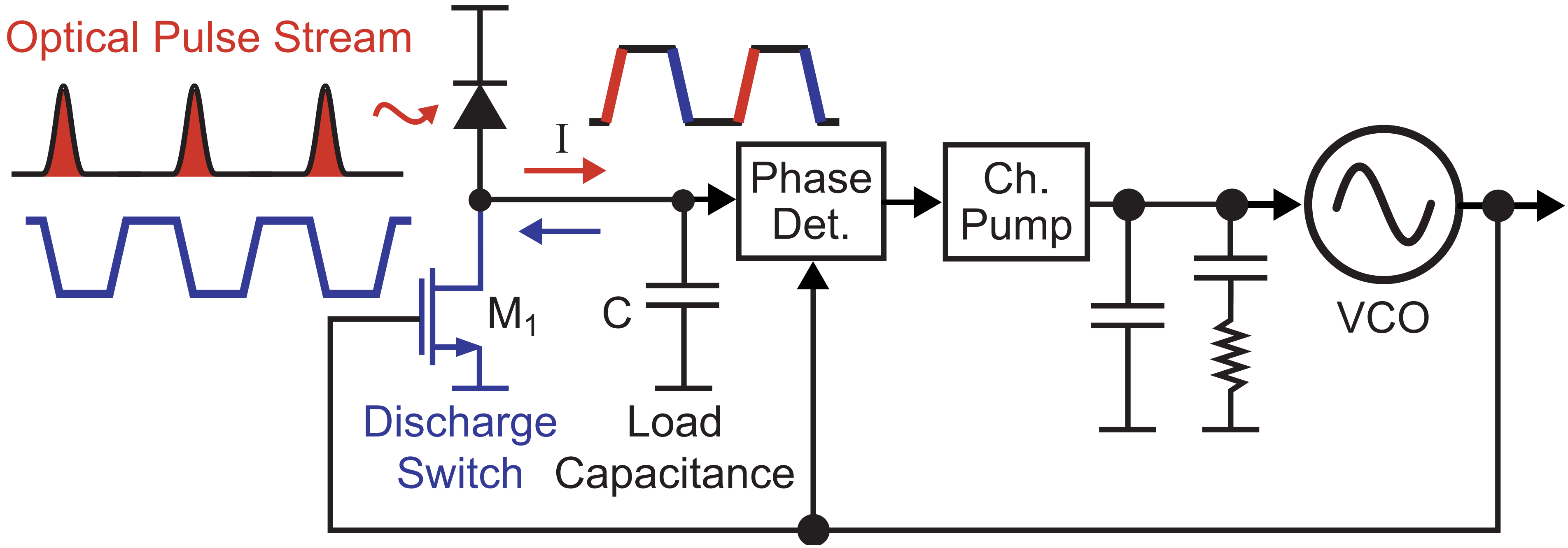
Can we lock an electrical clock to the optical pulse stream AND maintain low jitter?

Optical/Electrical Phase Locked Loops



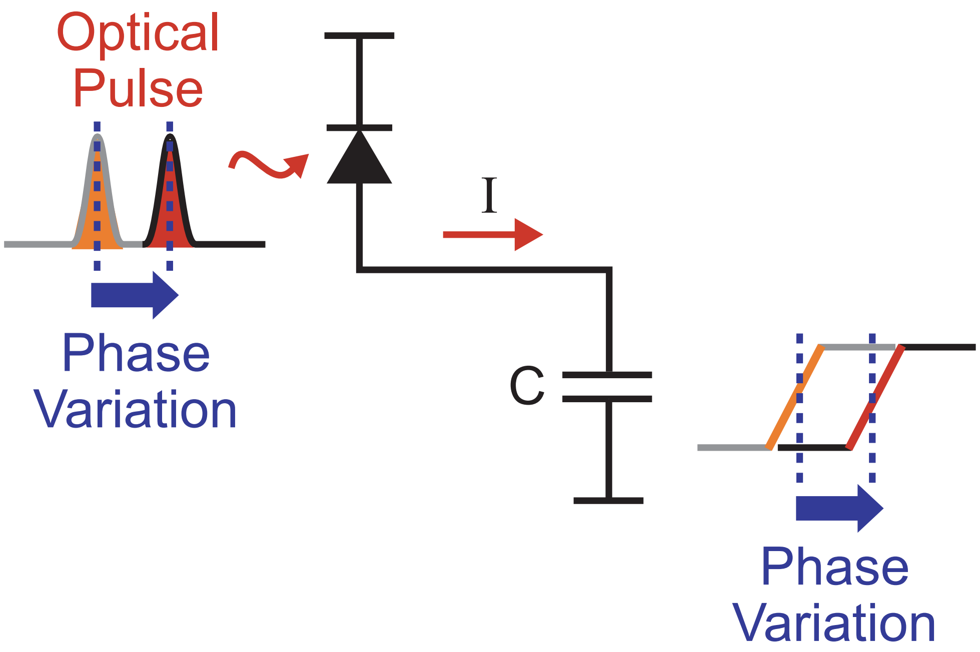
- **Generate a frequency tunable electronic clock source by using a voltage controlled oscillator (VCO)**
- **Lock VCO output to pulse stream using an optical/electrical synchronization circuit**

Method 1 of Implementing the Synchronization Circuit



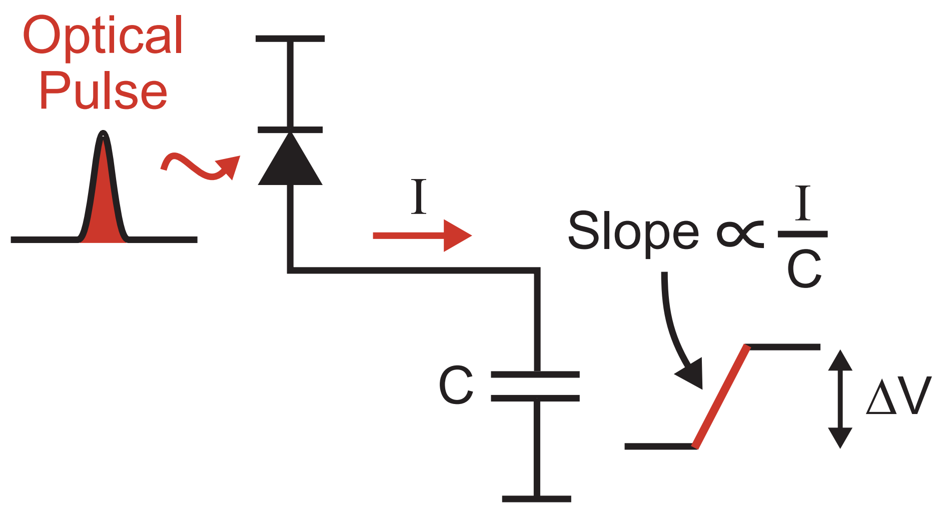
- **Create an electrical square wave reference signal by using a photodiode and discharge switch**
- **Lock the VCO output to the electrical reference signal by using a conventional electronic phase locked loop**

Key Idea of Method 1: Measure Phase Based on Edges



- **Relative phase positions of optical pulses are captured by the edge locations of the electrical reference waveform**

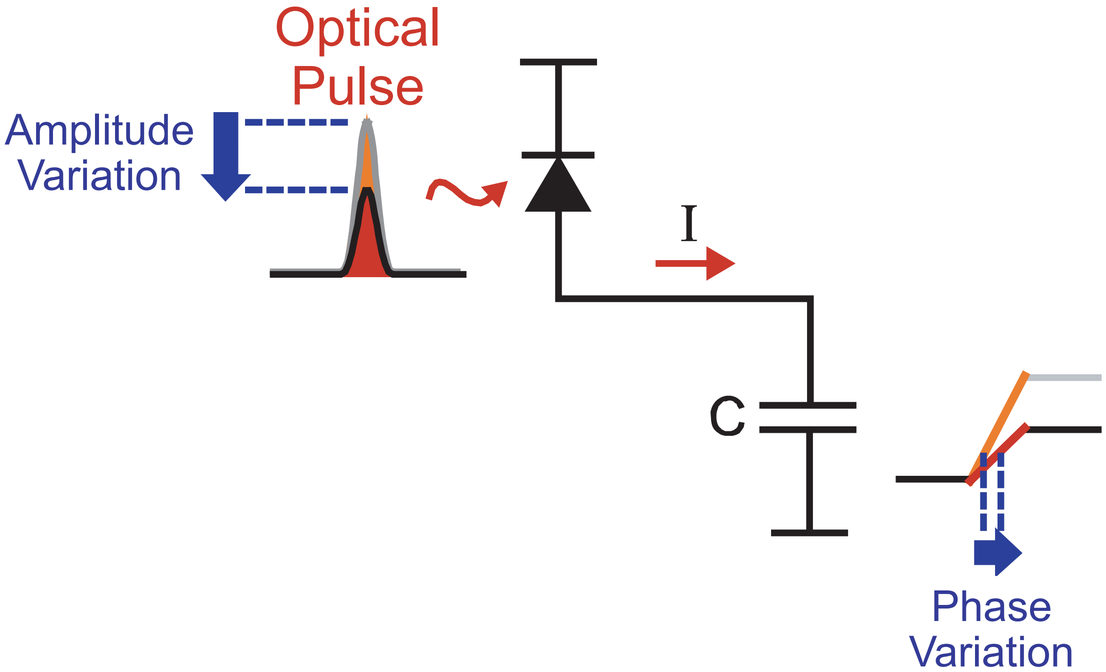
Issue 1: Noise



- **The slope of the transition edges is limited by the current/capacitance ratio at the photodetector output**
- **Higher edge slopes are desirable to achieve low noise**
  - **Voltage noise present in the reference waveform translates to timing jitter according to the edge slope**

Achievable noise performance is limited by the I/C ratio of the electronics (i.e., photodiode and the capacitive load it drives)

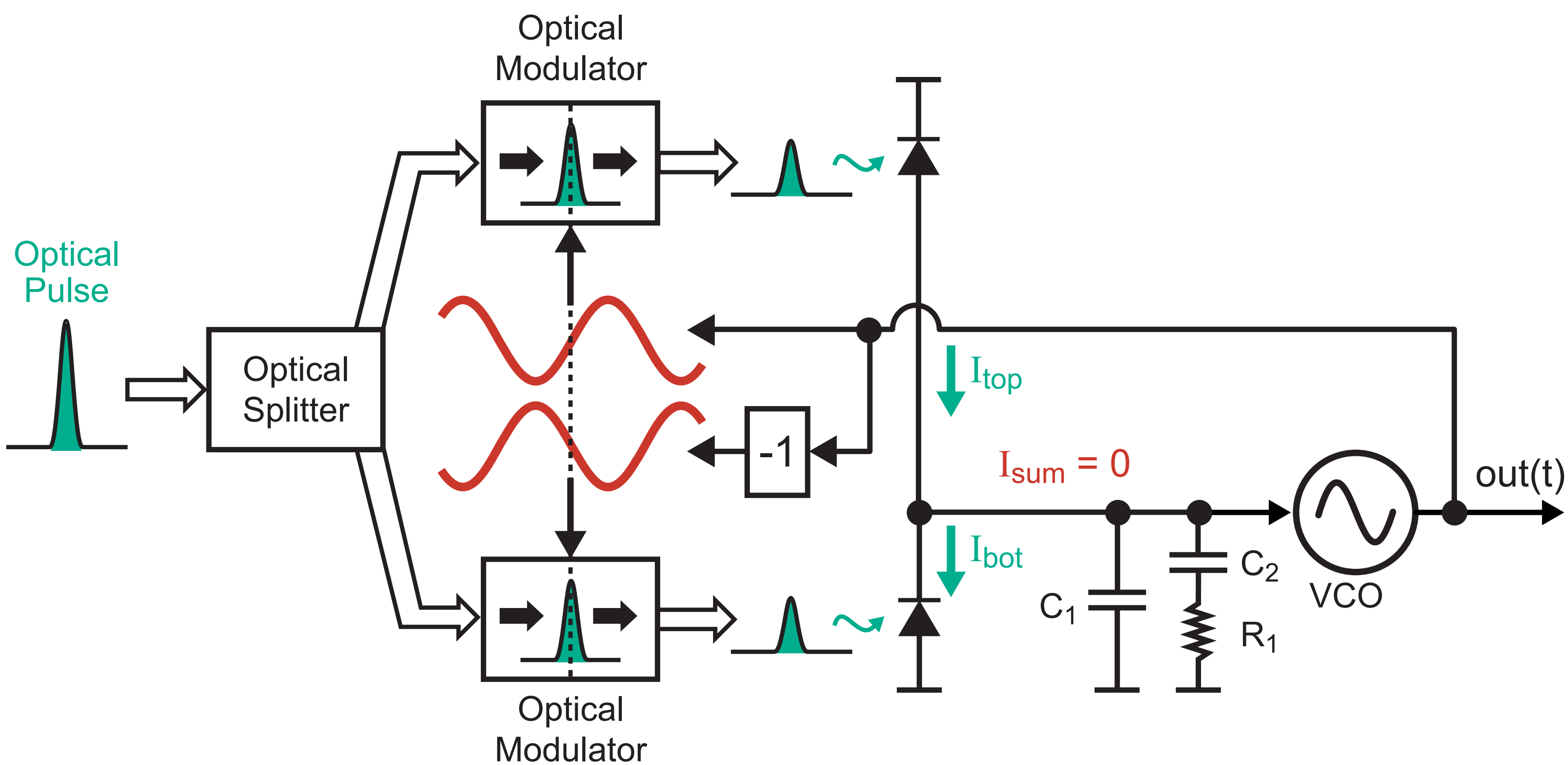
Issue 2: Sensitivity to Amplitude Variation



- **Practical pulse streams from mode-locked lasers exhibit undesired amplitude variation**
- **Phase detection based on the edge-based approach above translate pulse amplitude variation into phase variation**

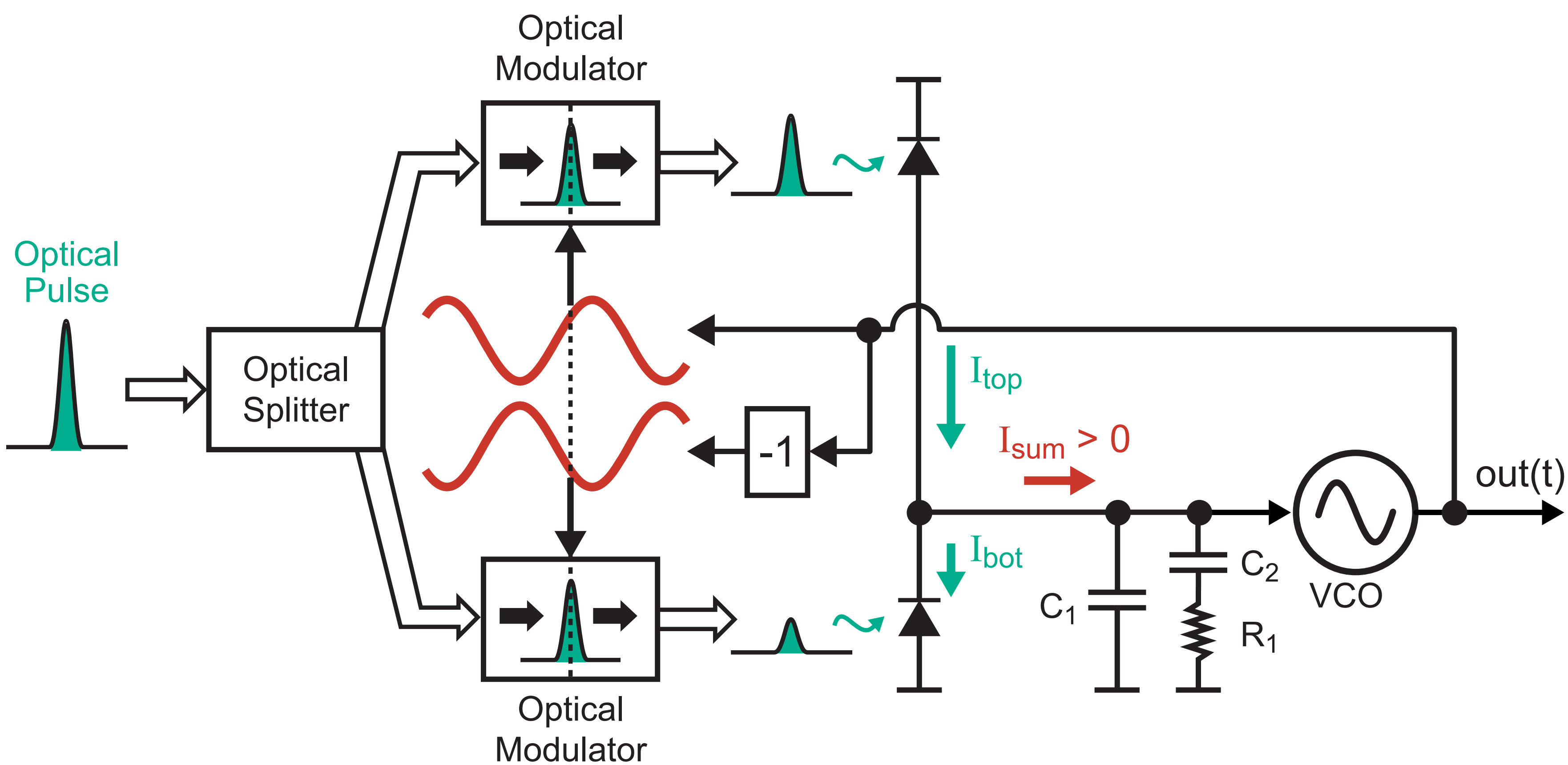
Can We Do Better?

Proposed Approach



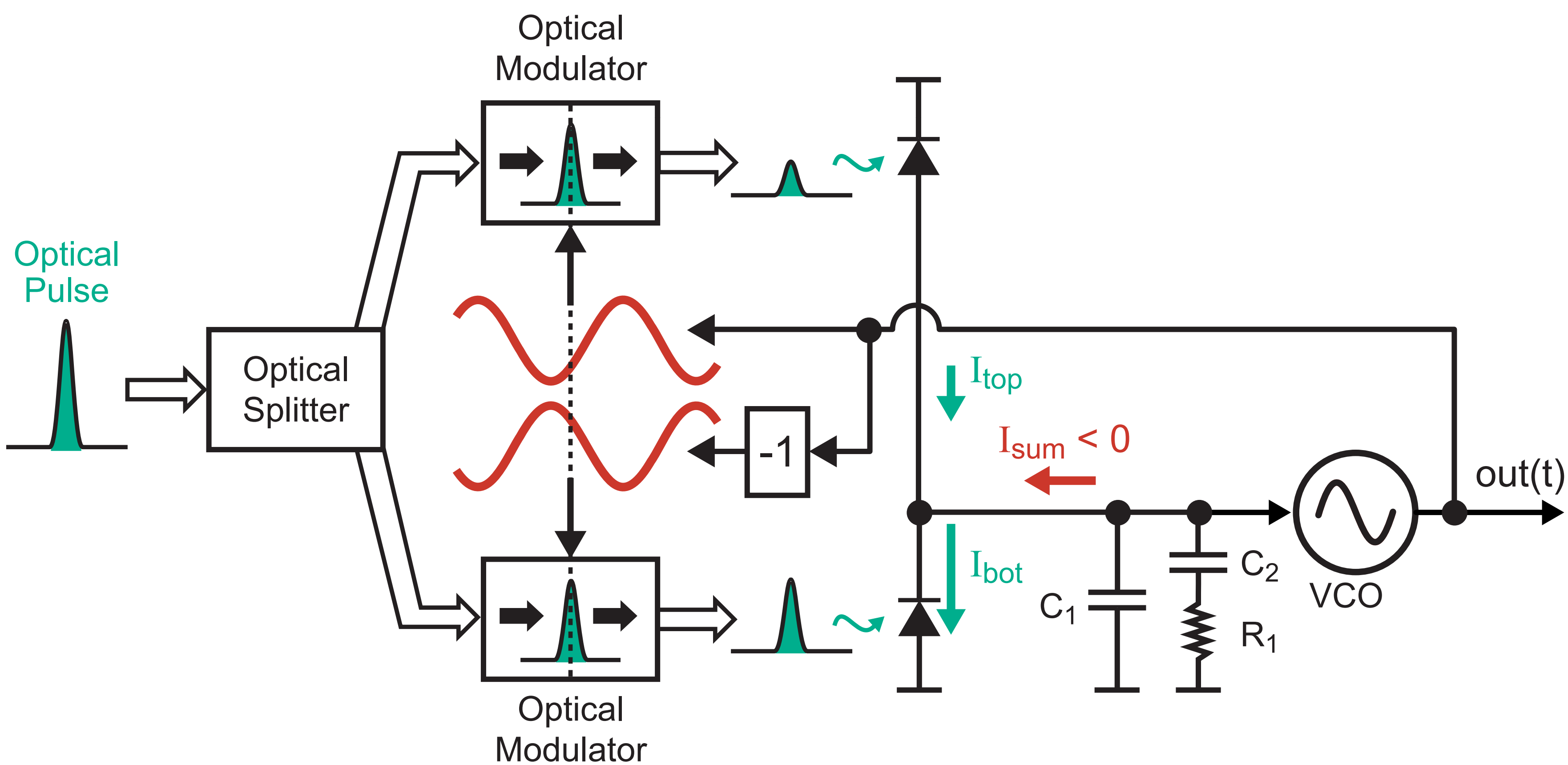
- **Move phase comparison into the optical domain**
  - **Passing an optical pulse through an optical modulator effectively samples its input value at the time**
- **Use photodetectors to detect the average *power* of the modulator outputs**

Impact of VCO Output Phase Being Too Early



- **An imbalance of modulator output power levels causes a difference in current between the top and bottom photodetectors**
  - **The resulting current causes the VCO input voltage to rise**

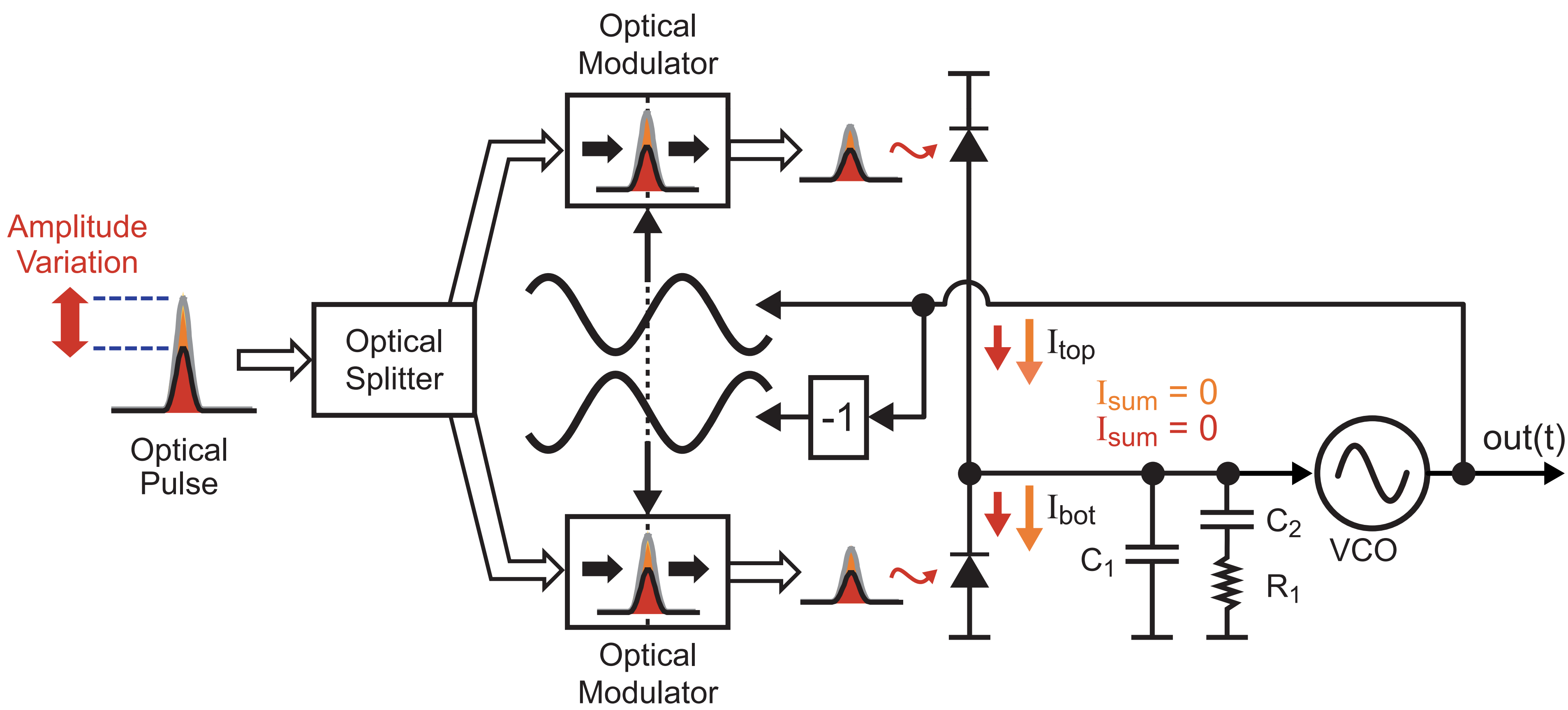
Impact of VCO Output Phase Being Too Late



- **Current imbalance shifts the opposite way, so that the VCO control voltage now starts to fall**

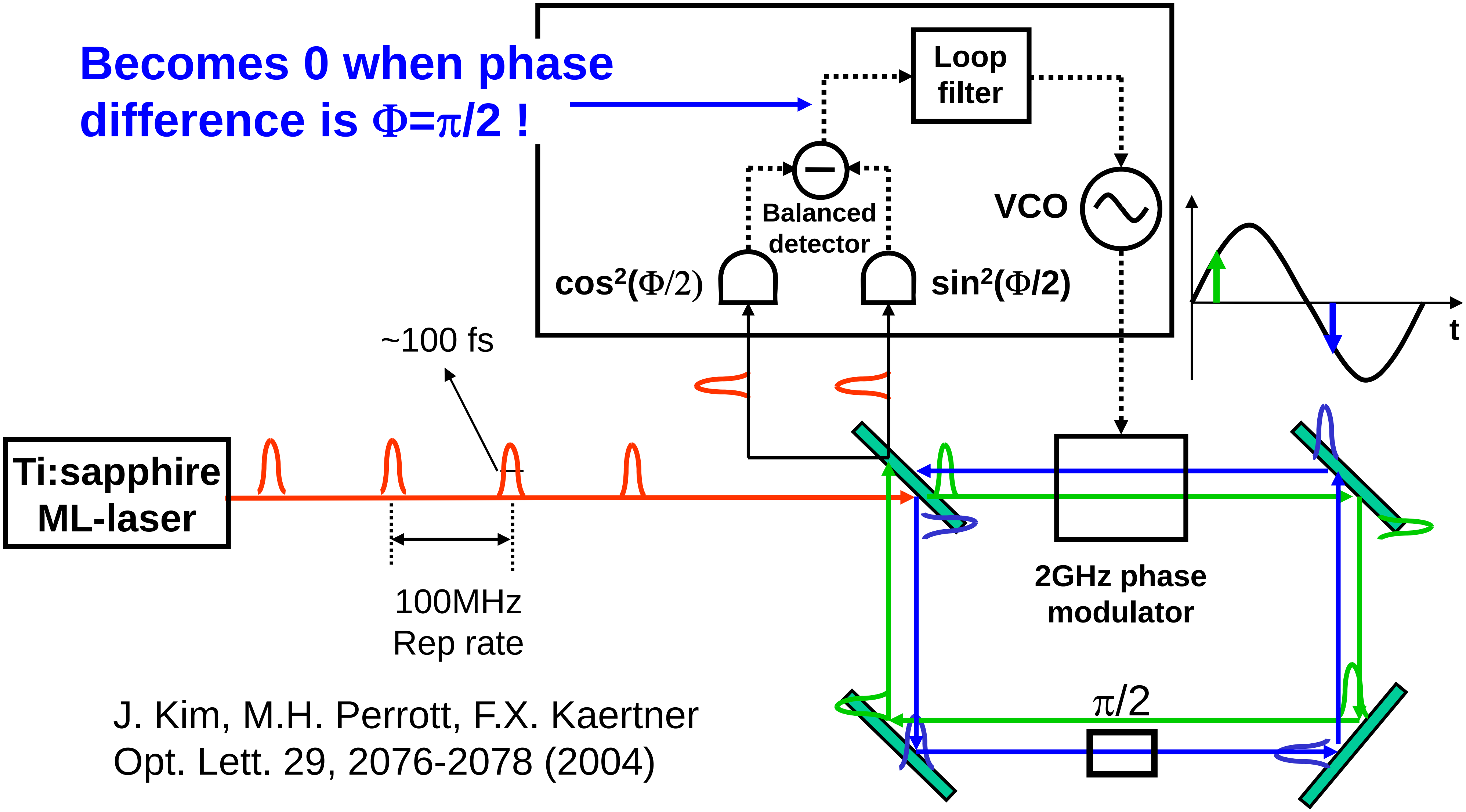
Accurate measurement of phase error is achieved

Approach is Insensitive to Amplitude Variations



- **Amplitude fluctuations impact the top and bottom currents equally (at least to first order)**
  - **The VCO control voltage remains undisturbed**

Actual Implementation

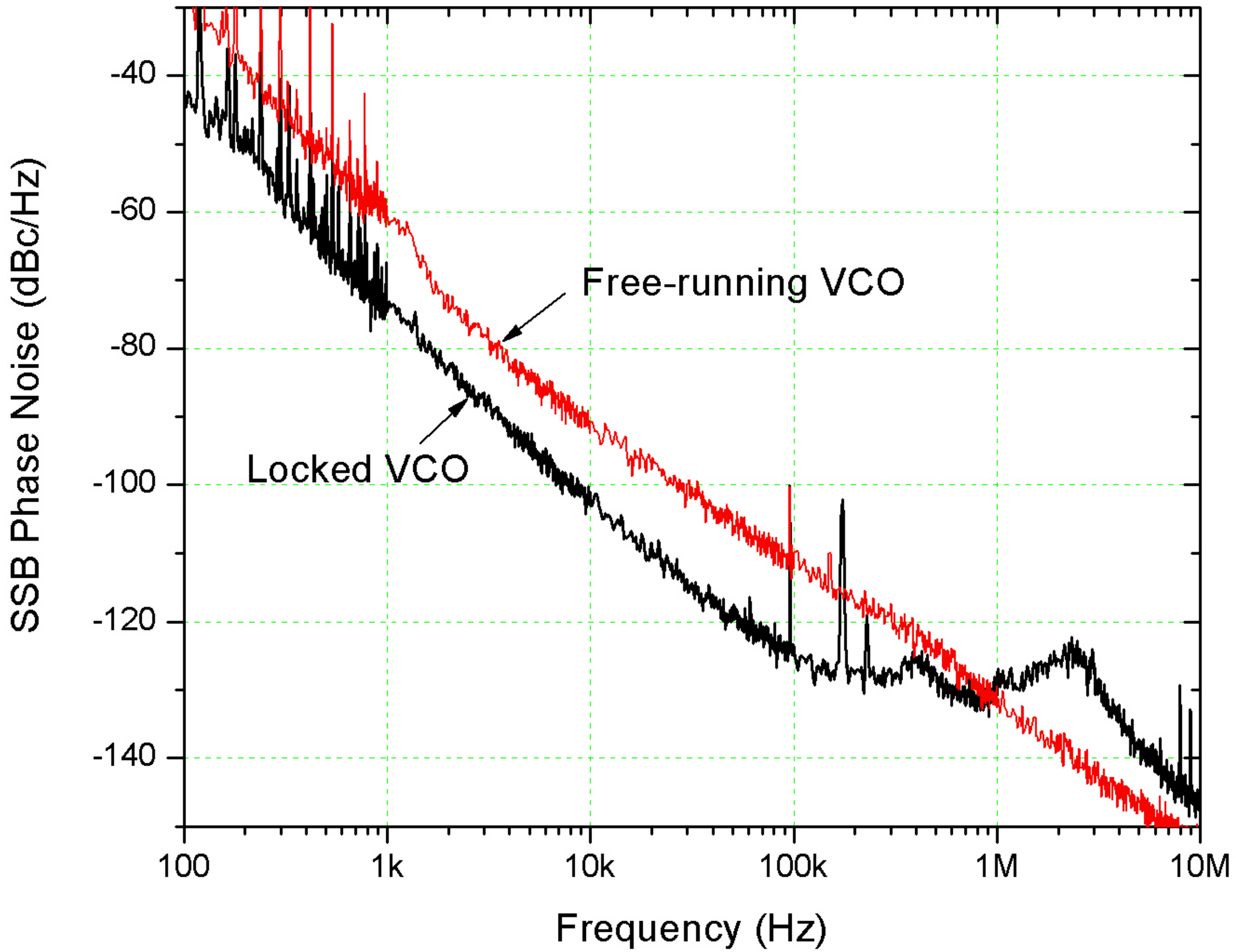


J. Kim, M.H. Perrott, F.X. Kaertner
Opt. Lett. 29, 2076-2078 (2004)

- **Use Mach-Zehnder interferometer within Sagnac-loop**
  - **Robust against temperature fluctuations**

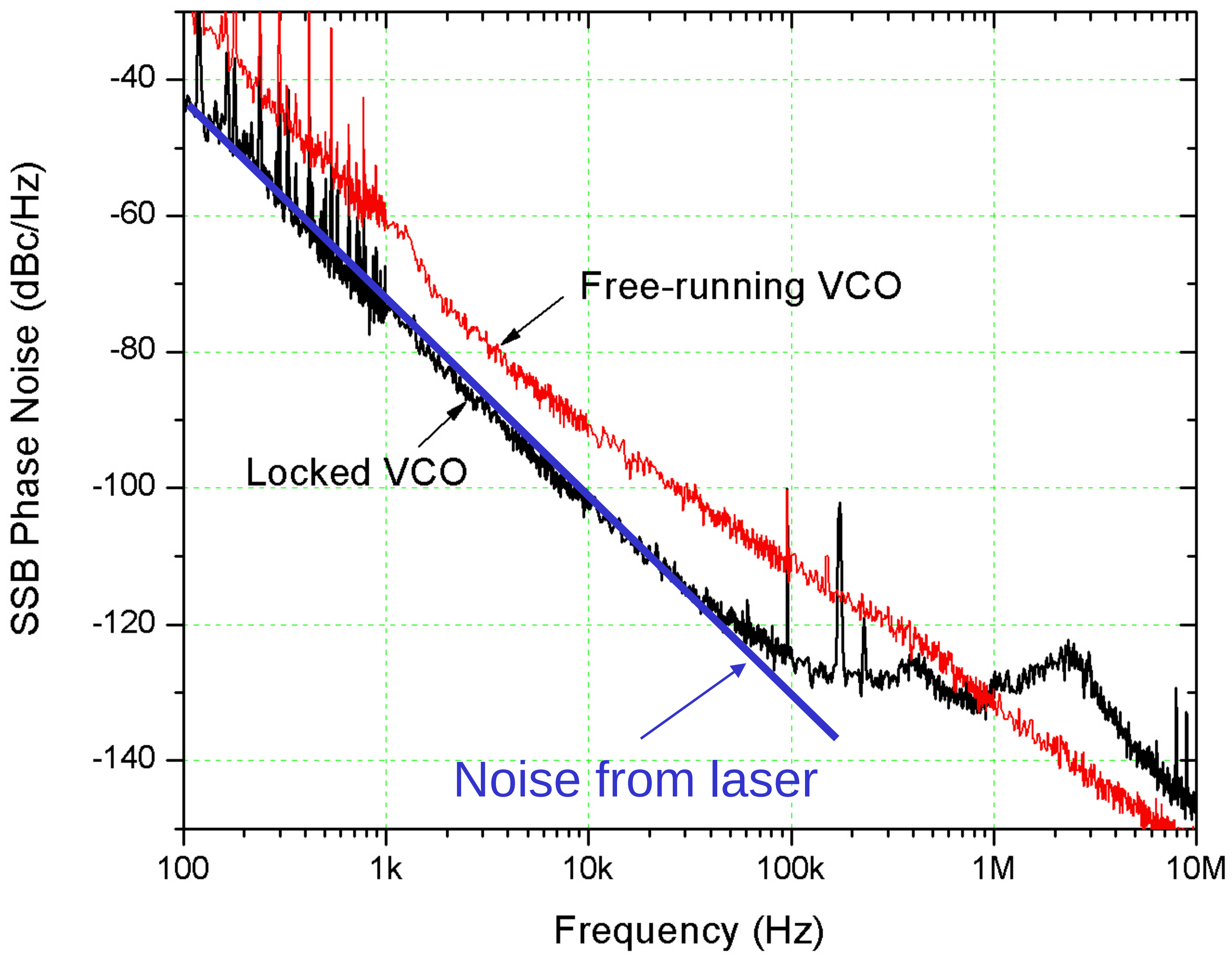
Measured Results

- **Locking is achieved with > 1 MHz bandwidth**



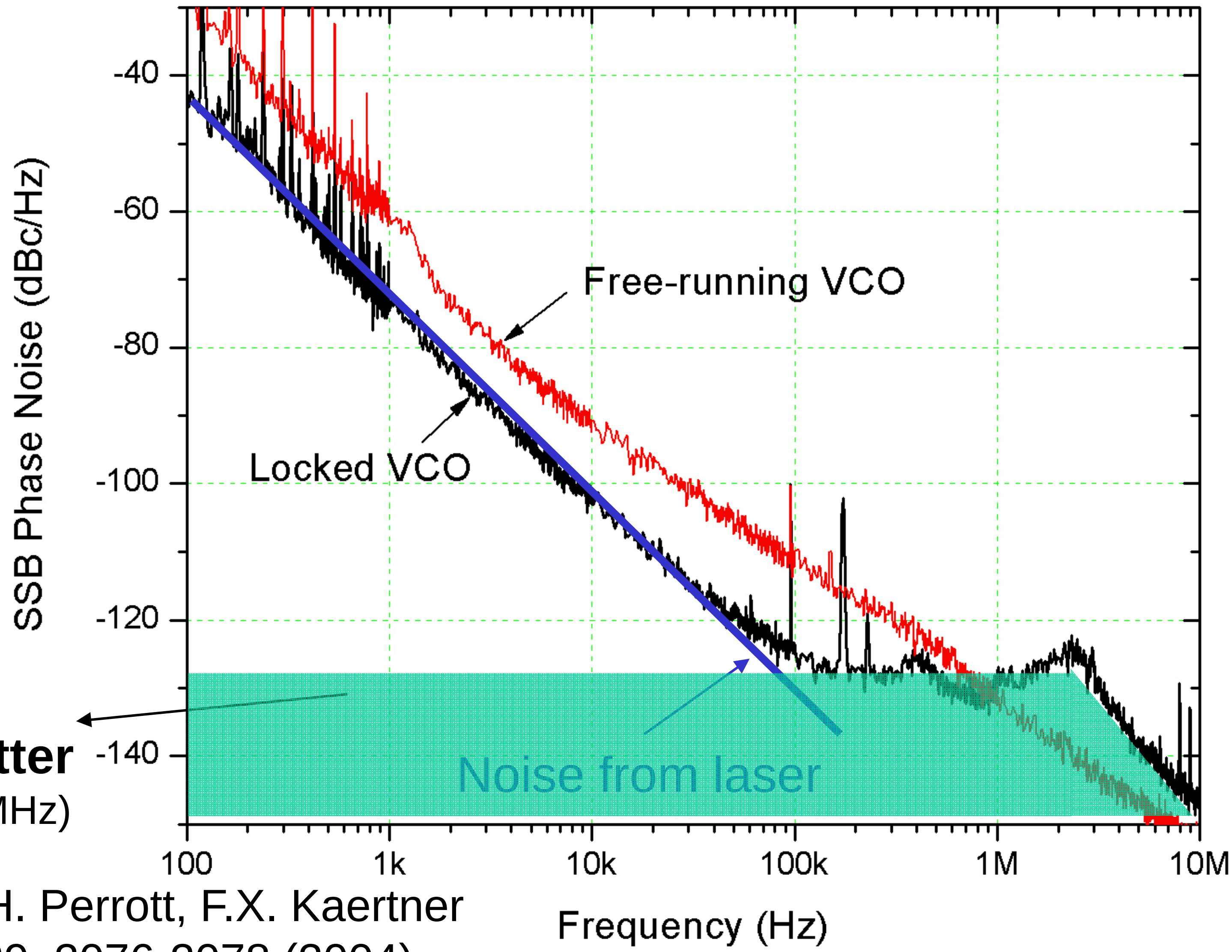
Limitation in Achieving Low Absolute Jitter

- **Noise of laser noise dominates at low frequencies**



Estimate of Relative Noise Between VCO and Laser

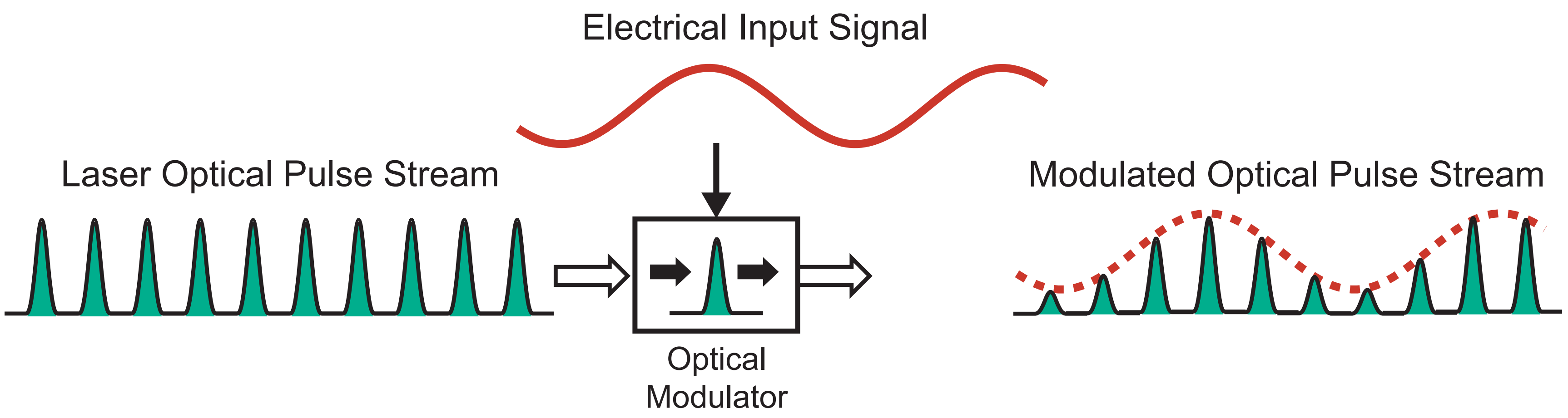
- **A separate experiment led to the estimate below**



<60 fs
Timing jitter
(100Hz-10MHz)

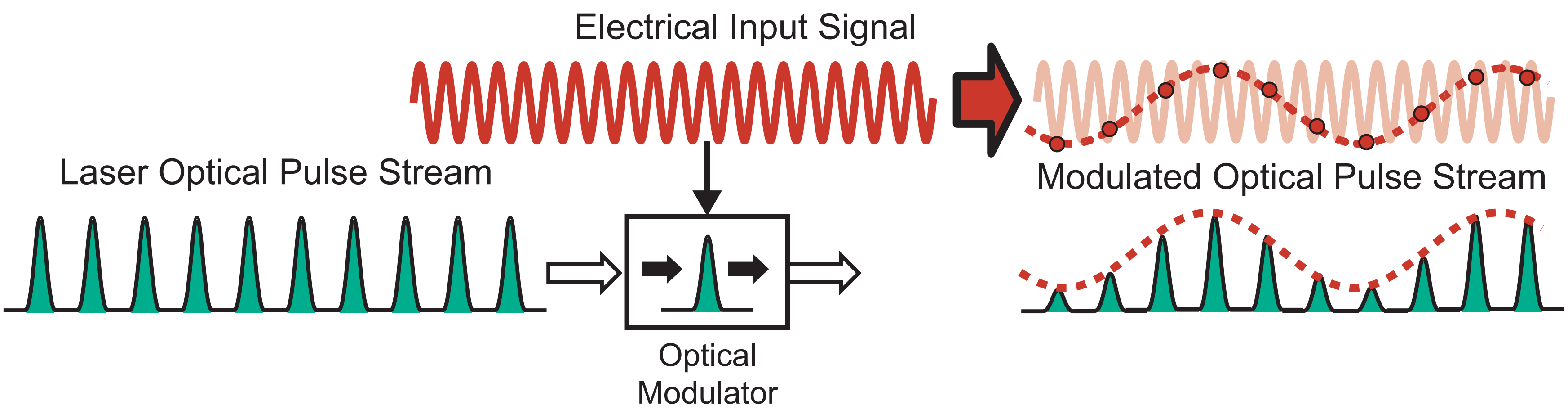
J. Kim, M.H. Perrott, F.X. Kaertner
Opt. Lett. 29, 2076-2078 (2004)

Optical Sampling of Electrical Signals



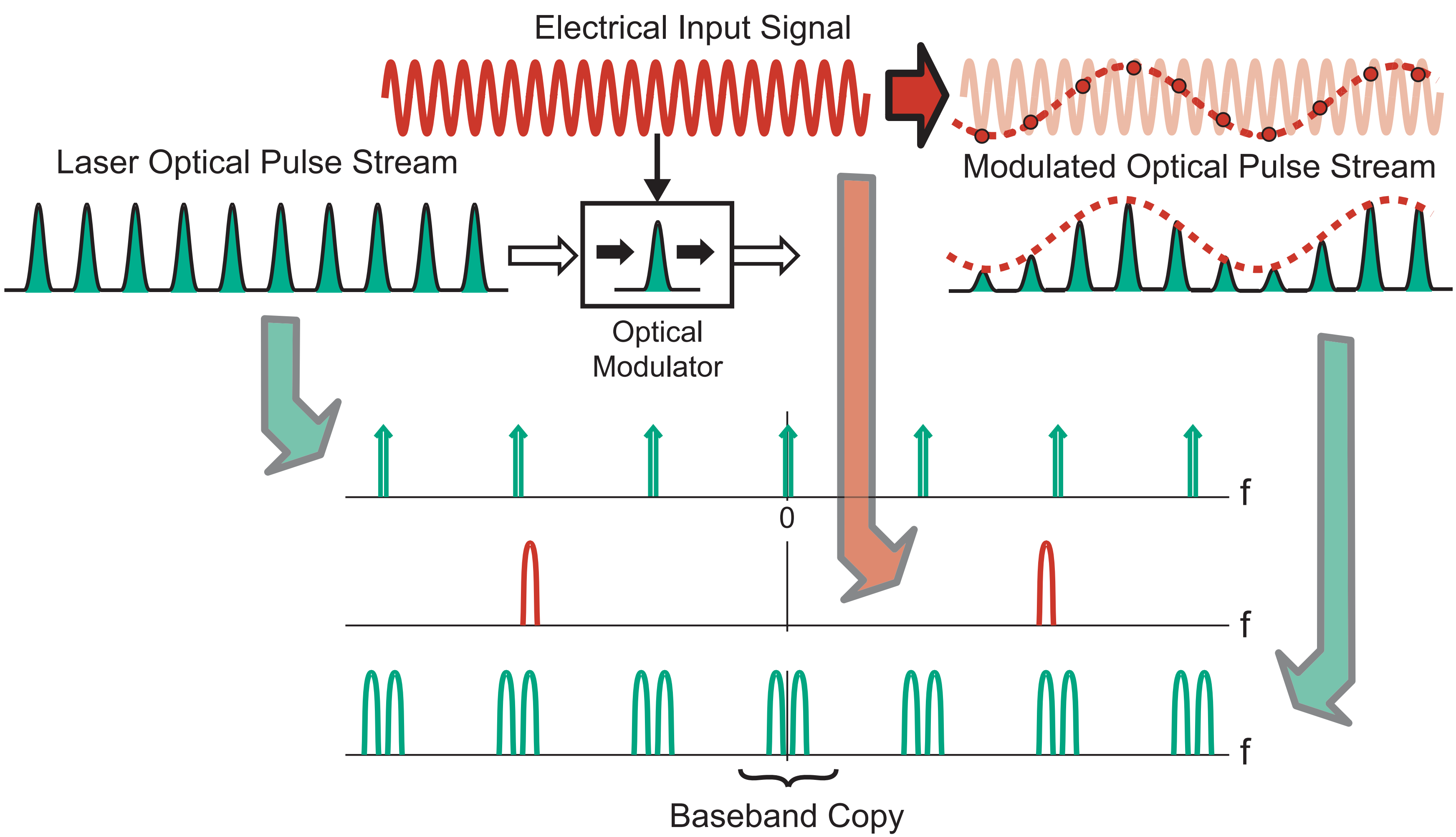
- **Optical modulator enables *low jitter* sampling of electrical signal**
- **Applications:**
  - **Input sampler for A/D converter**
    - A/D converters are often limited by jitter in sampling process
  - **Sub-sampling downconverter for RF signal digitization**

Sub-sampled Downconversion of RF Signals



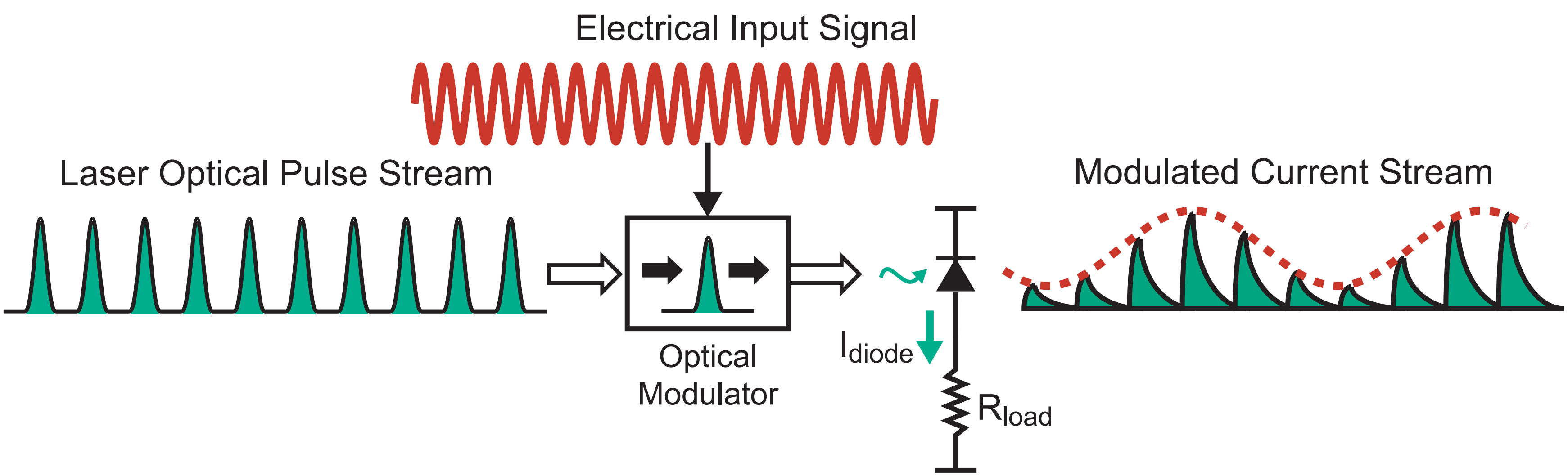
- **Sub-sampling a narrowband RF signal leads to a baseband signal component**
  - **We are purposefully *aliasing* the RF signal**
- **Good performance requires:**
  - **RF signal must be narrowband**
    - Use a resonant optical modulator to filter wider band RF components
  - **Sampling process must have low jitter**
    - Optical sampling offers very low jitter (< 10 fs possible)

Frequency Domain View of Sub-Sampling Downconversion



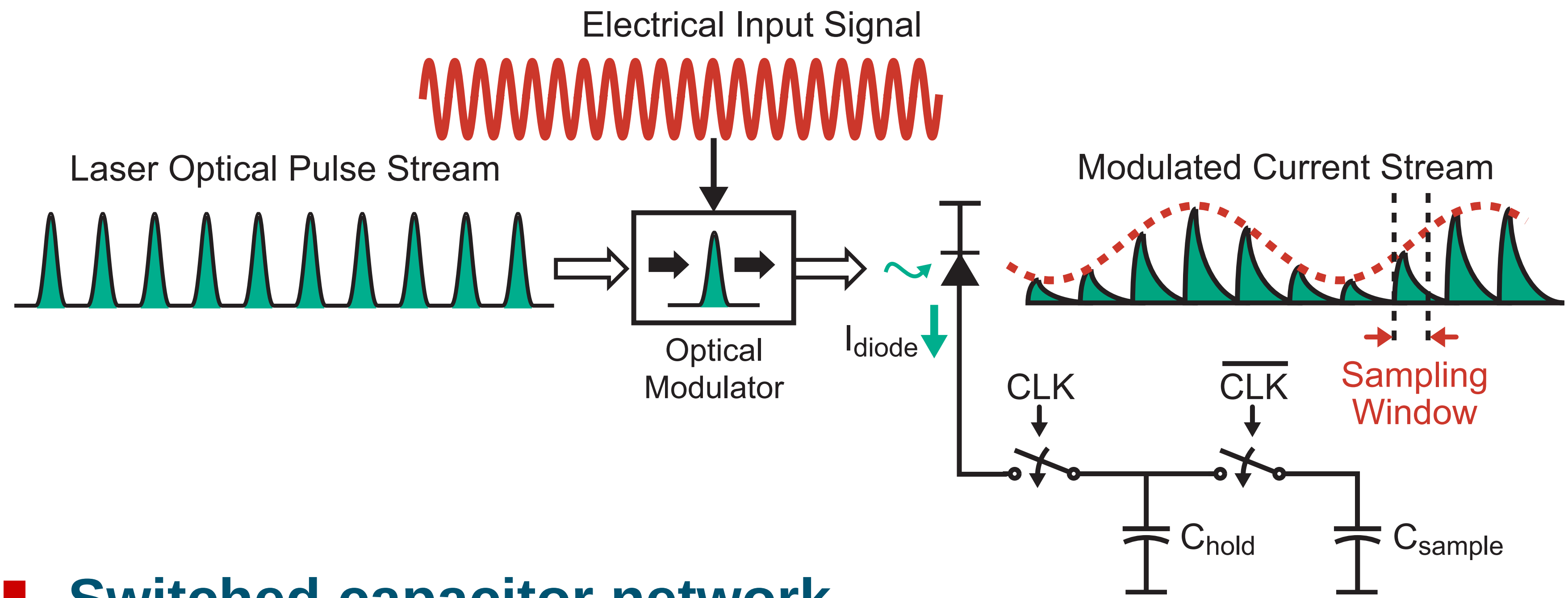
- **Optical pulse stream spectrum consists of equally spaced impulses in frequency**
  - **Impulse closest to RF signal downconverts it to baseband**

Conversion to Electrical Domain



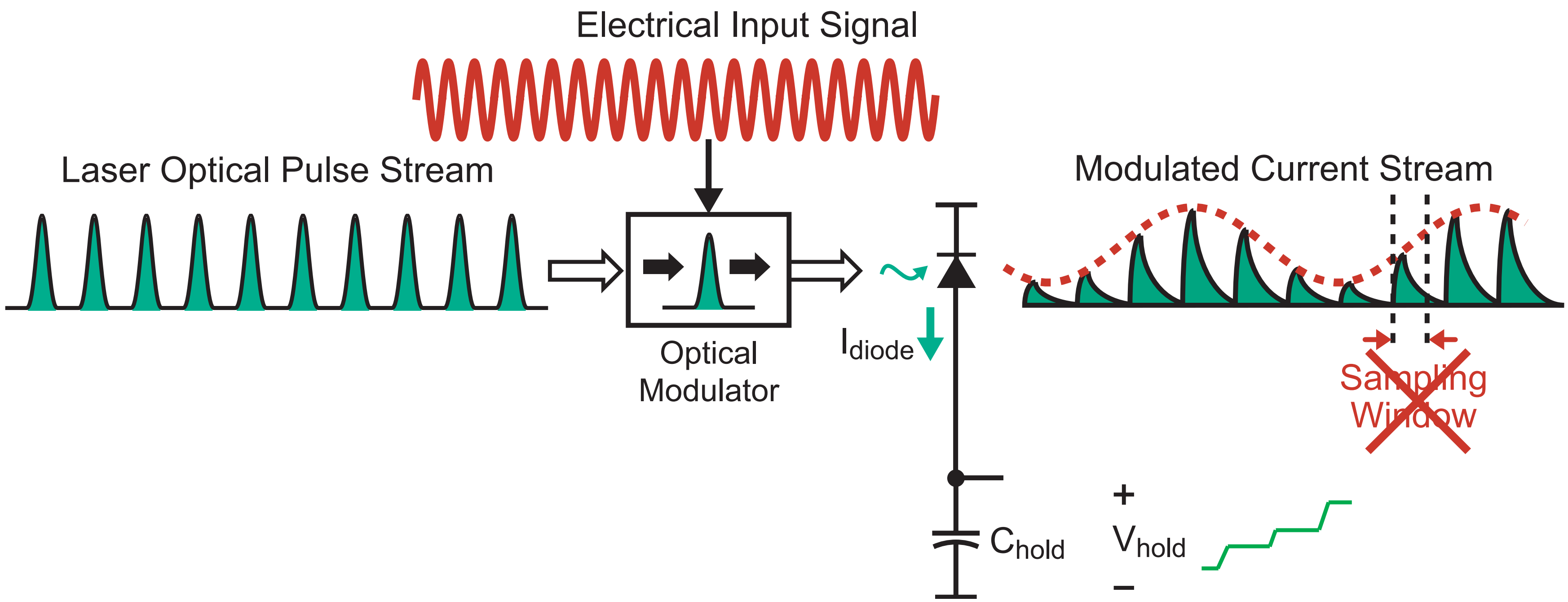
- **Photodiode used to convert modulated optical stream to modulated current stream**
  - **Issue: recombination in photodiode leads to parasitic tails in response to input optical pulses**
    - We no longer have pulses that are well confined in time
- **Issue: how do we transfer optical sample information to electrical samples?**

Transfer of Sampled Information to Electrical Domain



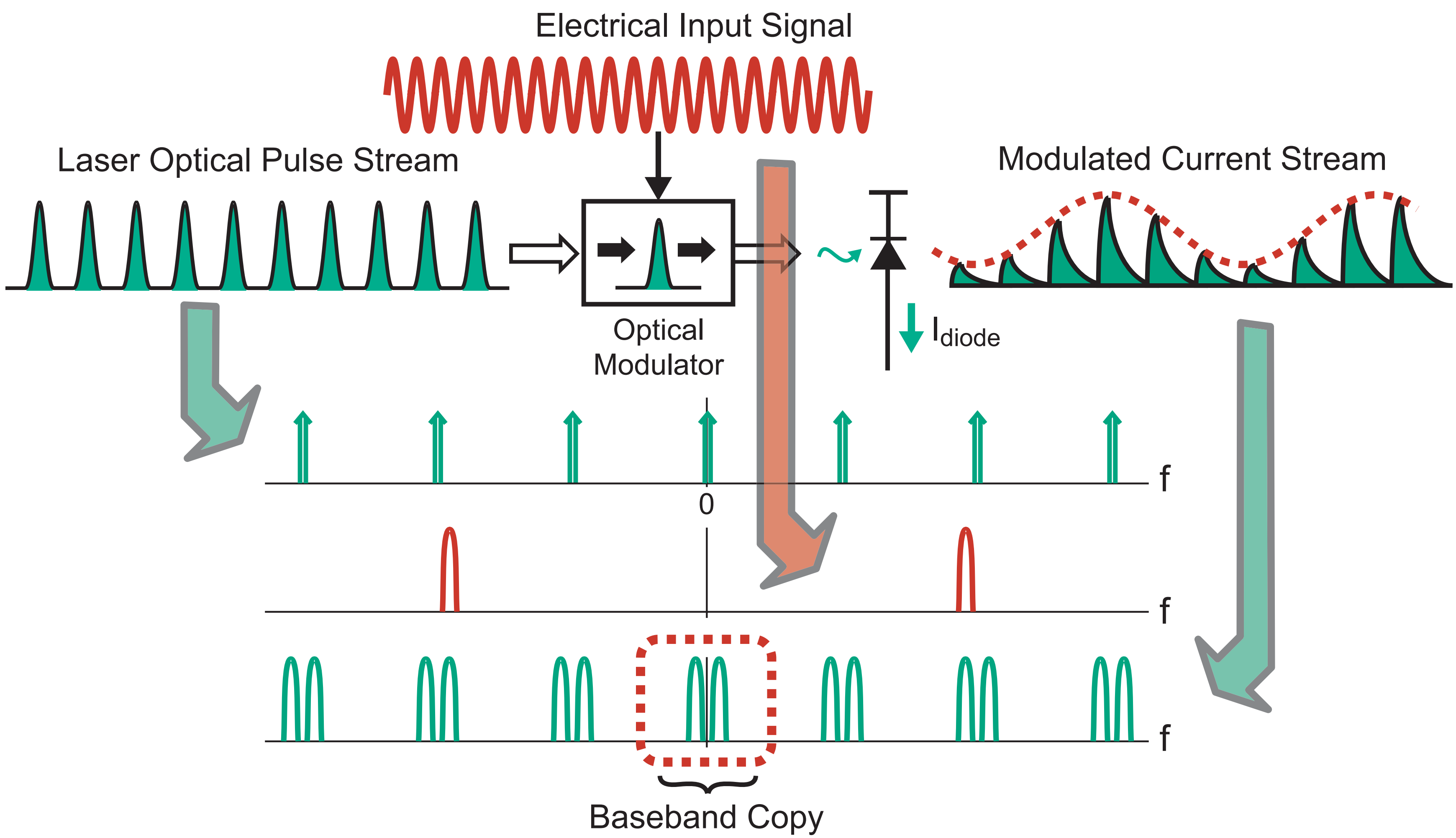
- **Switched capacitor network**
  - **Captures charge over a given time window and transfers to following stage**
- **Key issues:**
  - **Finite resistance of switches leads to large voltage deviations at photodiode output**
  - **Parasitic tail of photodiode response causes "leakage" of sample information to following electrical samples**

Consider Simply Storing Photodiode Charge



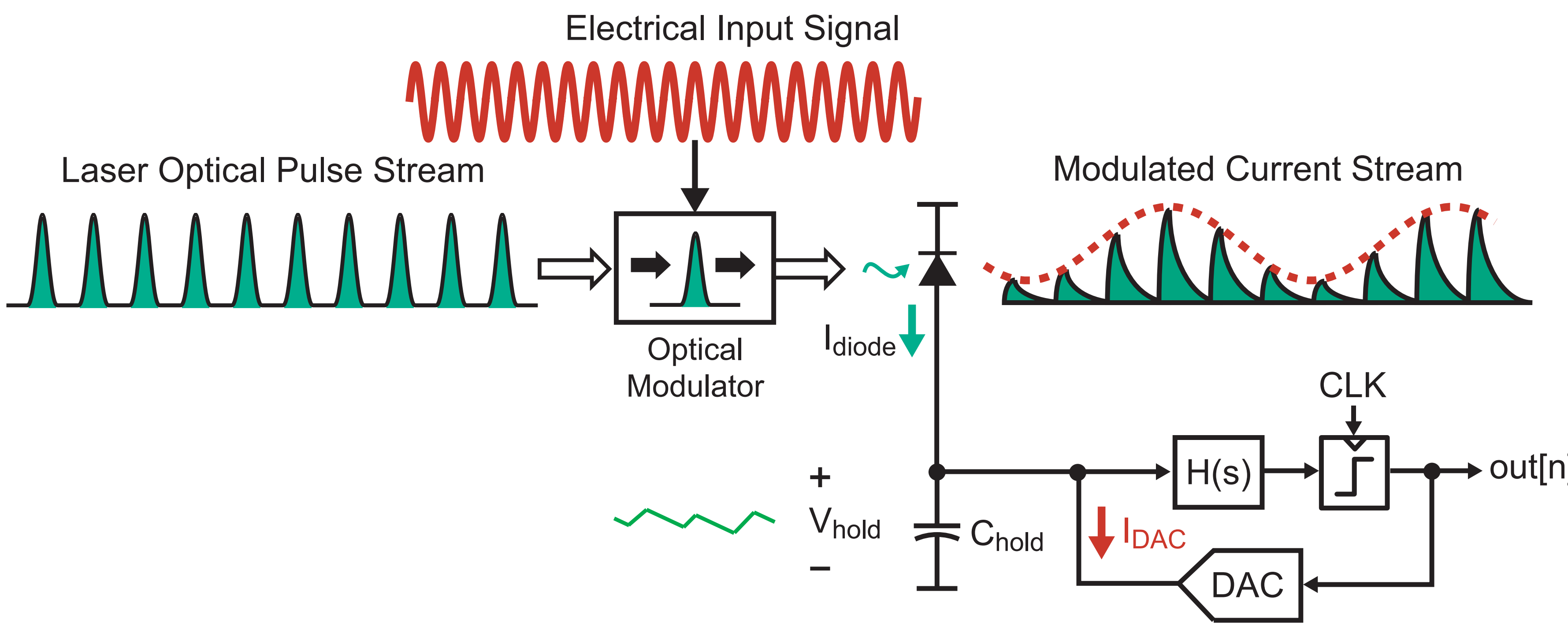
- **Send photodiode current directly into capacitor**
  - **Use of a high Q capacitor prevents large instantaneous voltage deviations at photodiode output**
    - Easily achieved with on-chip metal-metal capacitors
- **Issues:**
  - **Voltage across capacitor grows unbounded!**
  - **How do we transfer sample information?**

Key Observation



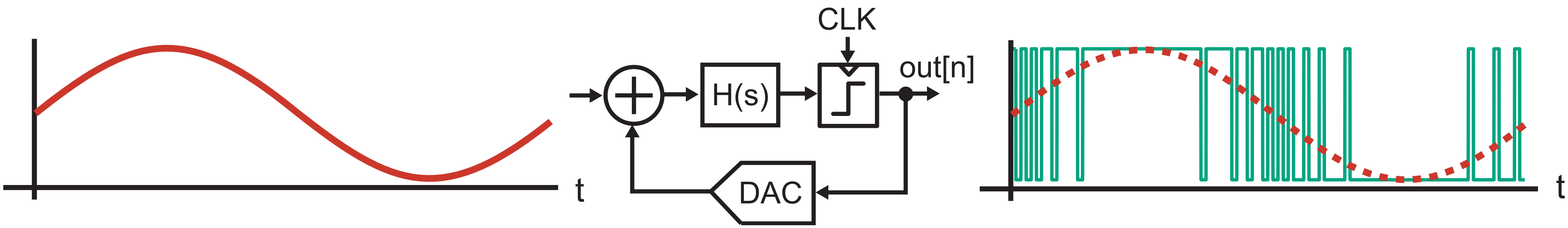
- **We need only extract filtered baseband copy**
  - **Explicit electronic sampling unnecessary if we use a continuous-time A/D structure**

Continuous-Time Sigma-Delta A/D is a Nice Fit



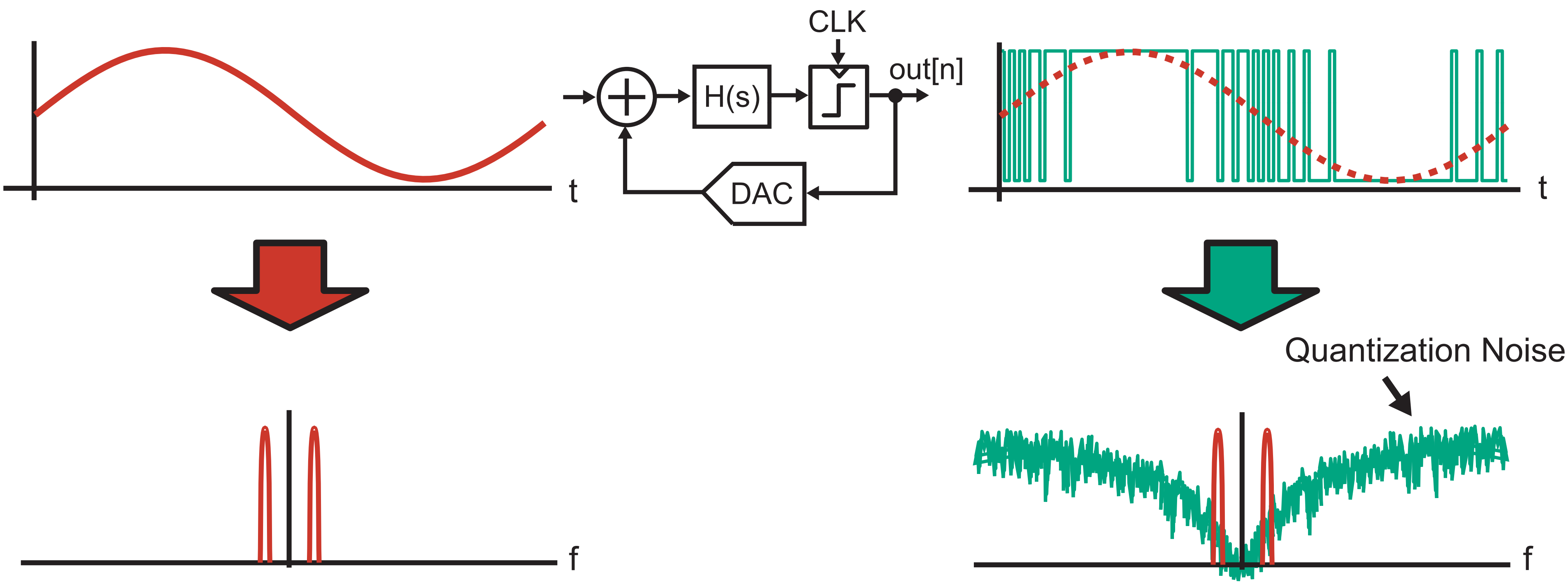
- **Continuous-time Sigma-Delta digitizes its input signal with the following characteristics:**
  - **Filters input waveform according to continuous-time filter design within A/D**
  - **Current from DAC keeps the voltage across C_{hold} at a constant value (along with a small amount of ripple)**
    - Keeps photodiode at a constant reverse-bias voltage

Review of Continuous-Time (CT) Sigma-Delta Operation



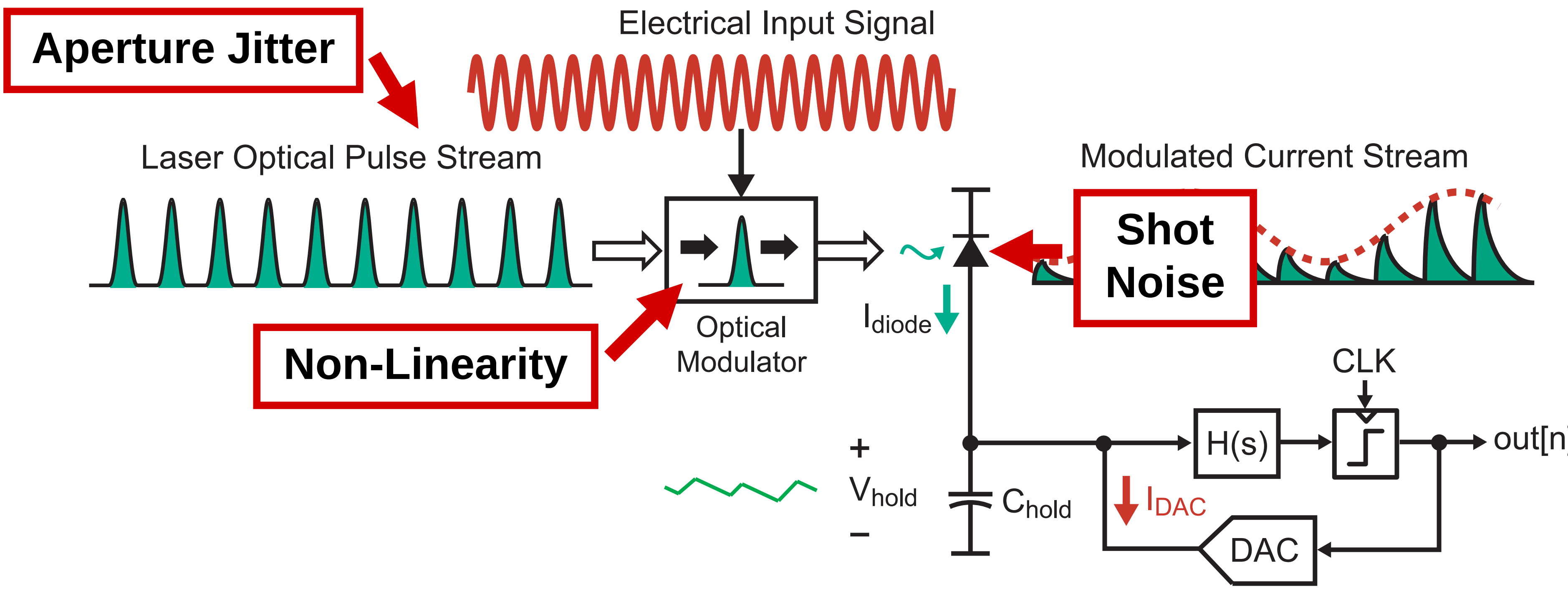
- **Key idea: dither a low resolution quantizer output such that its average tracks the A/D input**
  - **A/D output must be digitally filtered to extract desired signal**
  - **A/D must run at a very high oversampling ratio**
    - In our case: 1 GHz A/D sampling frequency for 2 MHz input signal bandwidth
      - Oversampling ratio in this case: 250
  - **Filter within A/D, H(s), must be designed for appropriate noise shaping and stable operation**

Frequency Domain View of CT Sigma-Delta A/D



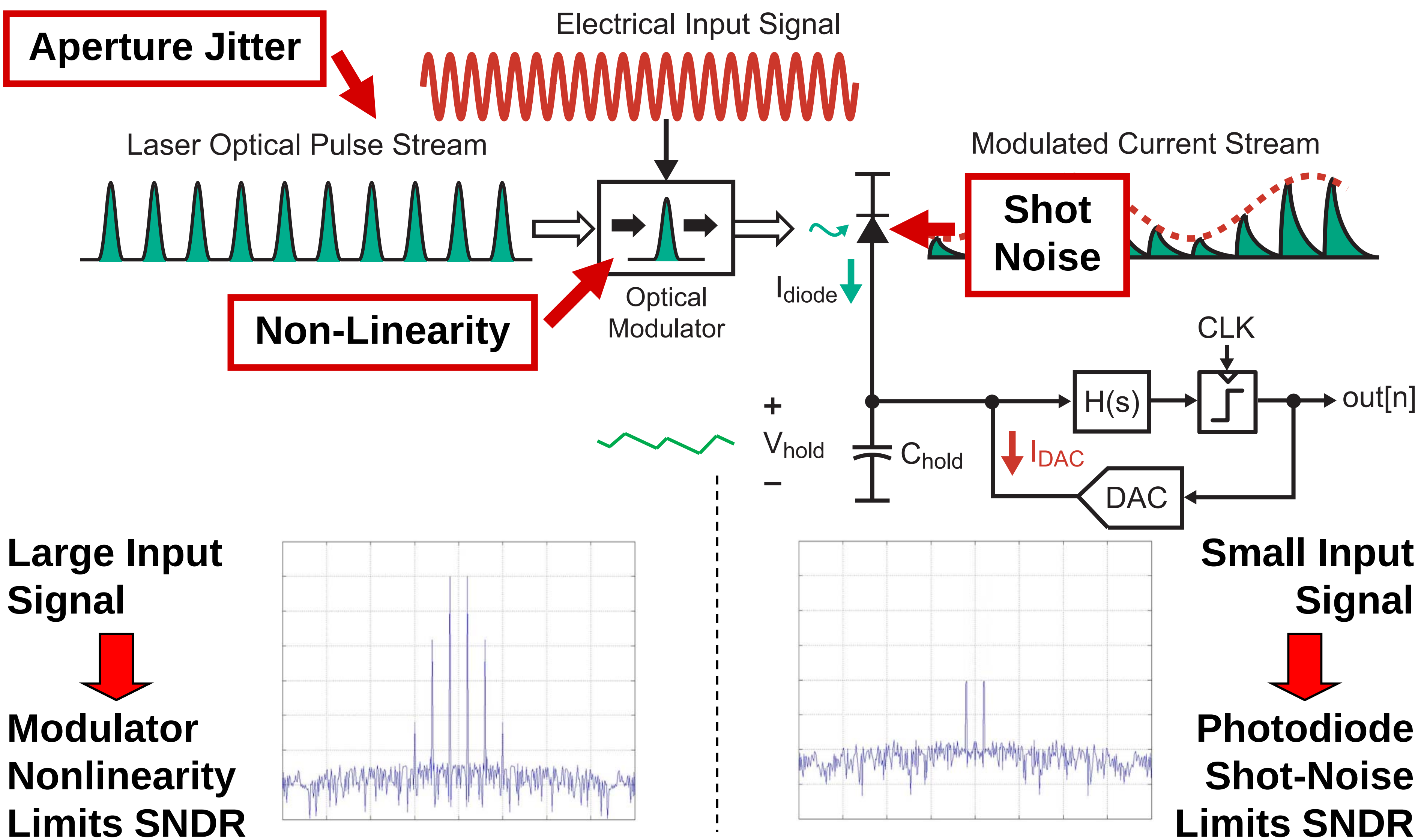
- **Sigma-Delta operation shapes quantization noise to high frequencies**
  - **Appropriate filtering of digitized output allows extraction of desired baseband signal with high SNR**

Theoretical Limitations of Architecture



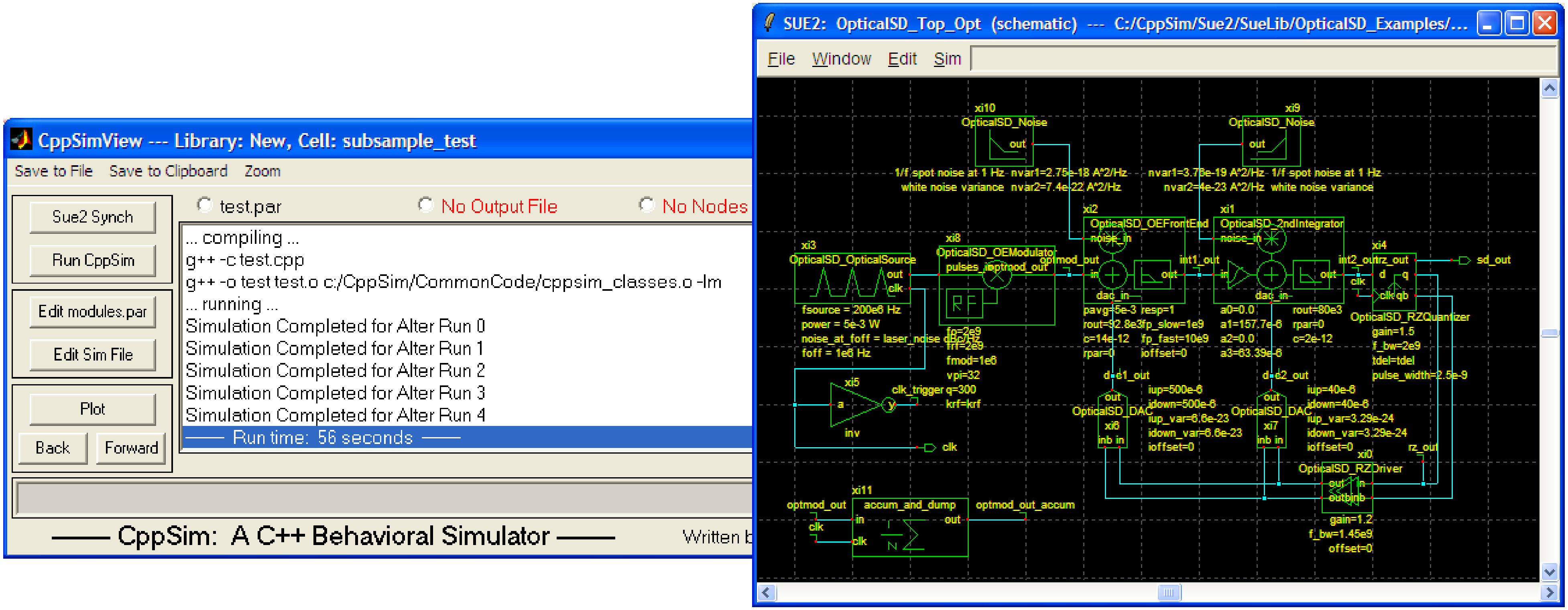
- **3 factors limit SNDR of receiver:**
  - **Laser aperture jitter**
  - **Modulator non-linearity**
  - **Photodiode shot-noise**
- **Aperture jitter set by laser, but photodiode power and signal amplitude are variable**
  - **What tradeoffs can we make to maximize SNDR?**

Theoretical Limitations of Architecture



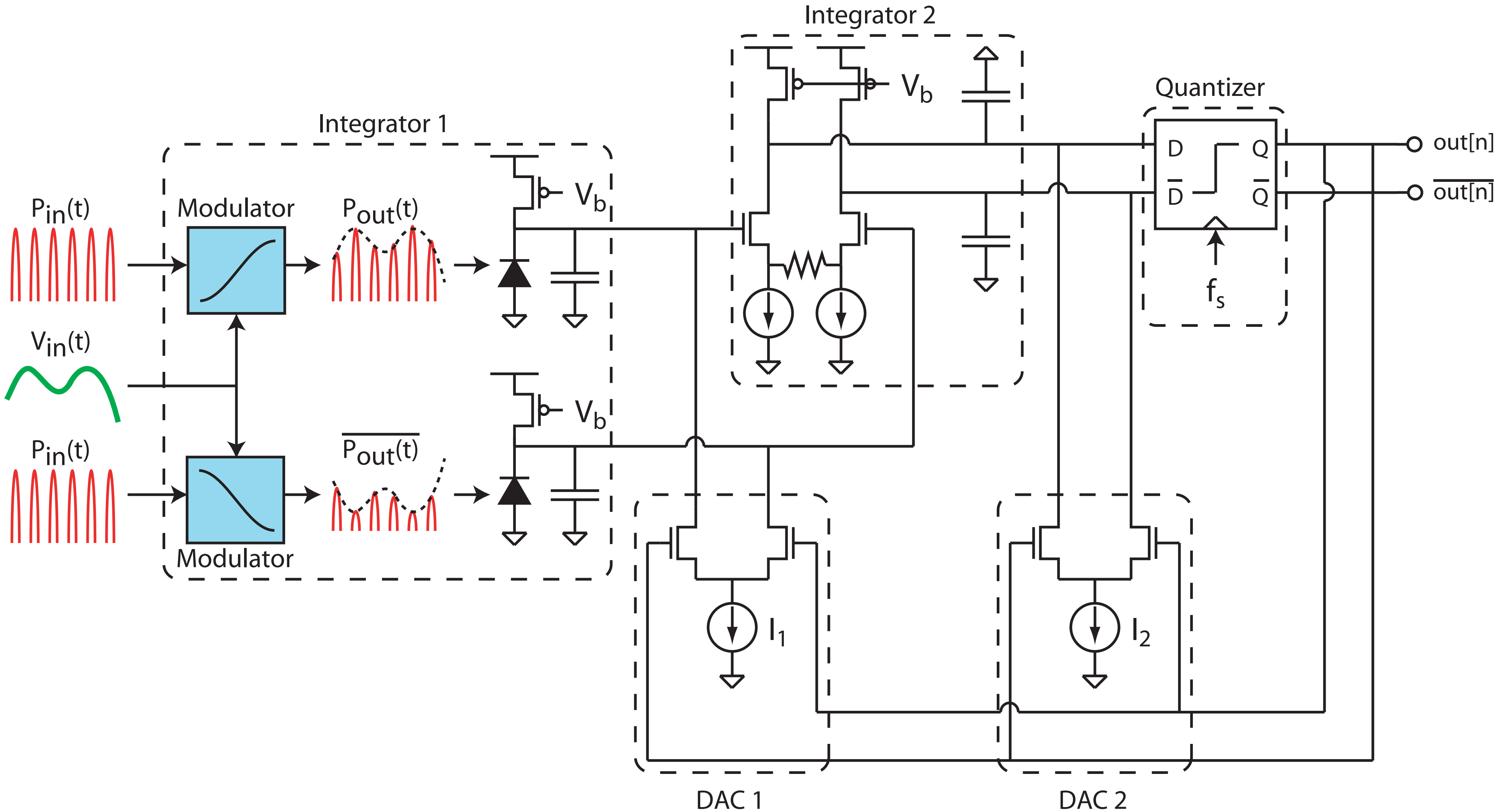
- **Optimal SNDR achieved by reducing signal power to lower distortion until comparable to shot noise floor**

Theoretical Performance of Architecture



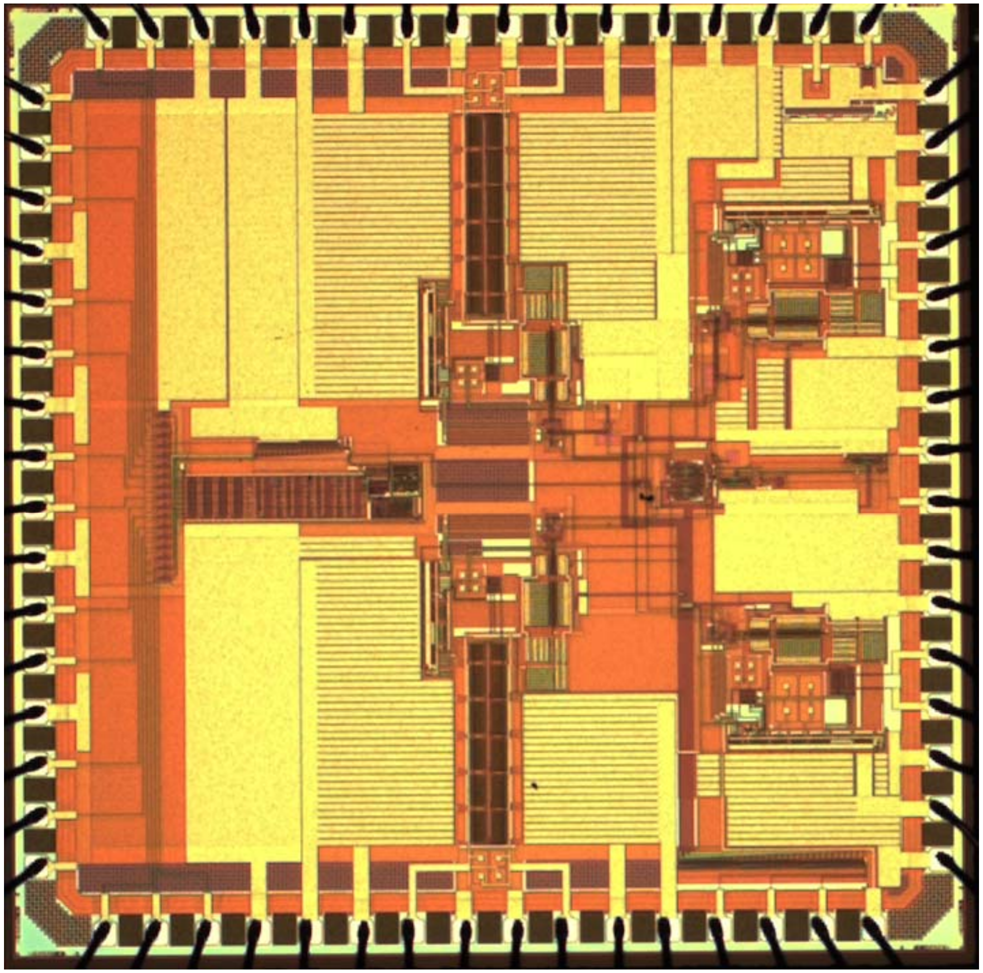
- **CppSim behavioral simulator used to determine overall theoretical performance of receiver/ADC**
  - **Model includes circuit noise, non-linearity, finite gain, loop delays, clock jitter, etc.**
  - **Tutorial can be downloaded online: http://www.cppsim.com**
- **Simulated SNDR ~ 57 dB in 2 MHz BW**

Custom ADC Implementation for Prototype



- Differential signaling used for robust operation
- Standard second-order Sigma-Delta topology used for its simplicity and robustness

Custom ADC IC



- Technology: 0.18 um CMOS
- Area: 3mm x 3mm (pad-limited)
- Precision: ~ 12 bit at 1 MHz BW, OSR = 390
- Power: ~ 50 mW
- Fabricated by National Semiconductor
- Funded by EPIC program DARPA W911NF-04-1-0431

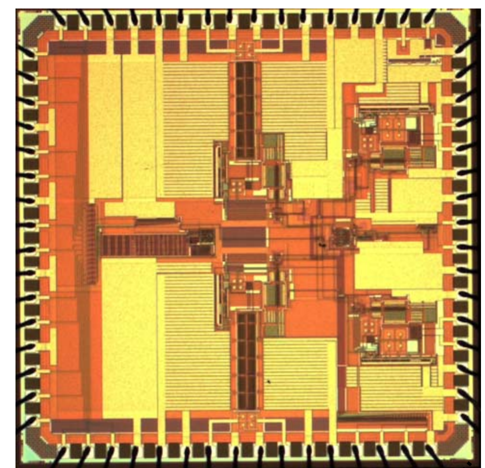
Designed by Matt Park

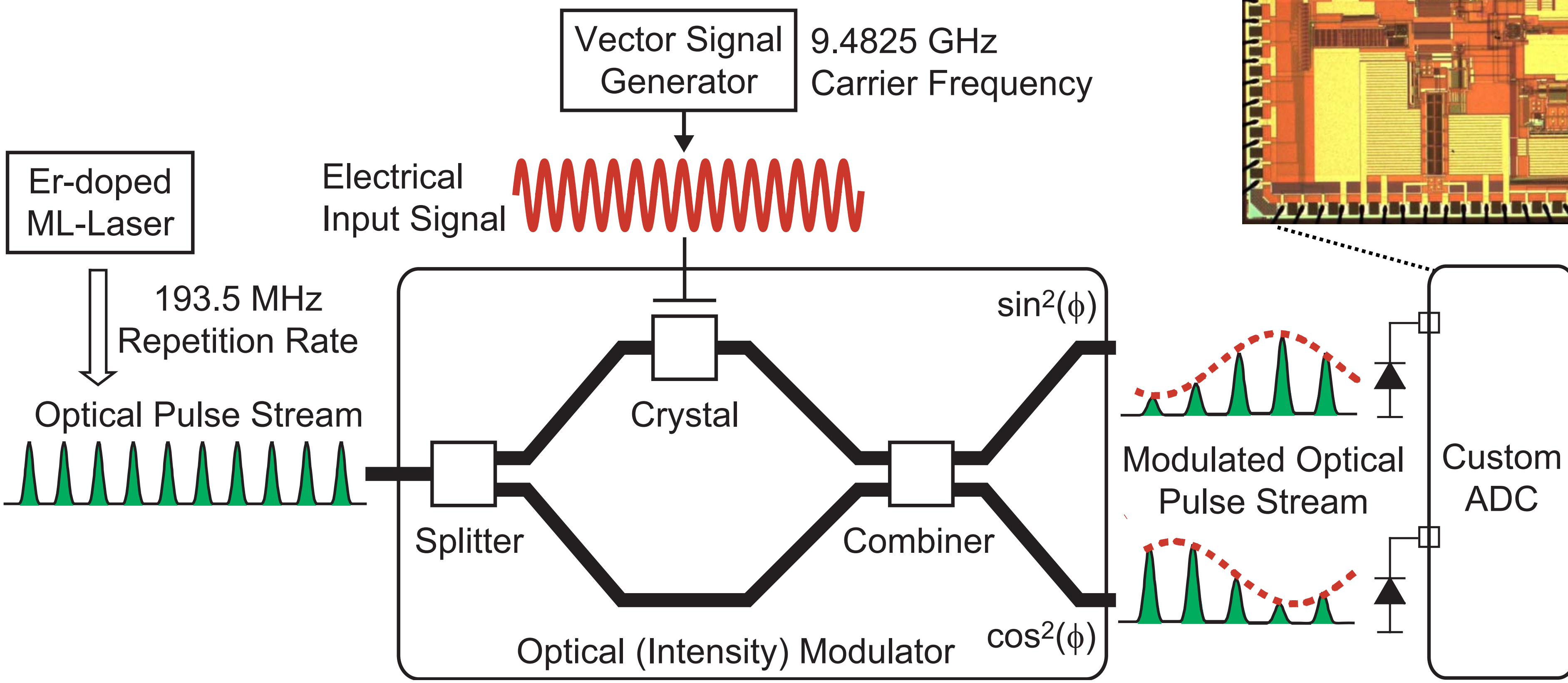
Overall optical/electrical prototype developed in collaboration with Jung-Won Kim and Prof. Franz Kaertner (MIT)

Overall Downconversion/Digitization Prototype

- **Optical portion is fiber-based**
- **Electrical input carrier frequency is 9.48 GHz with 1 Mbit/s GMSK modulation**
- **Repetition Rate of Mode-Locked Laser is 193.5 MHz**

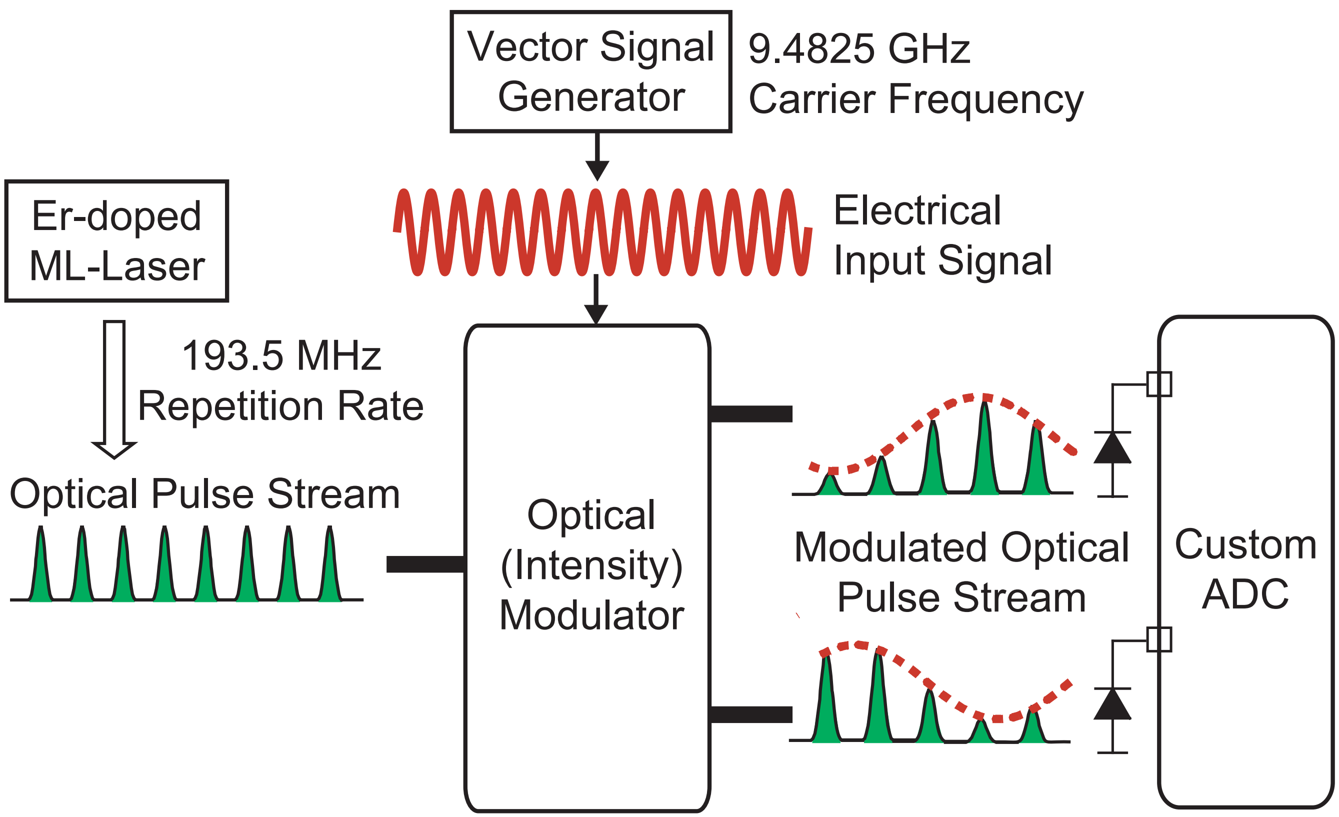
Custom Σ–Δ ADC Integrated Circuit



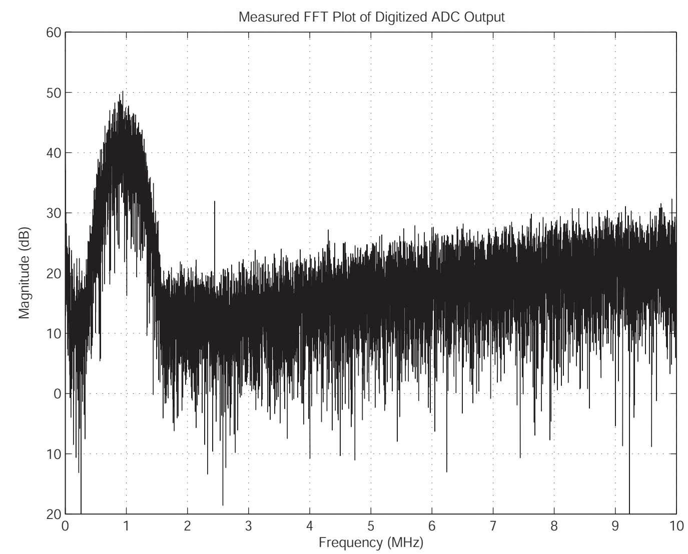


Measured Results

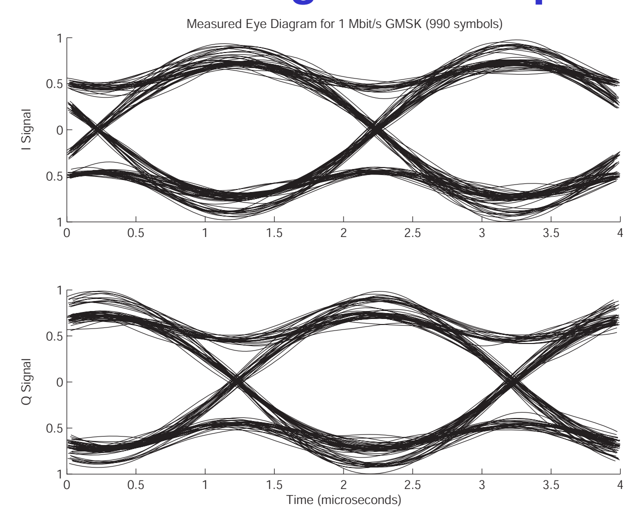
- **Clean eye diagrams obtained with 1 Mbit/s modulation at 9.48 GHz carrier frequency**
  - **Peak SNDR: 22 dB (2 MHz BW)**
  - **Peak SNR: 32 dB (2 MHz BW)**



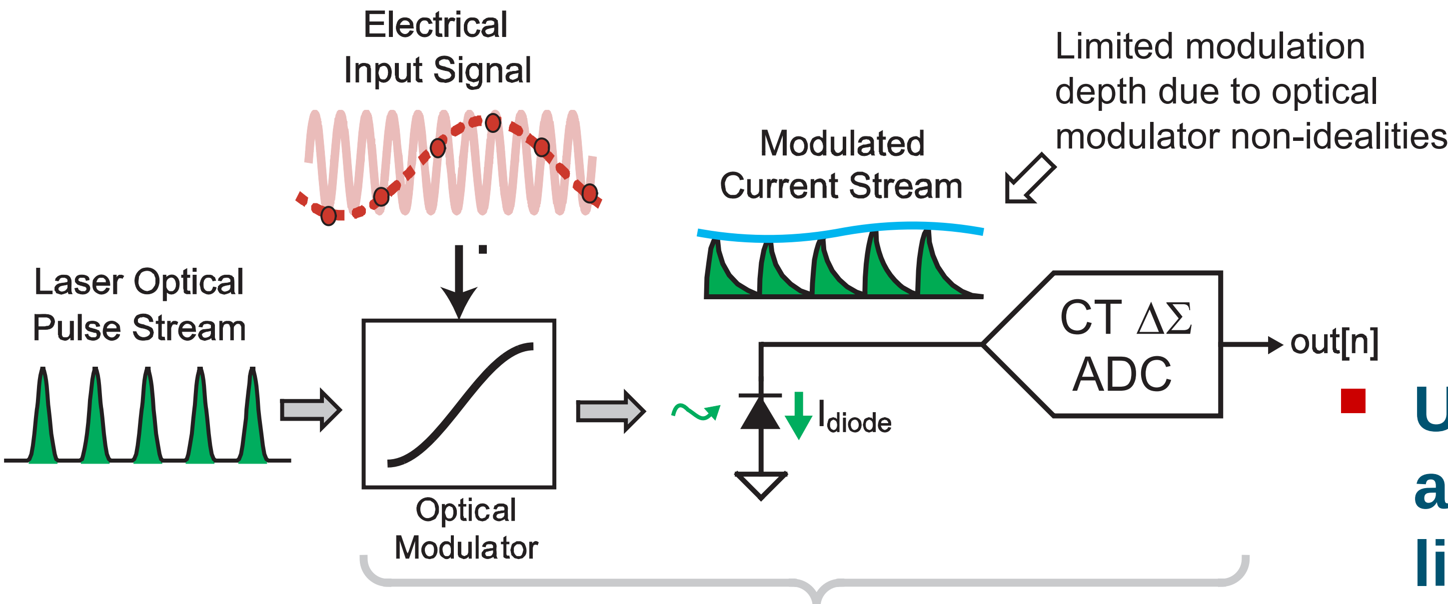
FFT of Digitized Output



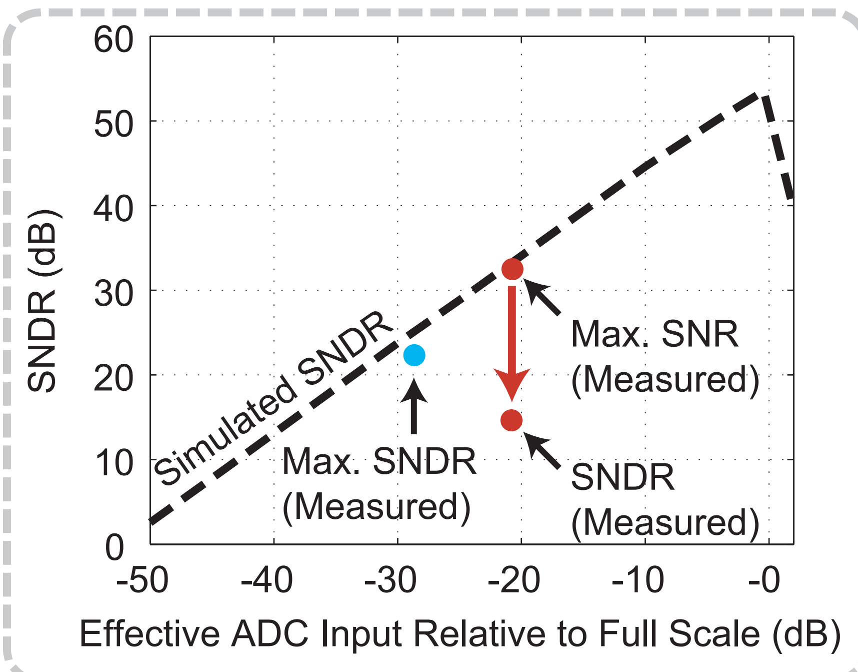
Recovered Eye Diagram From Digitized Output



Key Bottleneck – Nonlinearity and Loss in Optical Path

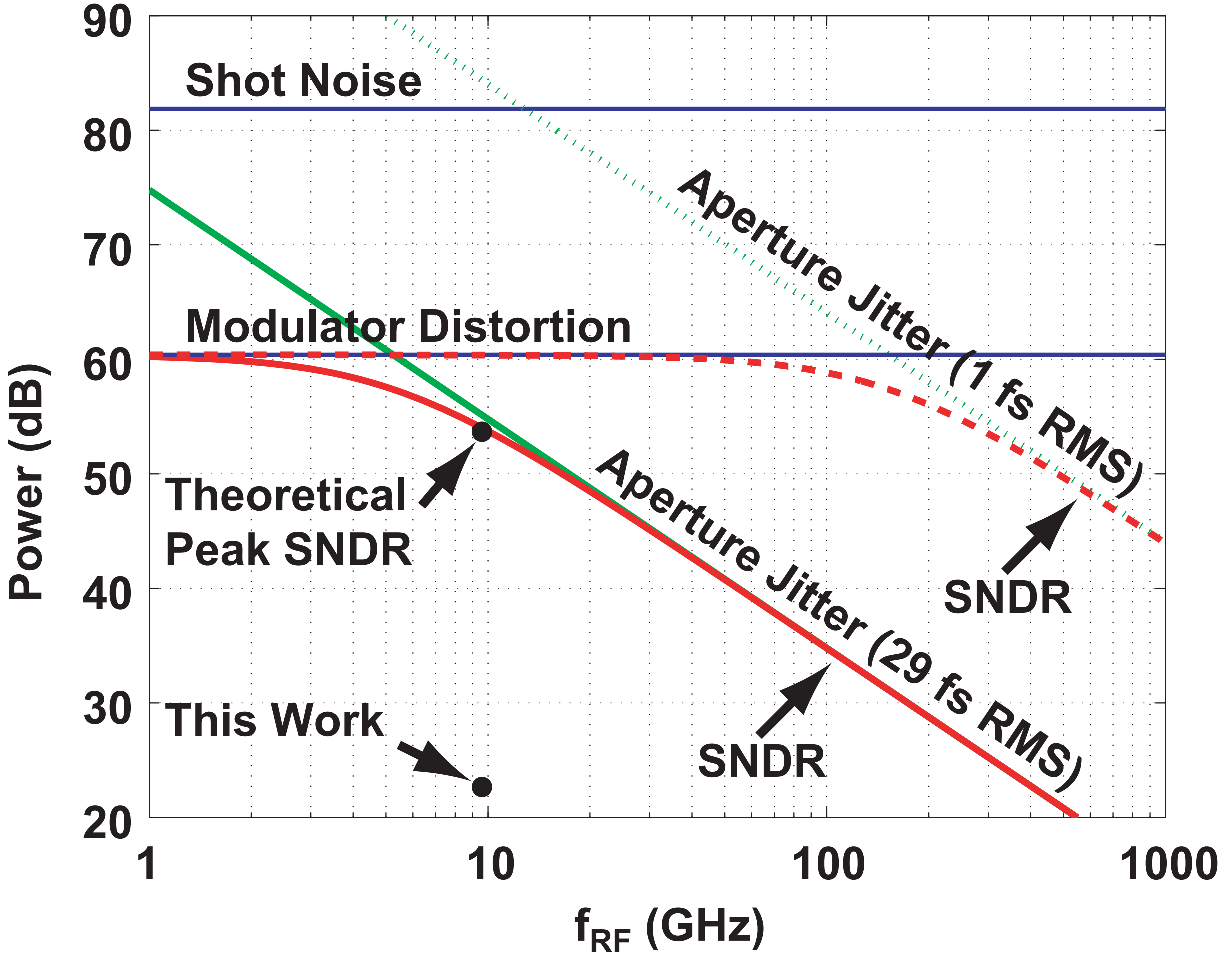


Measured SNDR of entire system vs. effective ADC input amplitude



- **Unexpected loss and nonlinearity limited the achievable swing into the ADC**
- **Better modulator and improved current carrying ability of photodiodes should improve performance**

Analysis of Achievable Performance



- **Next goal: demonstrate system at higher carrier frequency**
  - **Aperture jitter of laser will limit achievable performance**
  - **42 dB SNDR (2 MHz BW) should be achievable at 40 GHz**

Conclusions

- **Optical components have the following benefits for phase-locked loops, sampling, and downconversion:**
  - **Mode-locked lasers provide extremely low jitter pulse sequences**
  - **Optical channels provide extremely high bandwidth**
  - **Optical components allow extremely fast memoryless processing of signals (such as multiplication)**
- **We demonstrated the following**
  - **Low jitter phase-locked loop which leverages optical pulses as input and optical/electronic phase detection**
  - **Optical/electrical downconversion and digitization based on optical sampling and electronic filtering**

Many more exciting opportunities will arise as we obtain higher integration levels for optical components