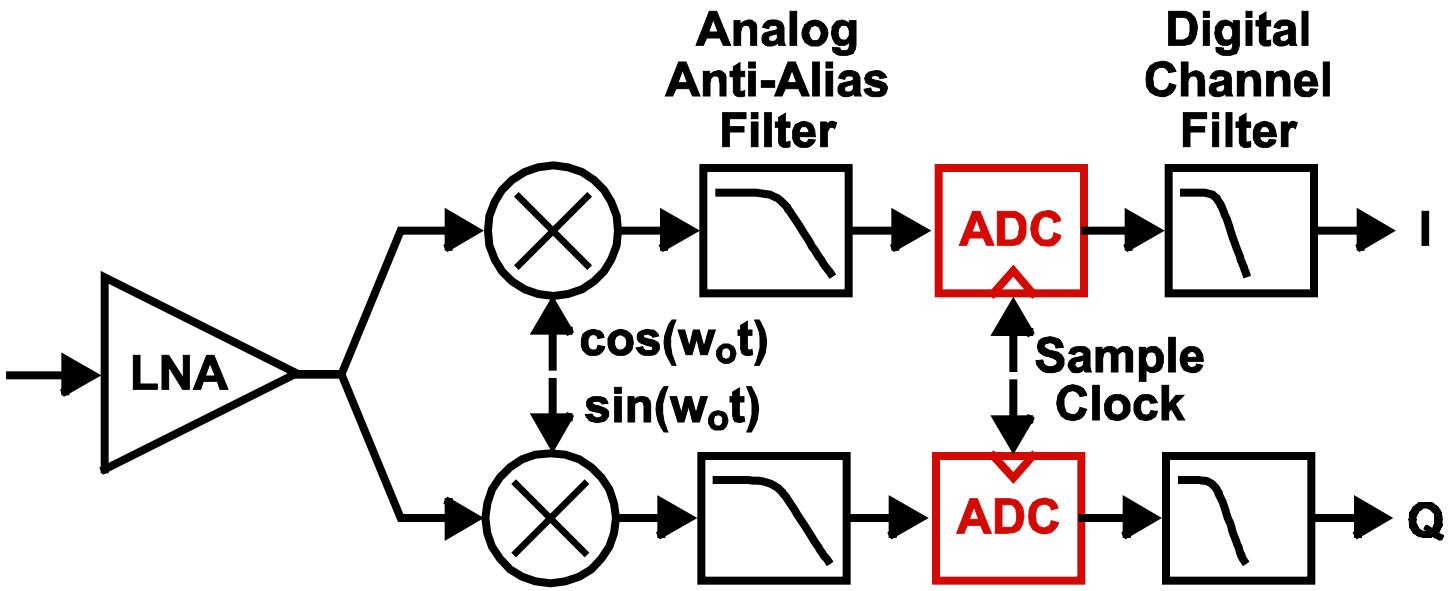
VCO-Based Wideband Continuous-Time Sigma-Delta Analog-to-Digital Converters

AACD 2010

Michael H. Perrott

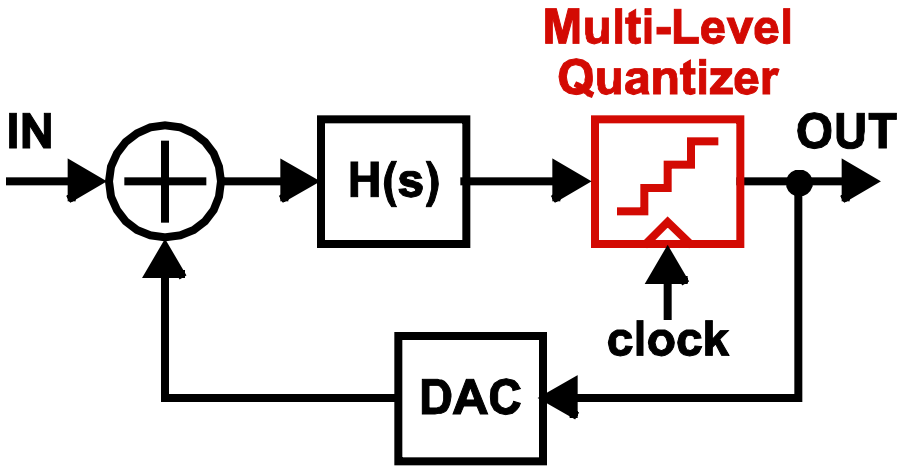
Motivation



- A highly digital receive path is very attractive for achieving multi-standard functionality
- A key issue is achieving a wide bandwidth ADC with high resolution and low power
  - Minimal anti-alias requirements are desirable for simplicity

Continuous-Time Sigma-Delta ADC structures have very attractive characteristics for this space

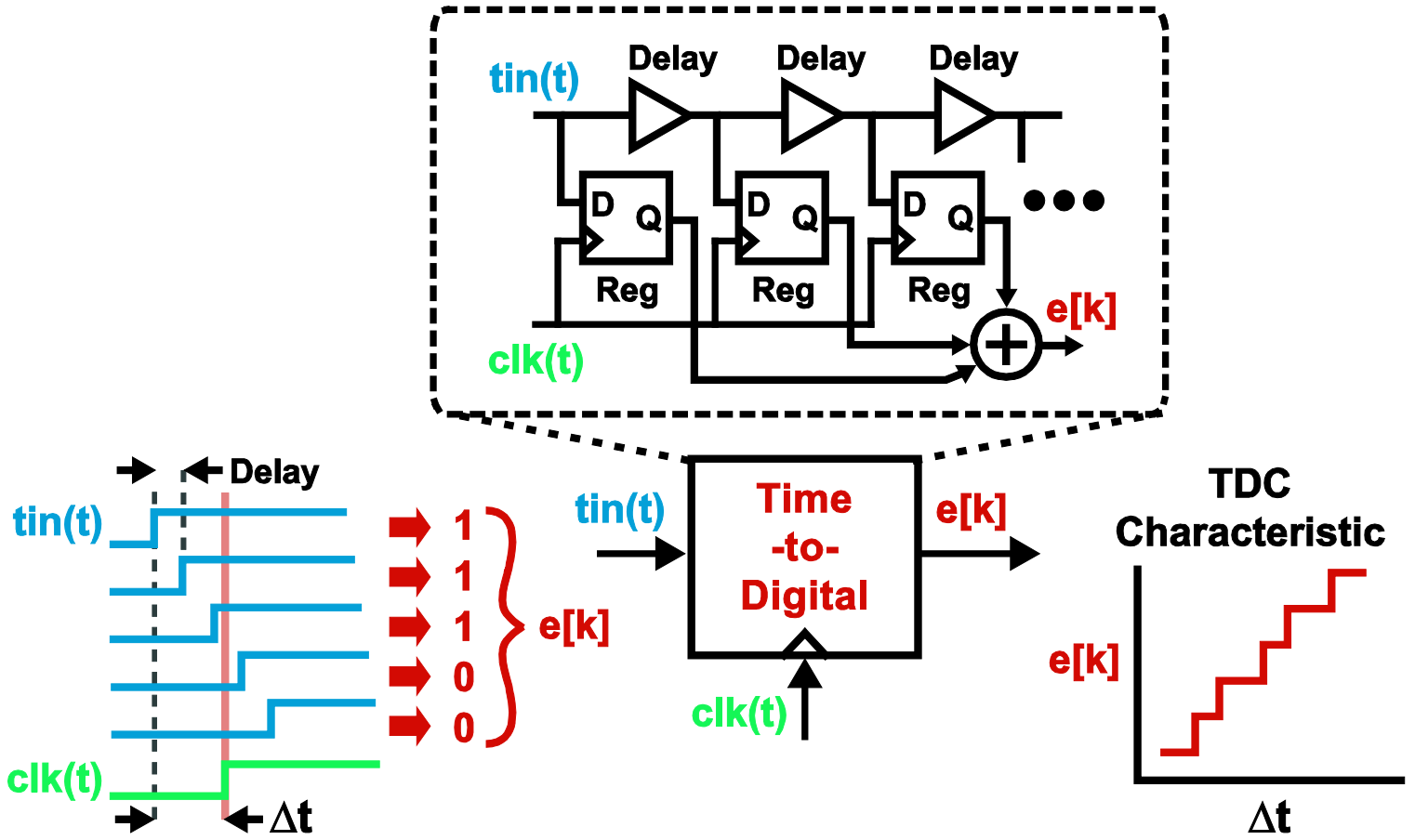
A Basic Continuous-Time Sigma-Delta ADC Structure



- Sampling occurs at the quantizer *after* filtering by *H(s)*
- Quantizer noise is shaped according to choice of *H(s)*
  - High open loop gain required to achieve high SNR

We will focus on achieving an efficient implementation of the multi-level quantizer by using a ring oscillator

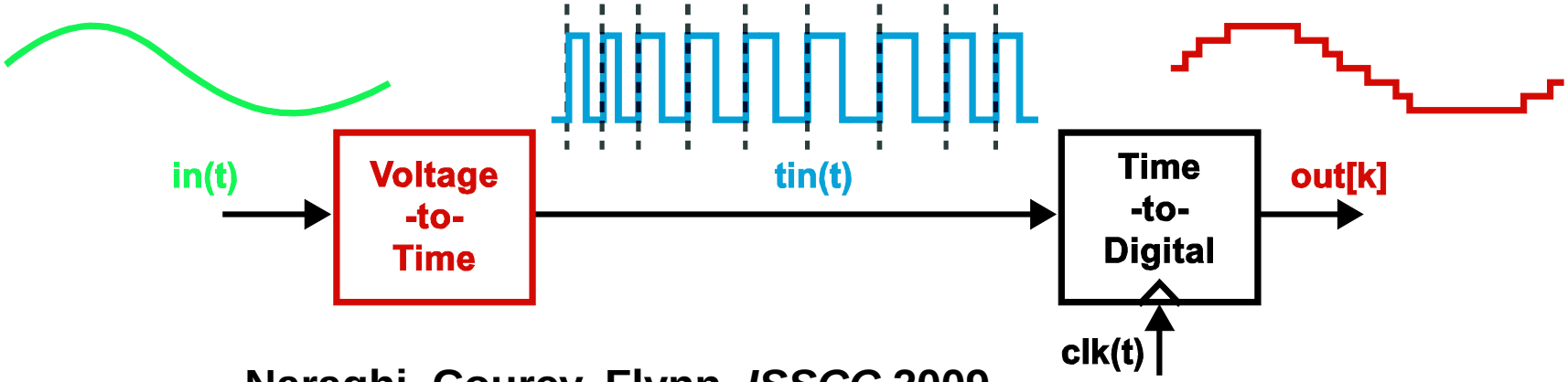
Consider Time-to-Digital Conversion



- Quantization in time achieved with purely digital gates
  - Easy implementation, resolution improving with Moore's law

How can we leverage this for quantizing an analog voltage?

Adding Voltage-to-Time Conversion

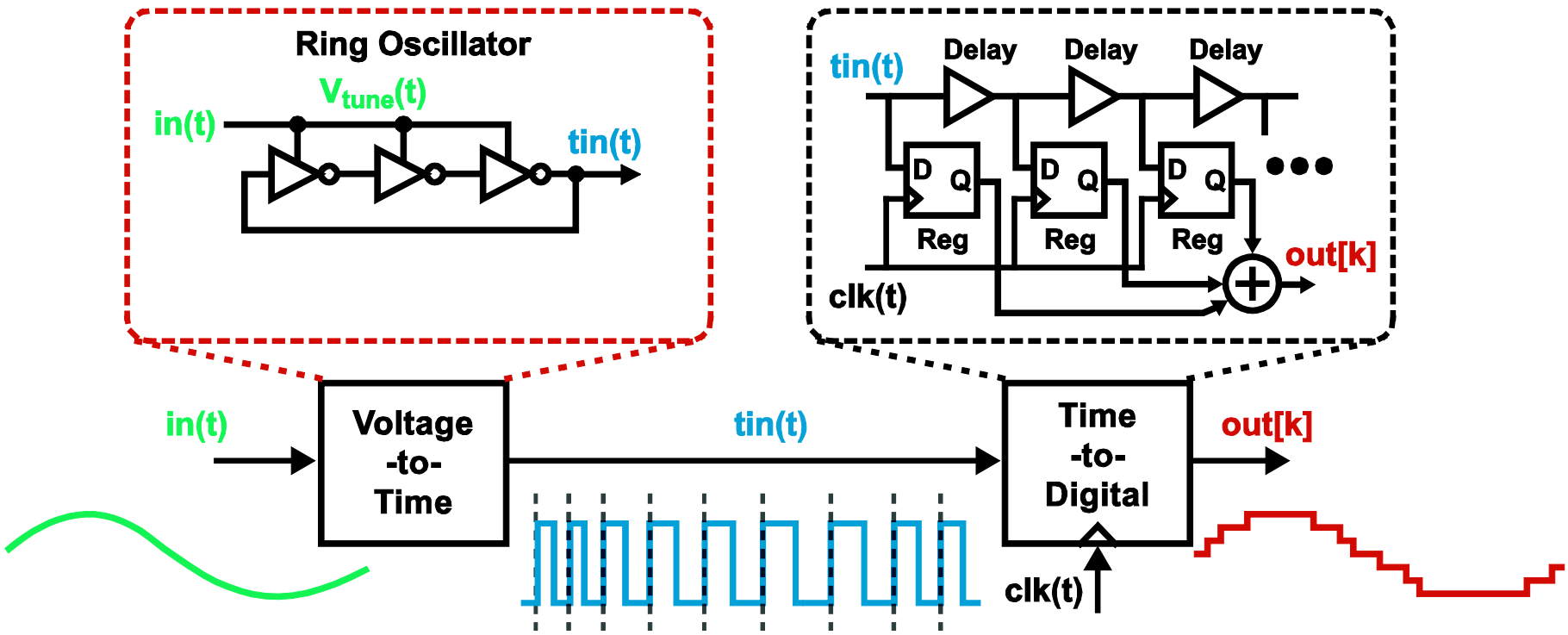


Naraghi, Courcy, Flynn, *ISSCC* 2009

- Analog voltage is converted into edge times
  - Time-to-digital converter then turns the edge times into digitized values
- Key issues
  - Non-uniform sampling
  - Noise, nonlinearity

Is there a simple implementation for the Voltage-to-Time Converter?

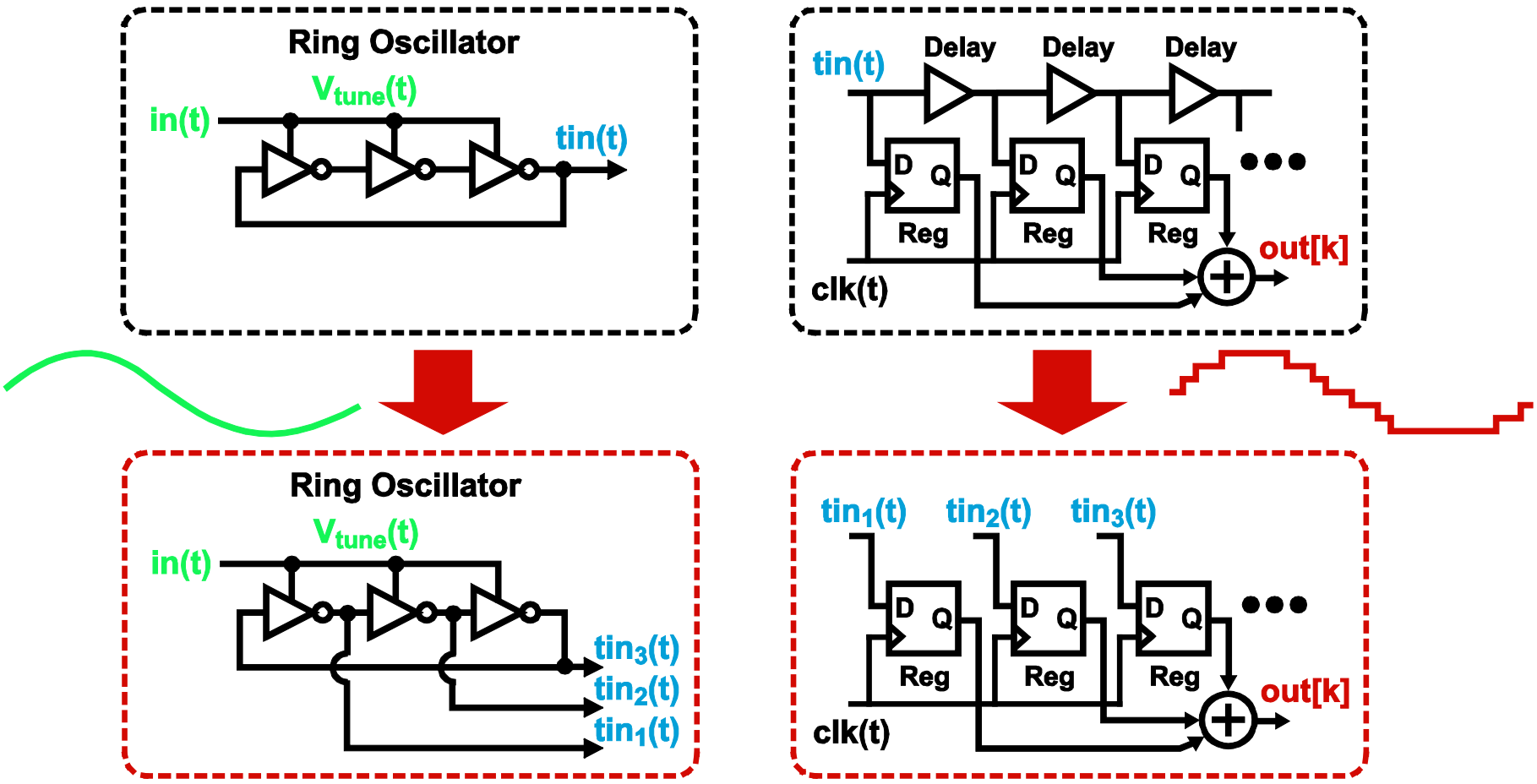
A Highly Digital Implementation



- A voltage-controlled ring oscillator offers a simple voltage-to-time structure
  - Non-uniform sampling is still an issue

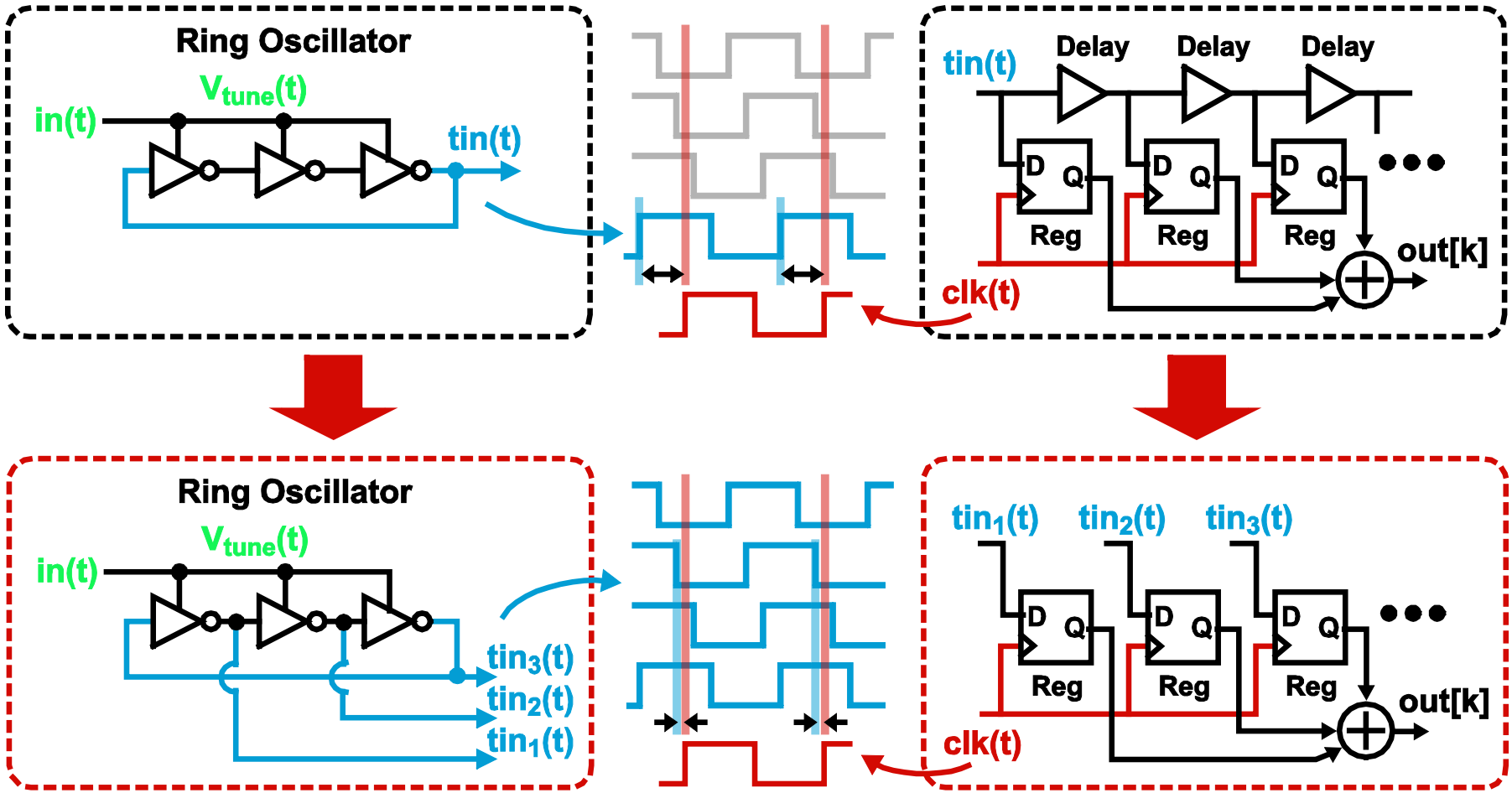
We can further simplify this implementation and lower the impact of non-uniform sampling

Making Use of the Ring Oscillator Delay Cells



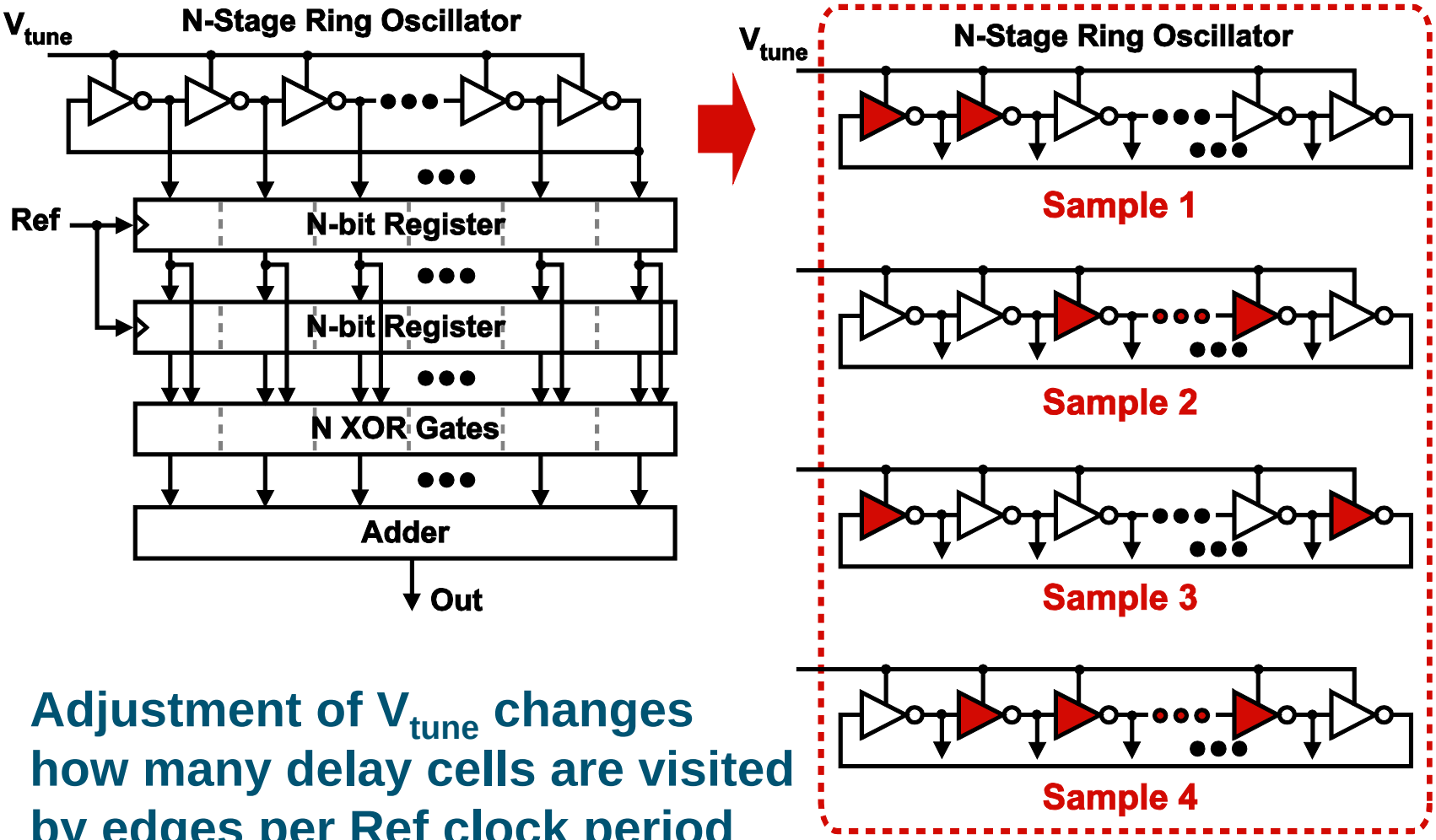
- Utilize all ring oscillator outputs and remove TDC delays
  - Simpler implementation
- TDC output now samples/quantizes phase state of oscillator

Improving Non-Uniform Sampling Behavior



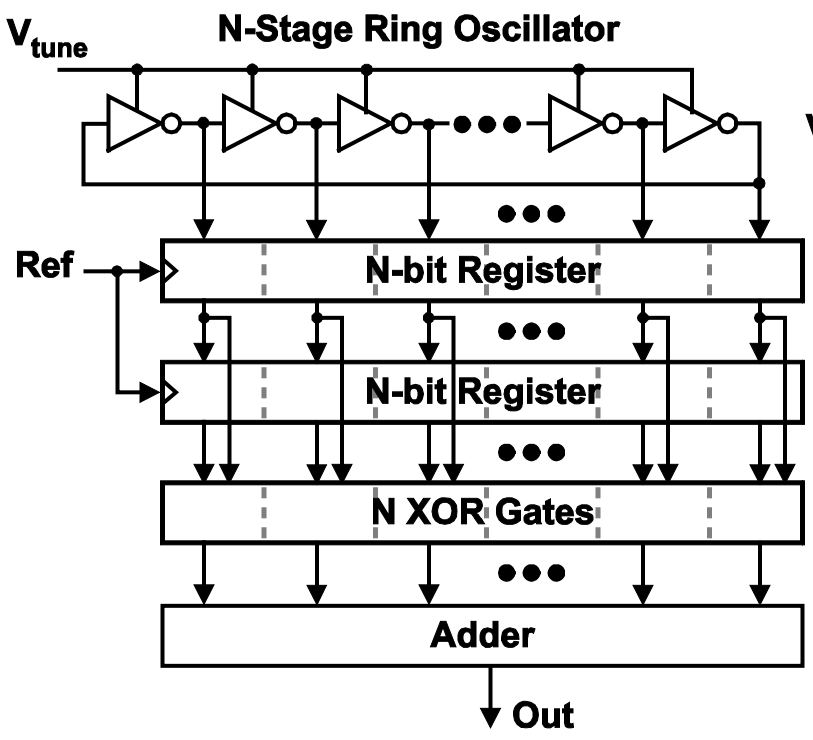
- Oscillator edges correspond to a sample window of the input
- Sampling the oscillator phase state yields sample windows that are much more closely aligned to the TDC clk

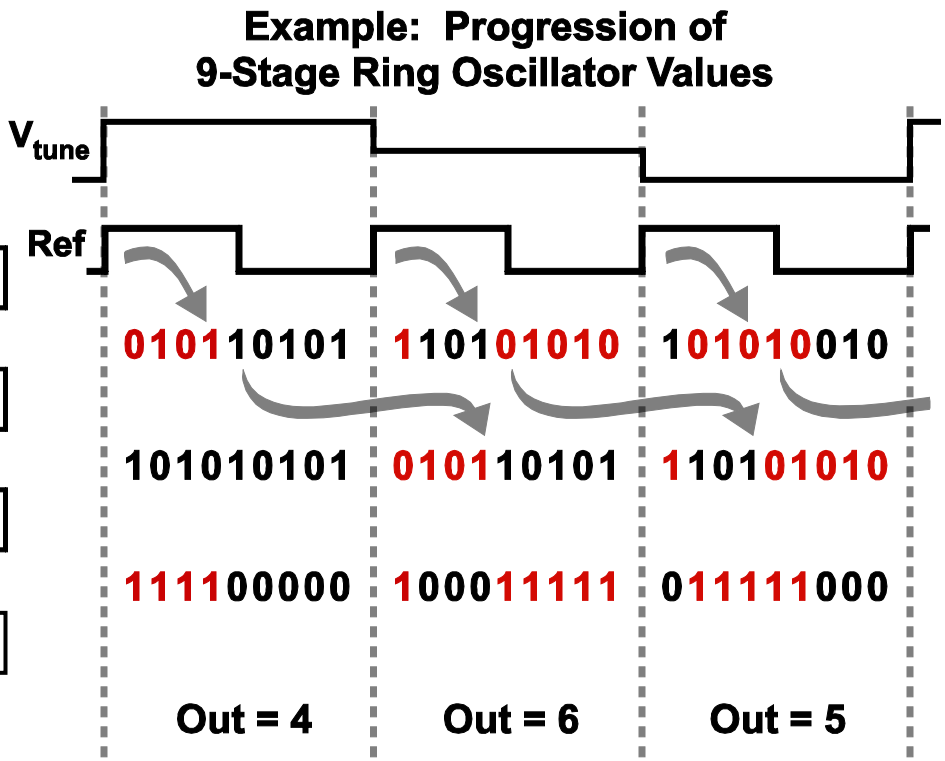
Multi-Phase Ring Oscillator Based Quantizer



- Adjustment of V_{tune} changes how many delay cells are visited by edges per Ref clock period
  - Quantizer output corresponds to the number of delay cells that experience a transition in a given Ref clock period

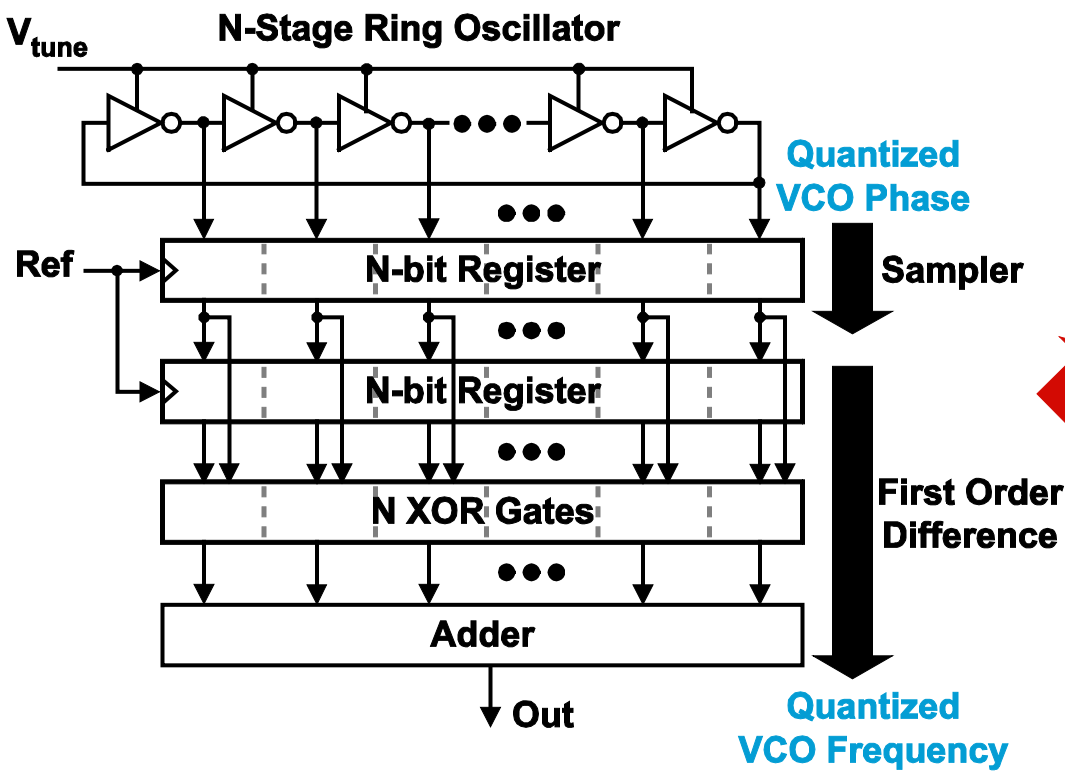
More Details …

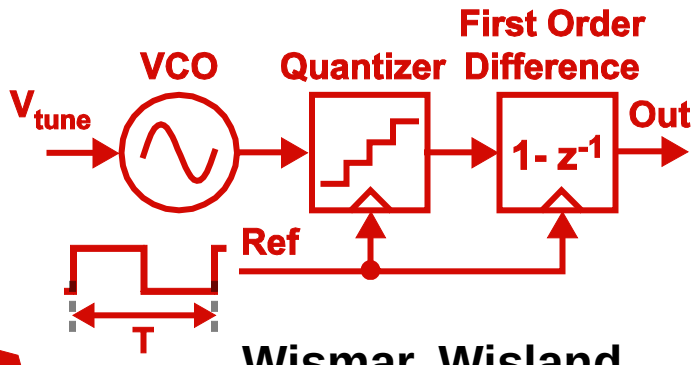




- Choose large enough number of stages, *N*, such that transitions never cycle through a given stage more than once per Ref clock period
  - Assume a high Ref clock frequency (i.e., 1 GHz)
- XOR operation on current and previous samples provides transition count

A First Step Toward Modeling





Wismar, Wisland, Andreani, ESSCIRC 2006

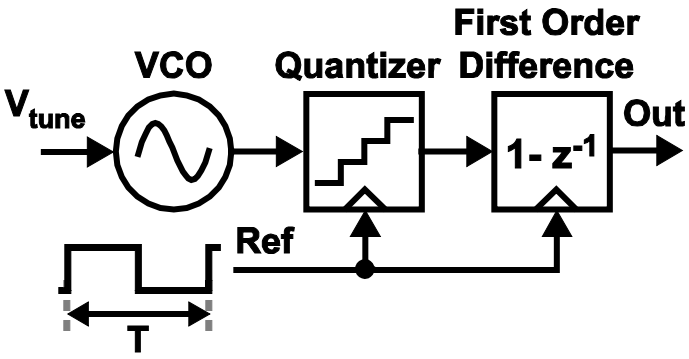
1000**11111** 0**11111**000

Out = 6 Out = 5

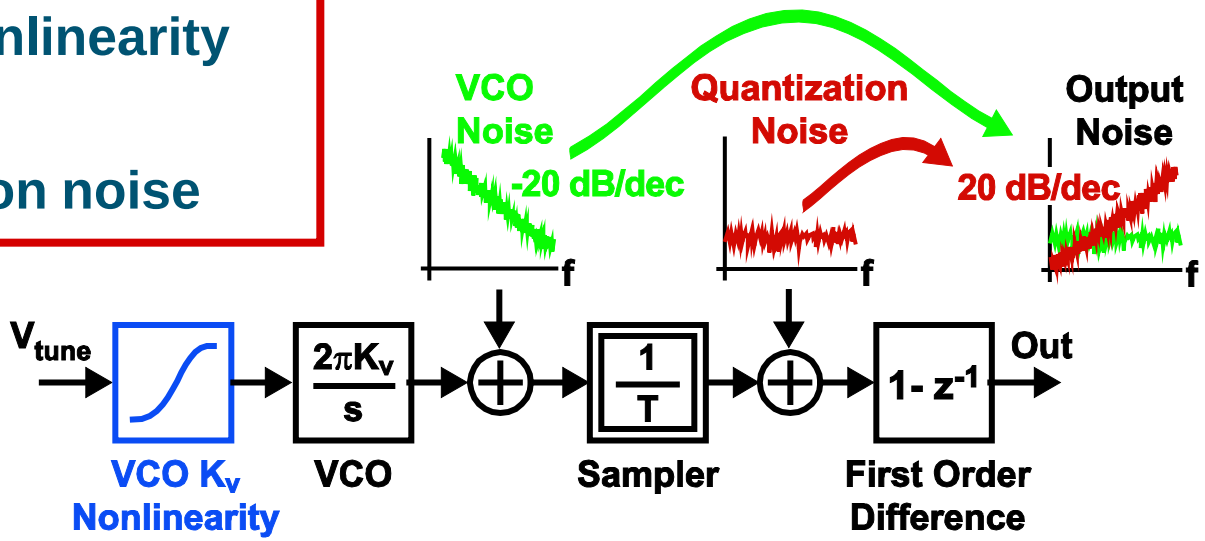
- VCO provides quantization, register provides sampling
  - Model as separate blocks for convenience
- XOR operation on current and previous samples corresponds to a first order difference operation
  - Extracts VCO frequency from the sampled VCO phase signal

Corresponding Frequency Domain Model

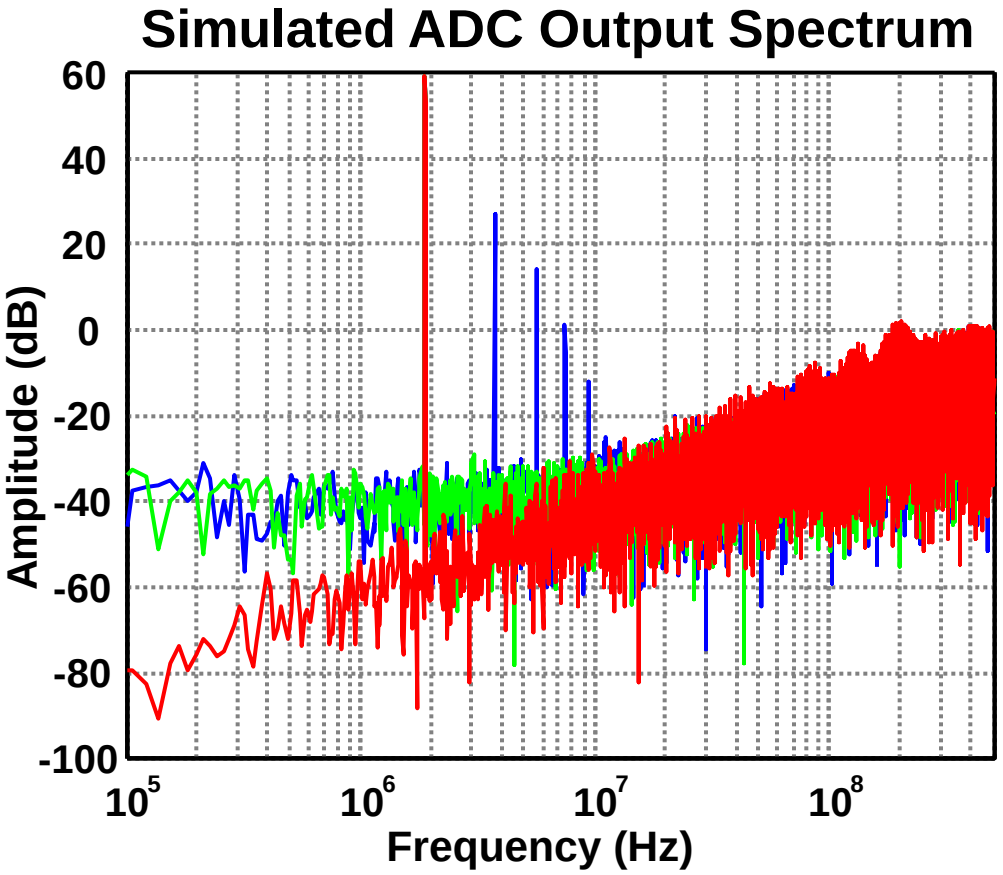
- VCO modeled as integrator and K_v nonlinearity
- Sampling of VCO phase modeled as scale factor of 1/T
- Quantizer modeled as addition of quantization noise



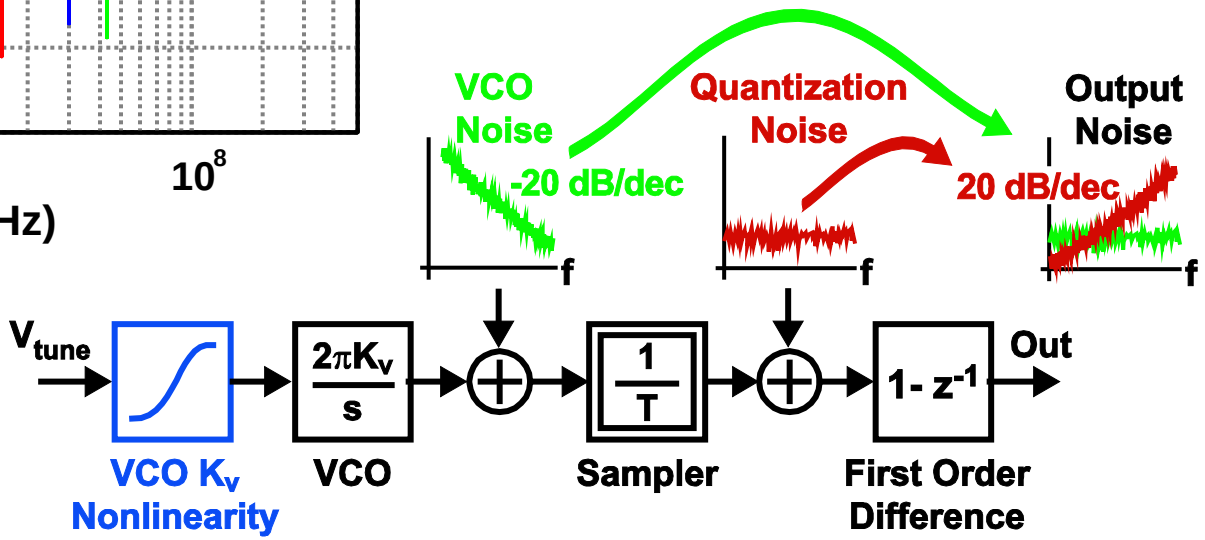
- Key non-idealities:
  - VCO K_v nonlinearity
  - VCO noise
  - Quantization noise



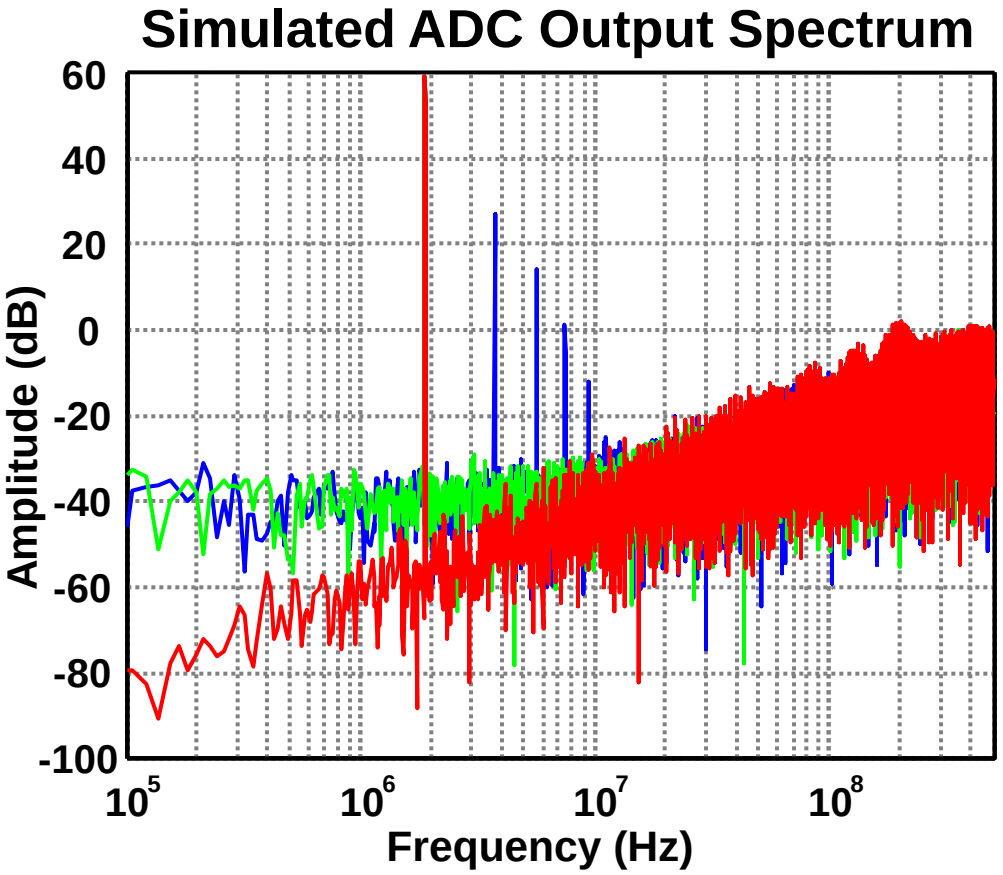
Example Design Point for Illustration



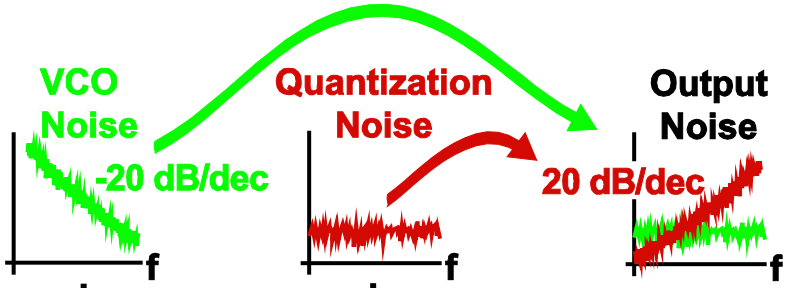
- Ref clk: 1/T = 1 GHz
- 31 stage ring oscillator
  - Nominal delay per stage: 65 ps
- K_{VCO} = 500 MHz/V
  - ±5% linearity
- VCO noise: -100 dBc/Hz at 10 MHz offset



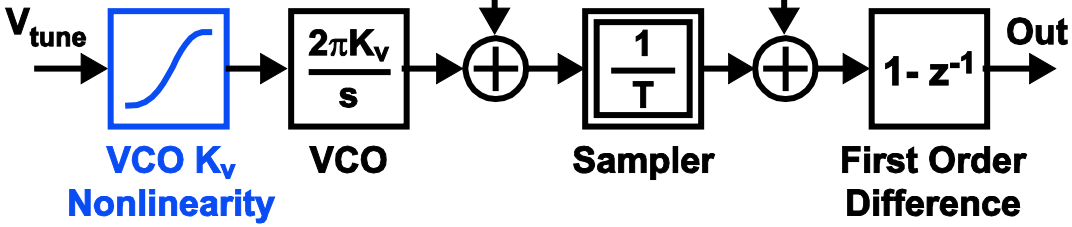
SNR/SNDR Calculations with 20 MHz Bandwidth



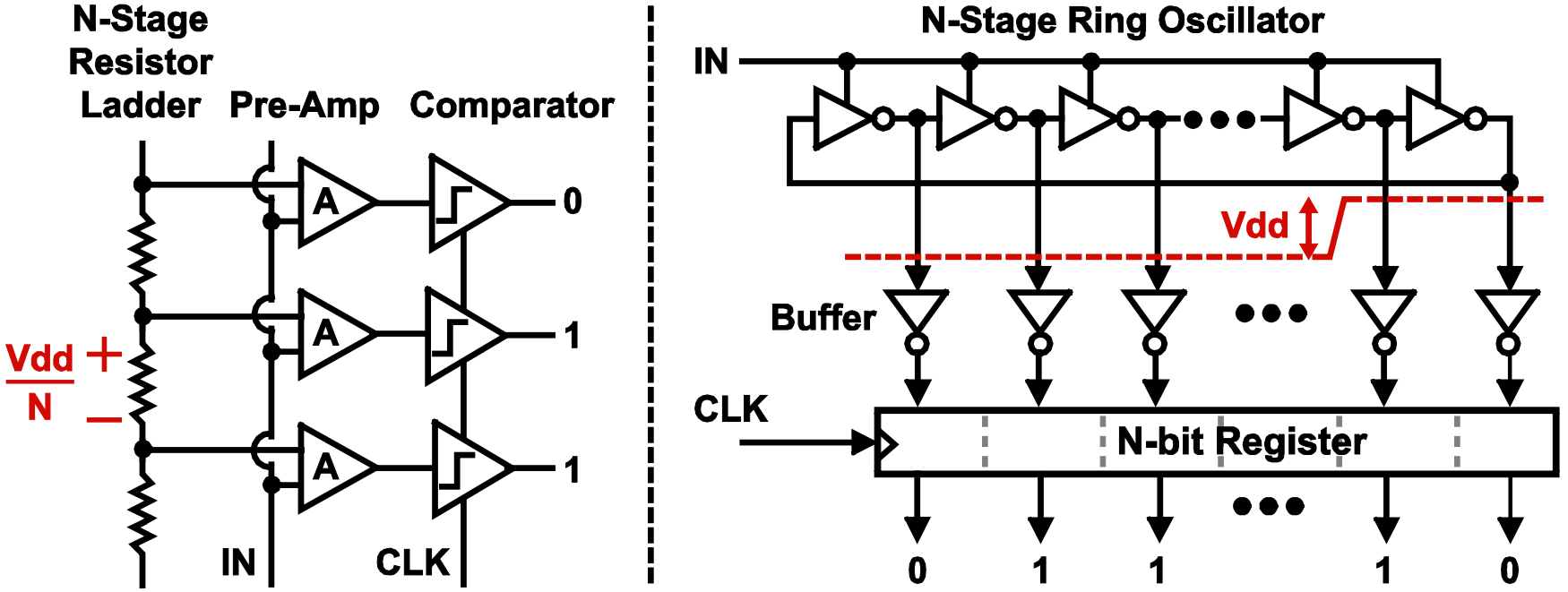
Conditions	SNDR
Ideal	68.2 dB
VCO Thermal Noise	65.4 dB
VCO Thermal + Nonlinearity	32.2 dB



VCO K_v nonlinearity is the key performance bottleneck



Classical Analog Versus VCO-based Quantization

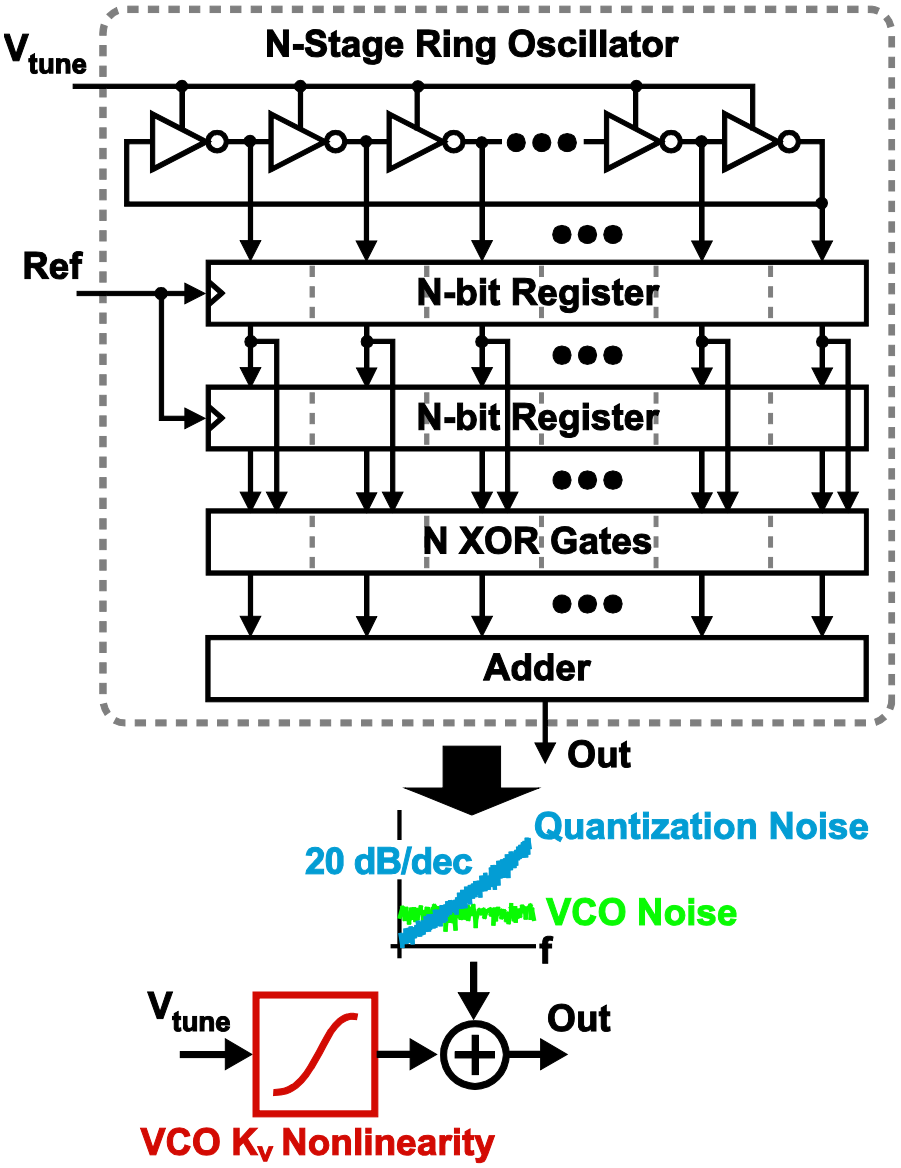


- Much more digital implementation
- Offset and mismatch is not of critical concern
- Metastability behavior is potentially improved
- Improved SNR due to quantization noise shaping

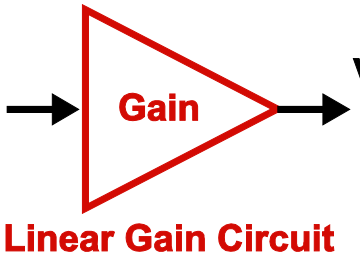
Implementation is high speed, low power, low area

Key Performance Issues: Nonlinearity and Noise

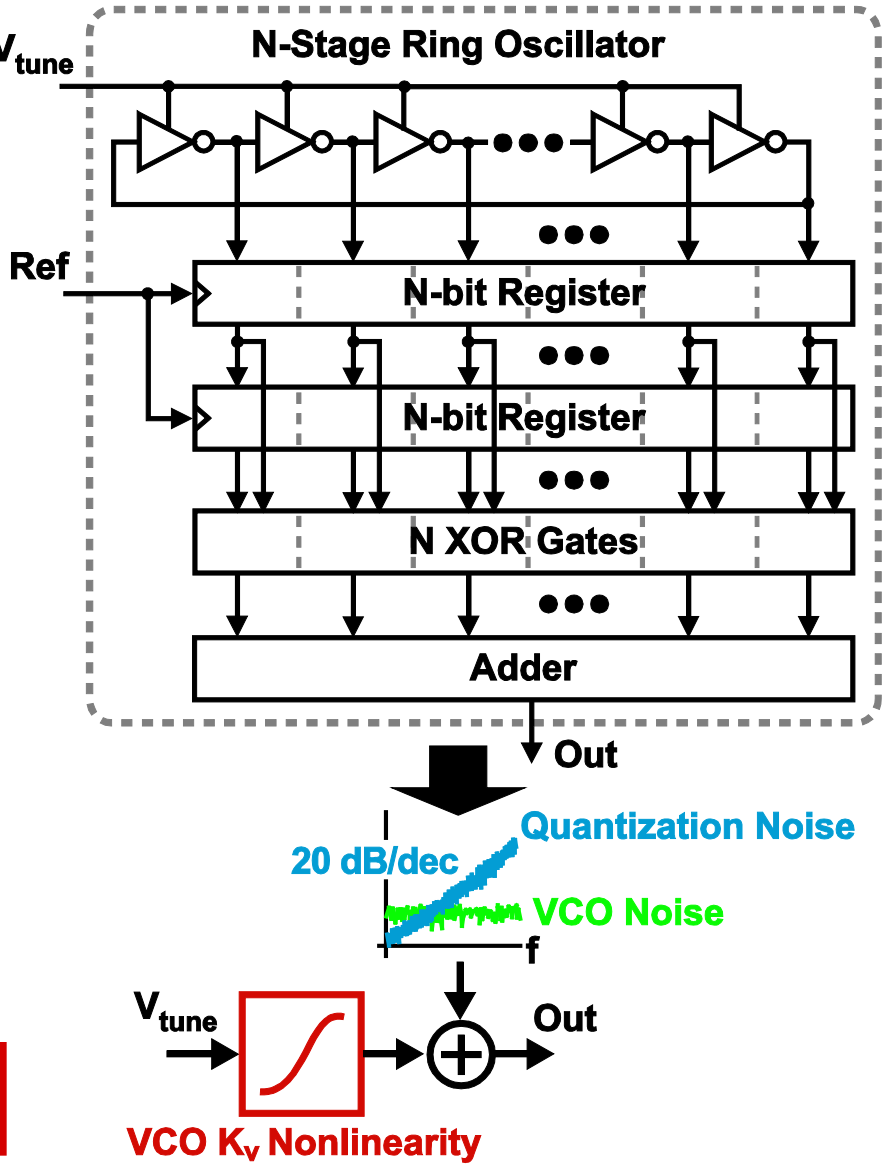
- **Very hard to build a simple ring oscillator with linear K_v**
- **Noise floor set by VCO phase noise is typically higher than for analog amplifiers at same power dissipation**



What Can Analog Bring to the Table?



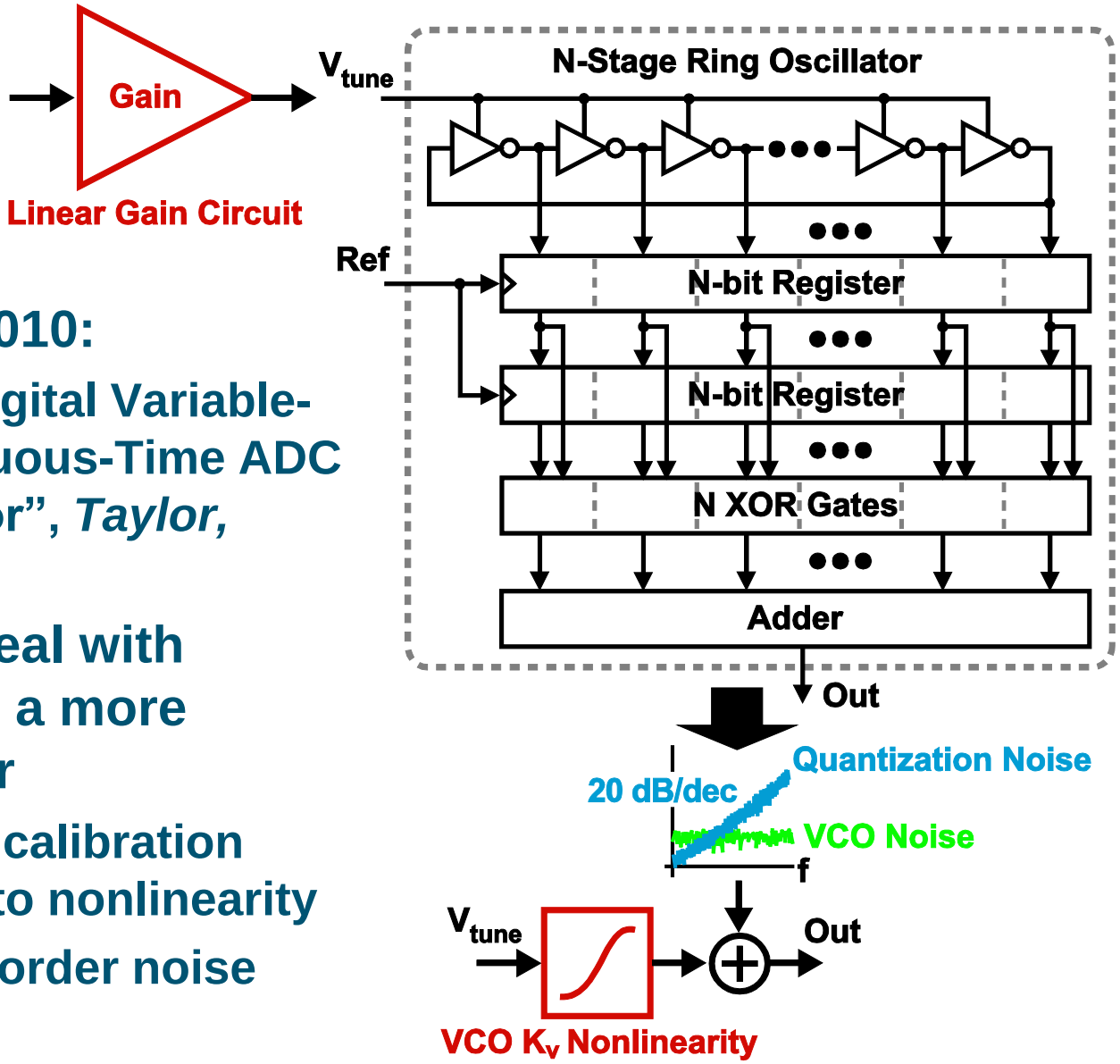
Linear Gain Circuit



- We know how to build fairly linear gain blocks with relatively low noise
  - For this simple function, analog offers relatively high speed, low area, low power
- Analog gain can reduce impact of noise in blocks that follow it

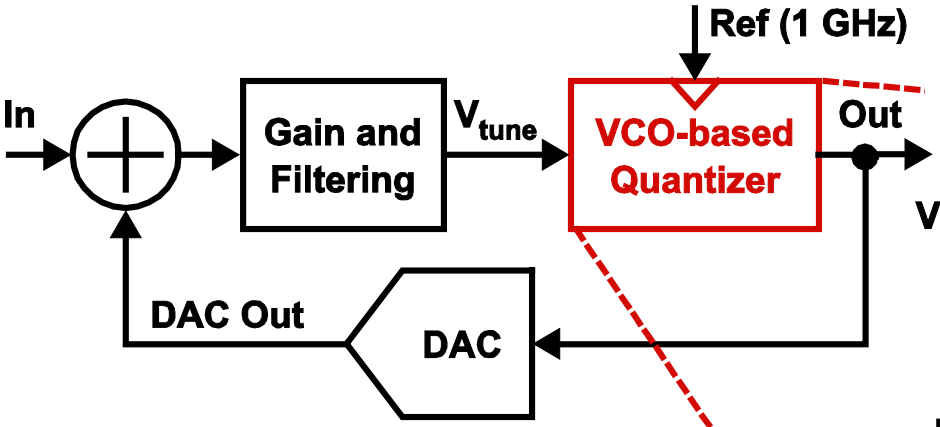
Nonlinearity is still an issue

Massive Digital Processing Can Deal with Nonlinearity

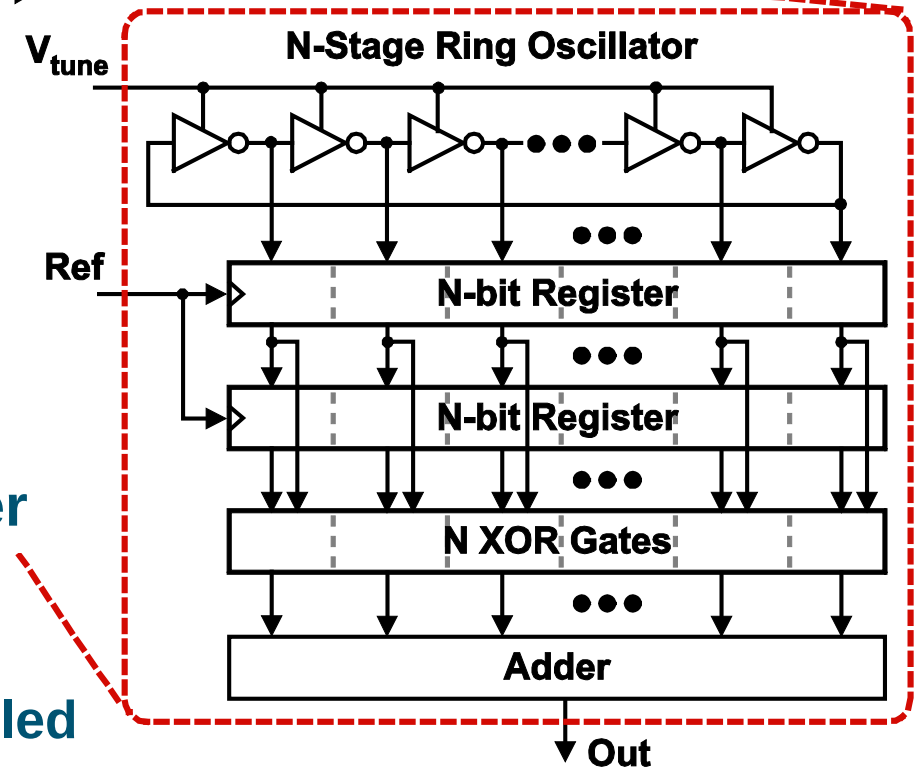


- From ISSCC 2010:
  - "A Mostly Digital Variable-Rate Continuous-Time ADC ΔΣ Modulator", *Taylor, Galton*
- We can also deal with nonlinearity in a more analog manner
  - Avoids long calibration startup due to nonlinearity
  - Allows high order noise shaping

Feedback Is Our Friend

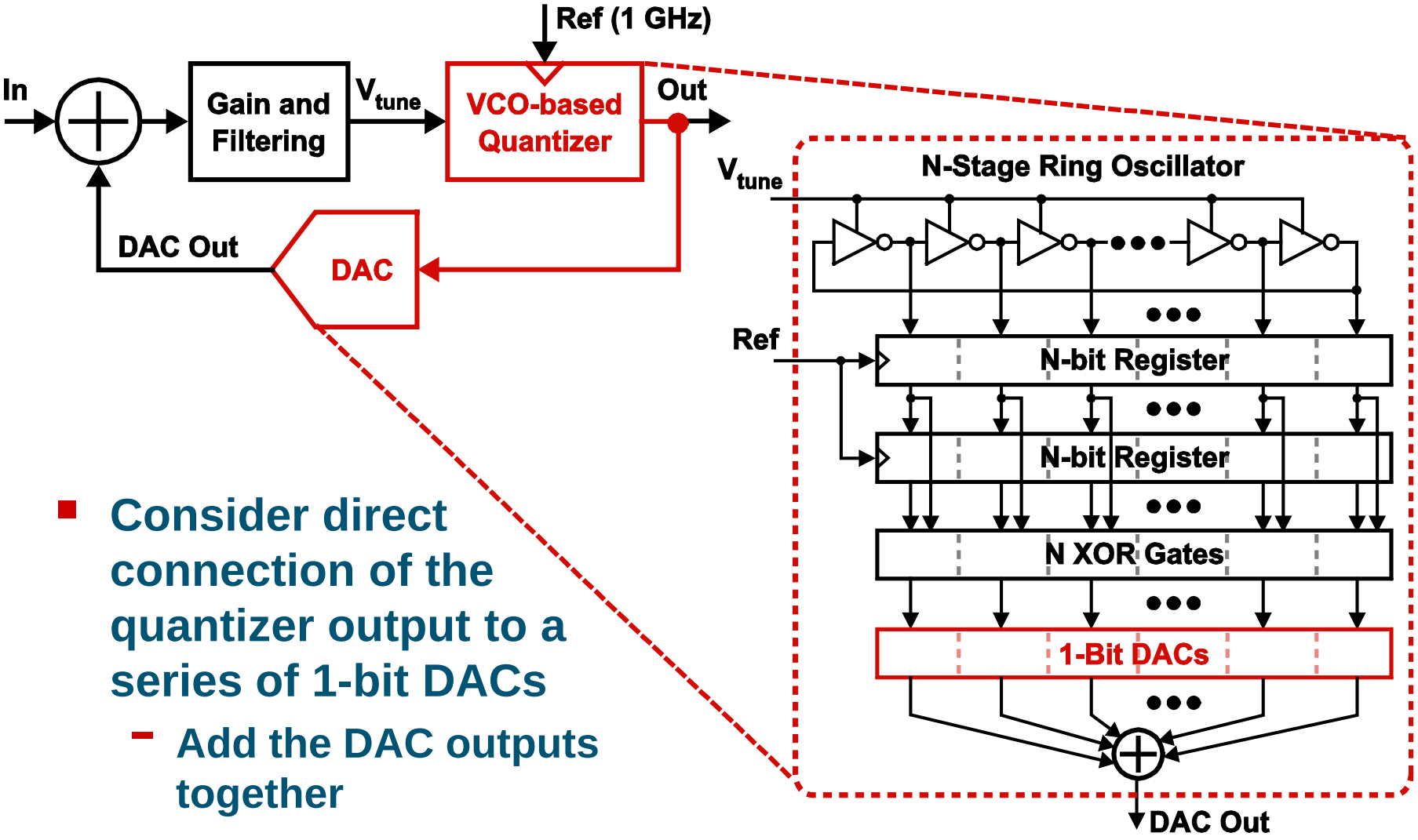


Iwata, Sakimura, TCAS II, 1999
Naiknaware, Tang, Fiez, TCAS II, 2000



- Combining feedback with front end gain acts to suppress impact of quantizer noise and nonlinearity
  - Scale factor from input to output is also better controlled
  - Structure is a continuous-time Sigma-Delta ADC
- Issue: must achieve a highly linear DAC structure
  - Otherwise, noise folding and other bad things happen …

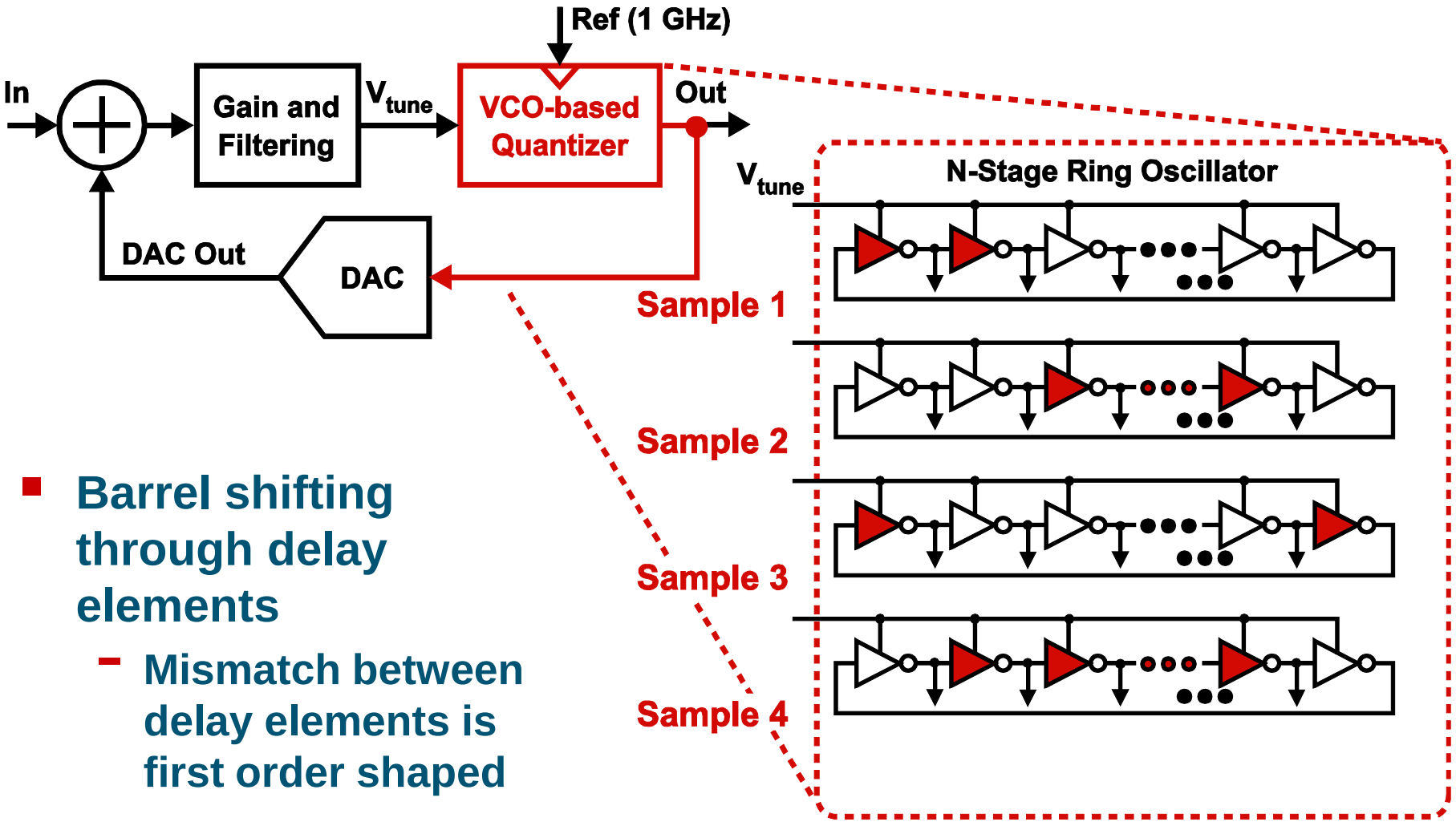
A Closer Look at the DAC Implementation



- Consider direct connection of the quantizer output to a series of 1-bit DACs
  - Add the DAC outputs together

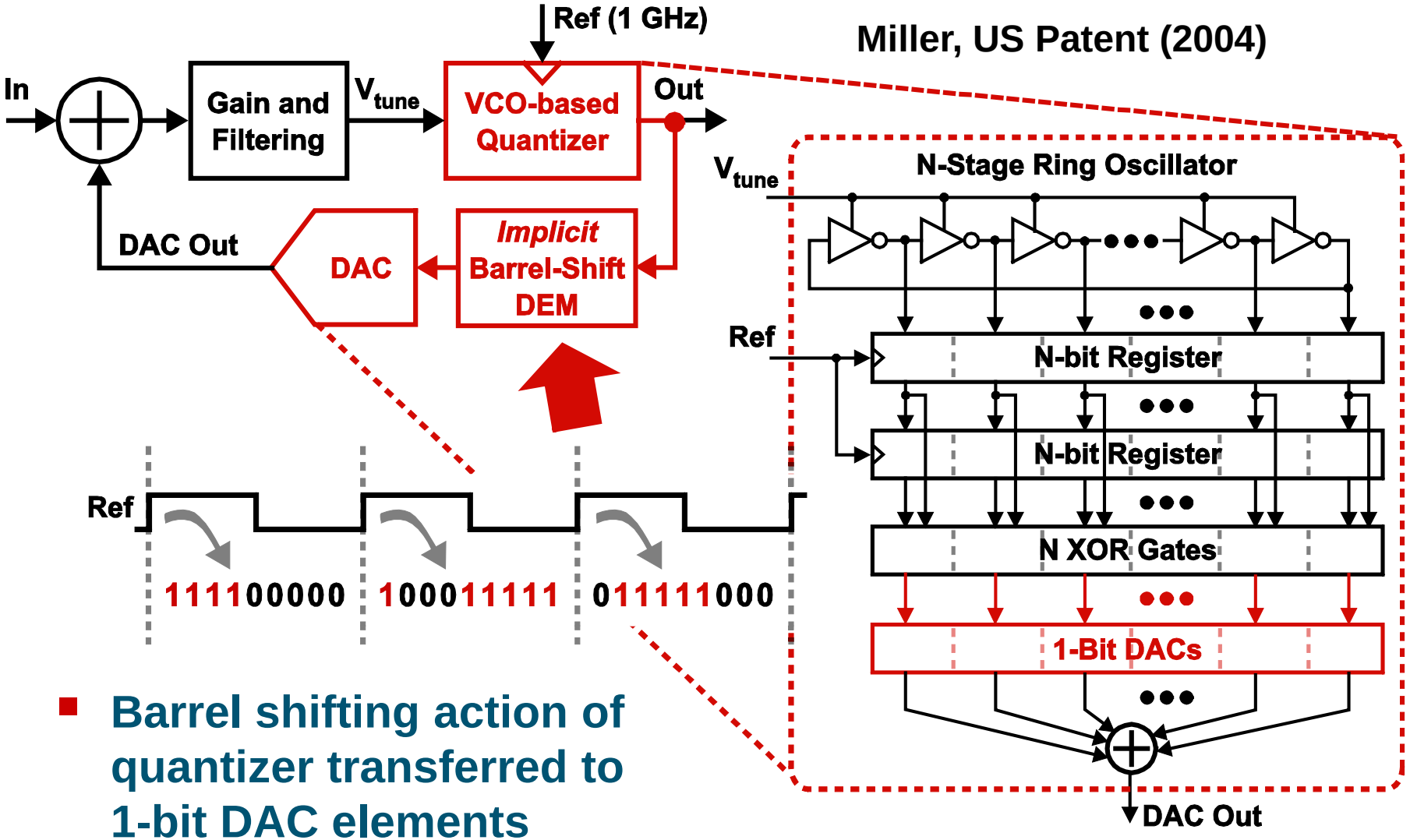
What is so special about doing this?

Recall that Ring Oscillator Offers Implicit Barrel Shifting



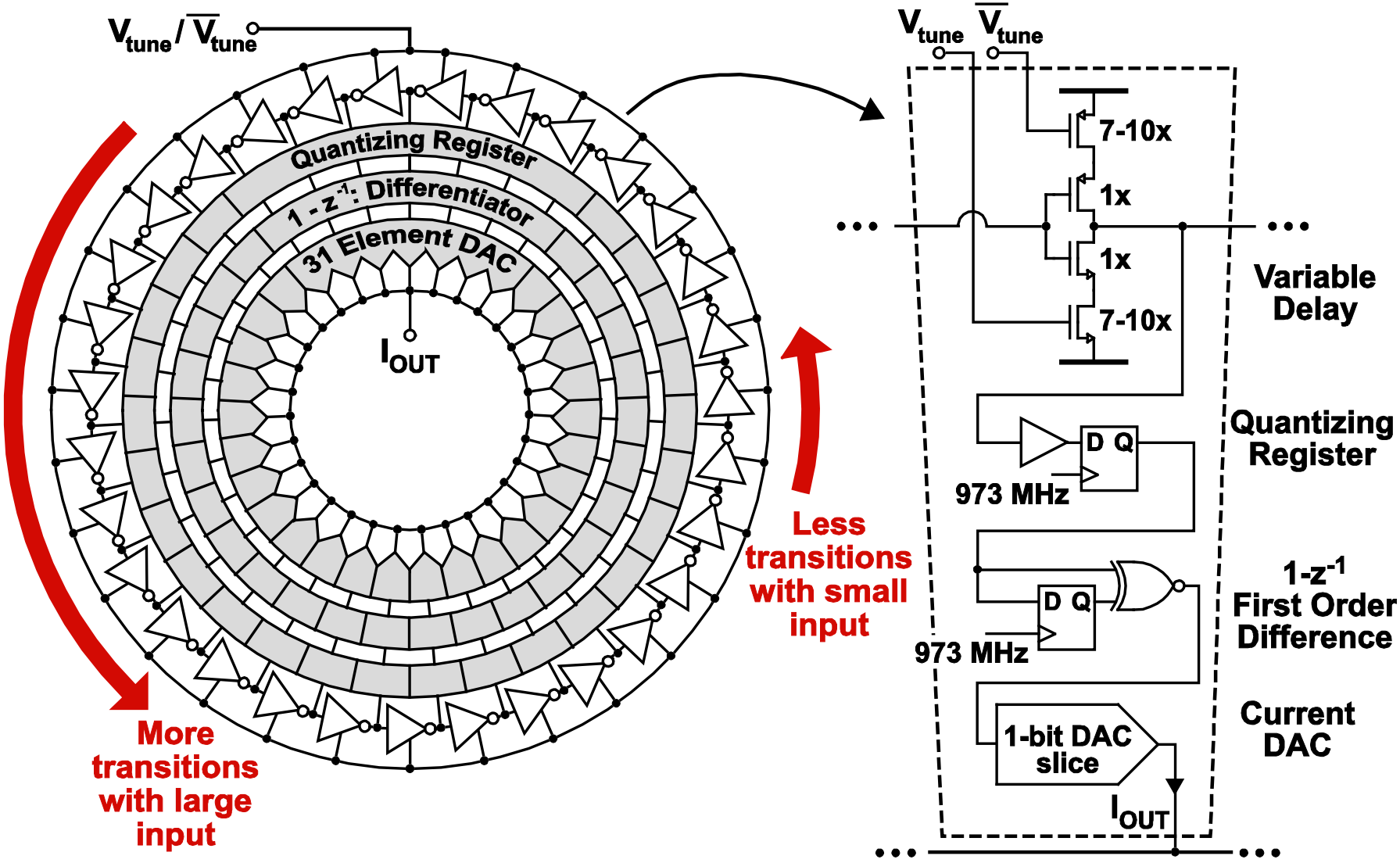
- Barrel shifting through delay elements
  - Mismatch between delay elements is first order shaped

Implicit Barrel Shifting Applied to DAC Elements

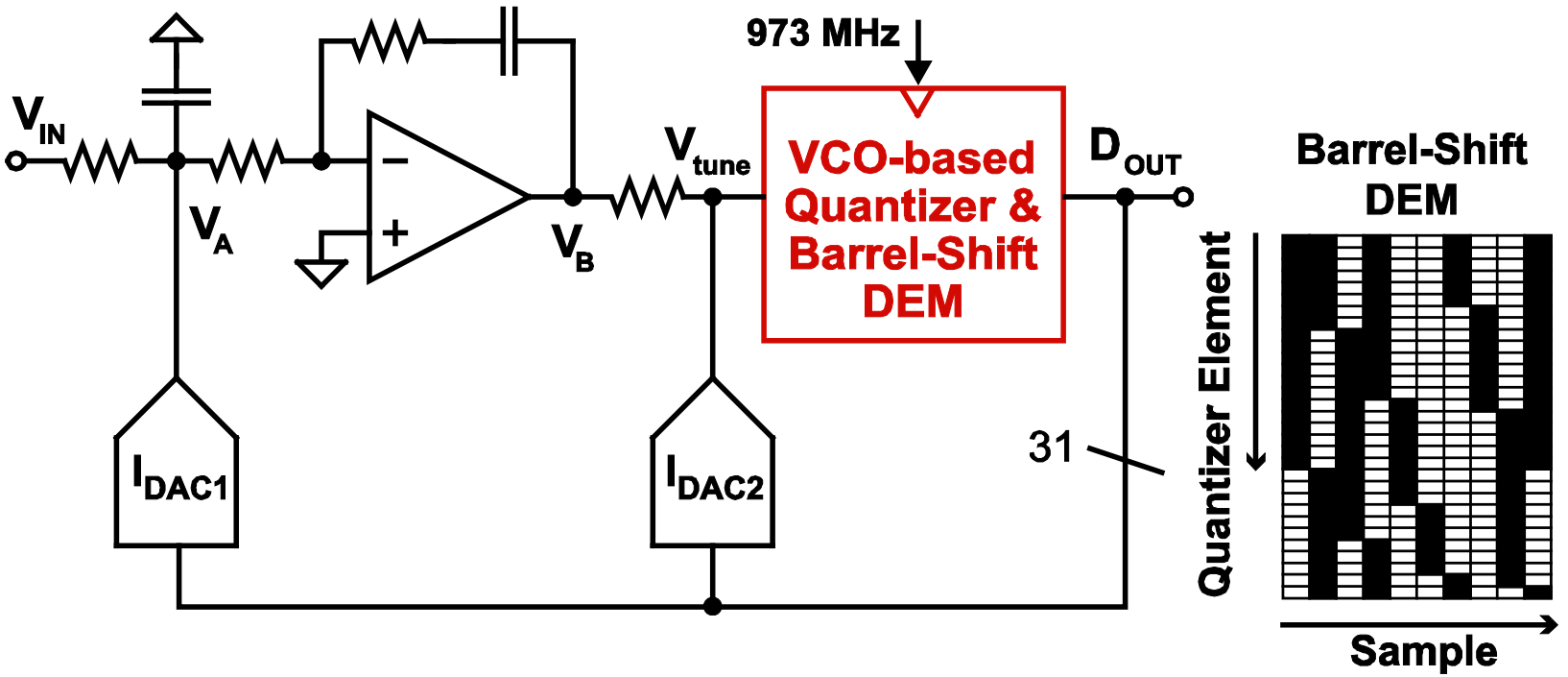


- Barrel shifting action of quantizer transferred to 1-bit DAC elements
  - Acts to shape DAC mismatch and linearize its behavior

A Geometric View of the VCO Quantizer/DEM and DAC

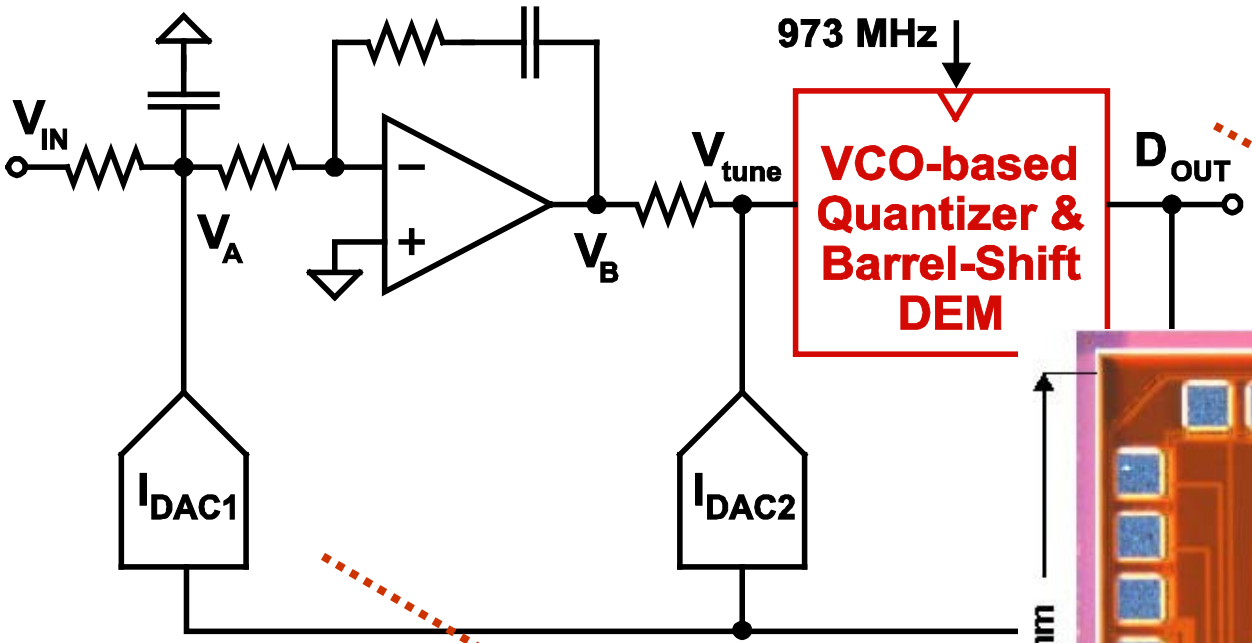


First Generation Prototype

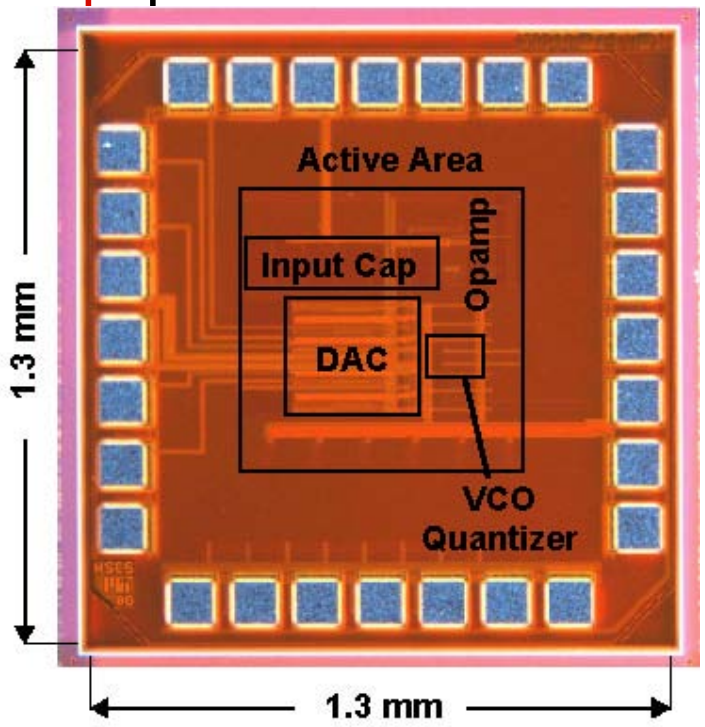


- Second order dynamics achieved with only *one* op-amp
  - Op-amp forms one integrator
  - I_{dac1} and passive network form the other (lossy) integrator
  - Minor loop feedback compensates delay through quantizer
- *Third order* noise shaping is achieved!
  - VCO-based quantizer adds an extra order of noise shaping

Custom IC Implementing the Prototype

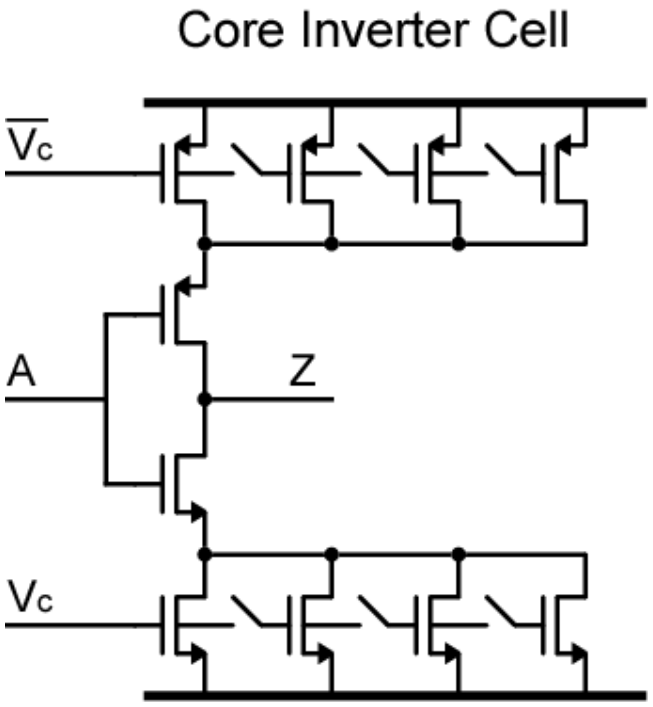


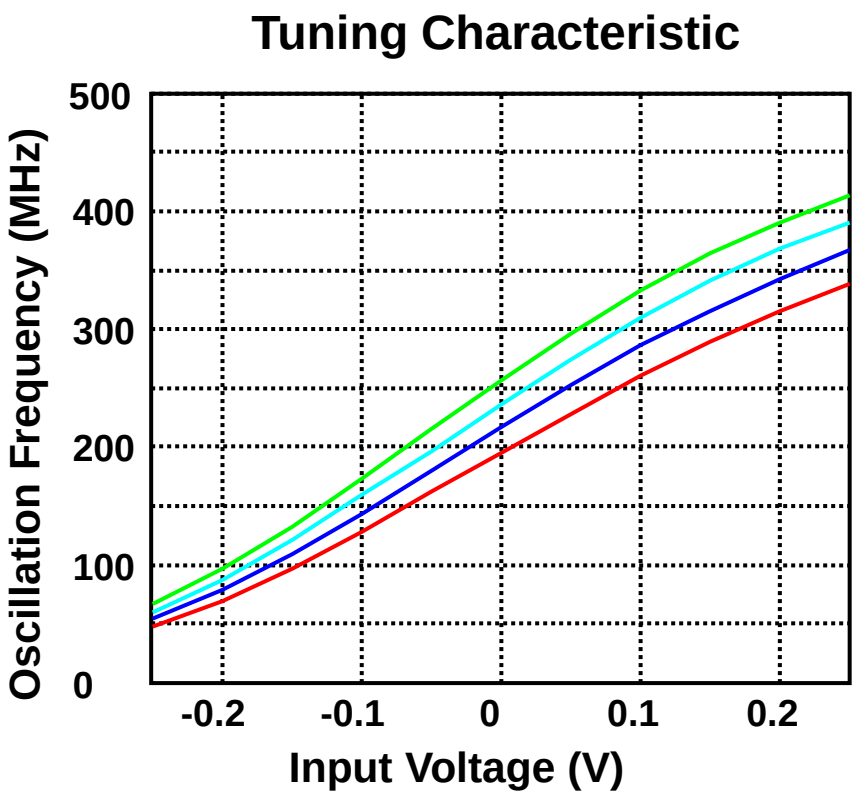
Straayer, Perrott
VLSI 2007



- 0.13u CMOS
- Power: 40 mW
- Active area: 700u X 700u
- Peak SNDR: 67 dB (20 MHz BW)
- Efficiency: 0.5 pJ/conv. step

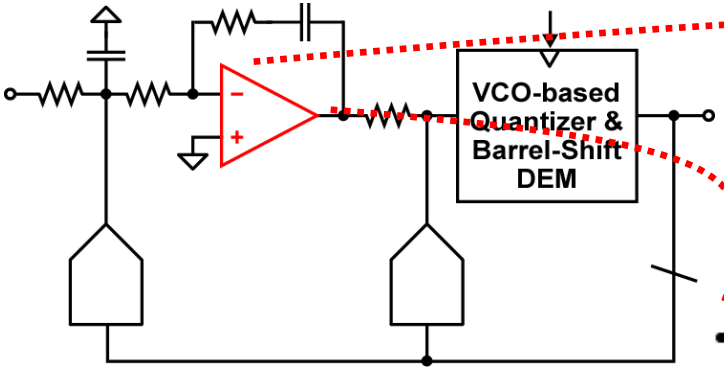
Design of the VCO Core Inverter Cell





- 31 stages
- Fast for good resolution (< 100 psec / stage)
- Large K_{VCO} (600-700 MHz) with good dynamic range
- 2 bits of coarse tuning for process variations
- < 8 mW for 1 GSPS 5-bit quantizer / DEM

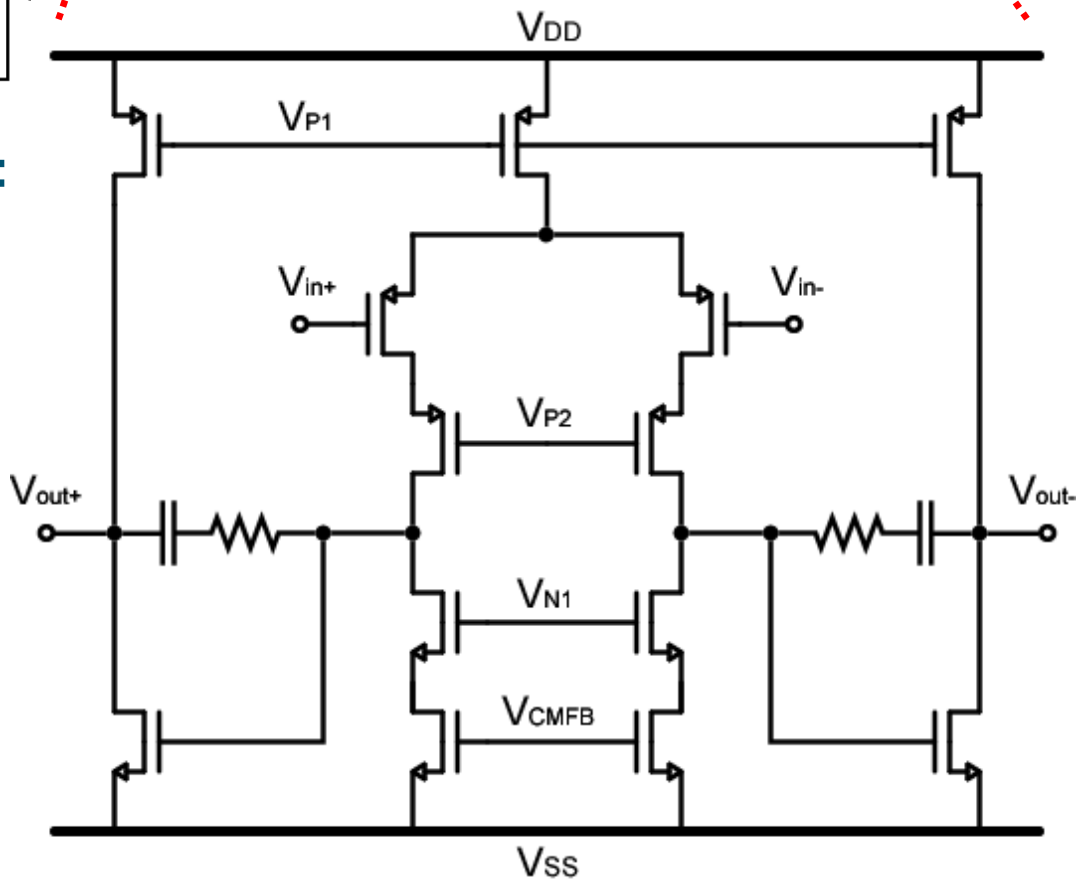
Opamp Design is Straightforward



Simulated Performance:

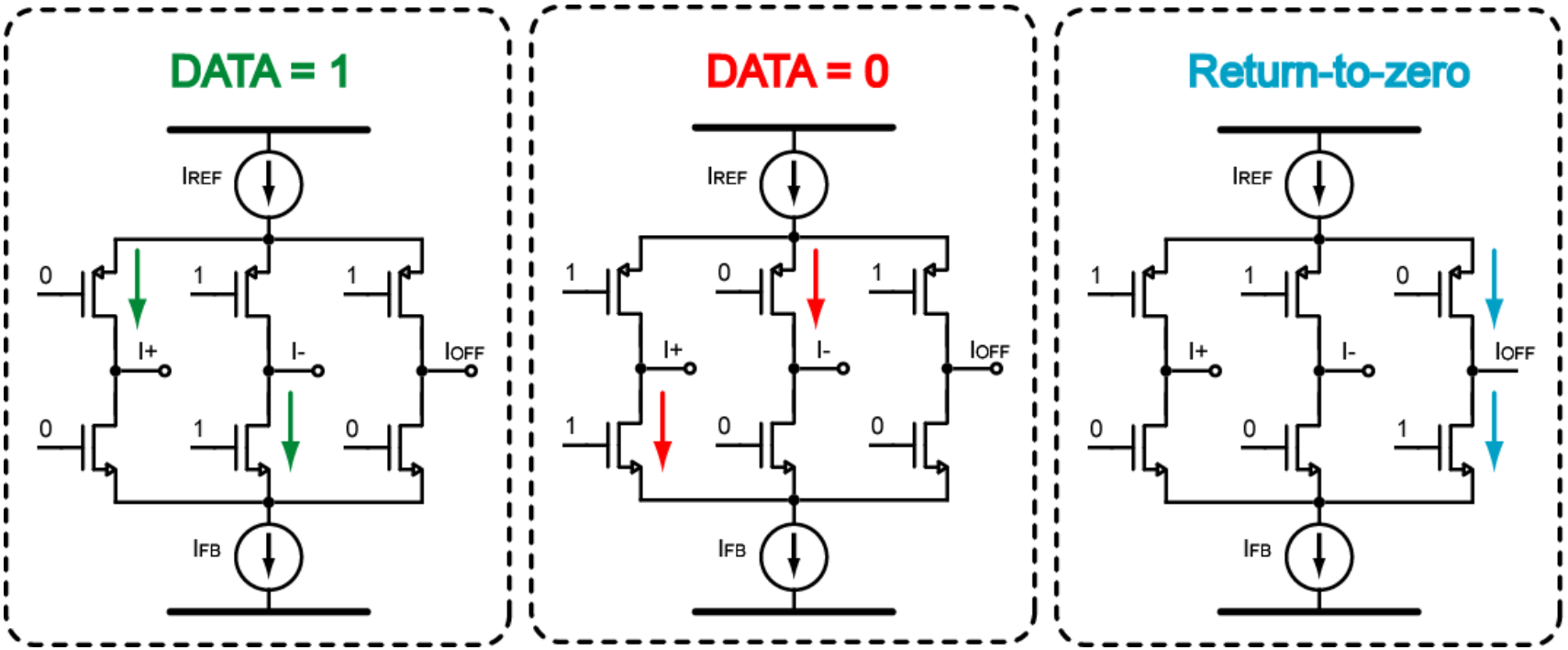
- A_V = 55 dB
- GBW = 2 GHz
- P_{DISS} = 15 mW

High SNR of VCO-based quantizer allows reduced opamp gain (A_V)

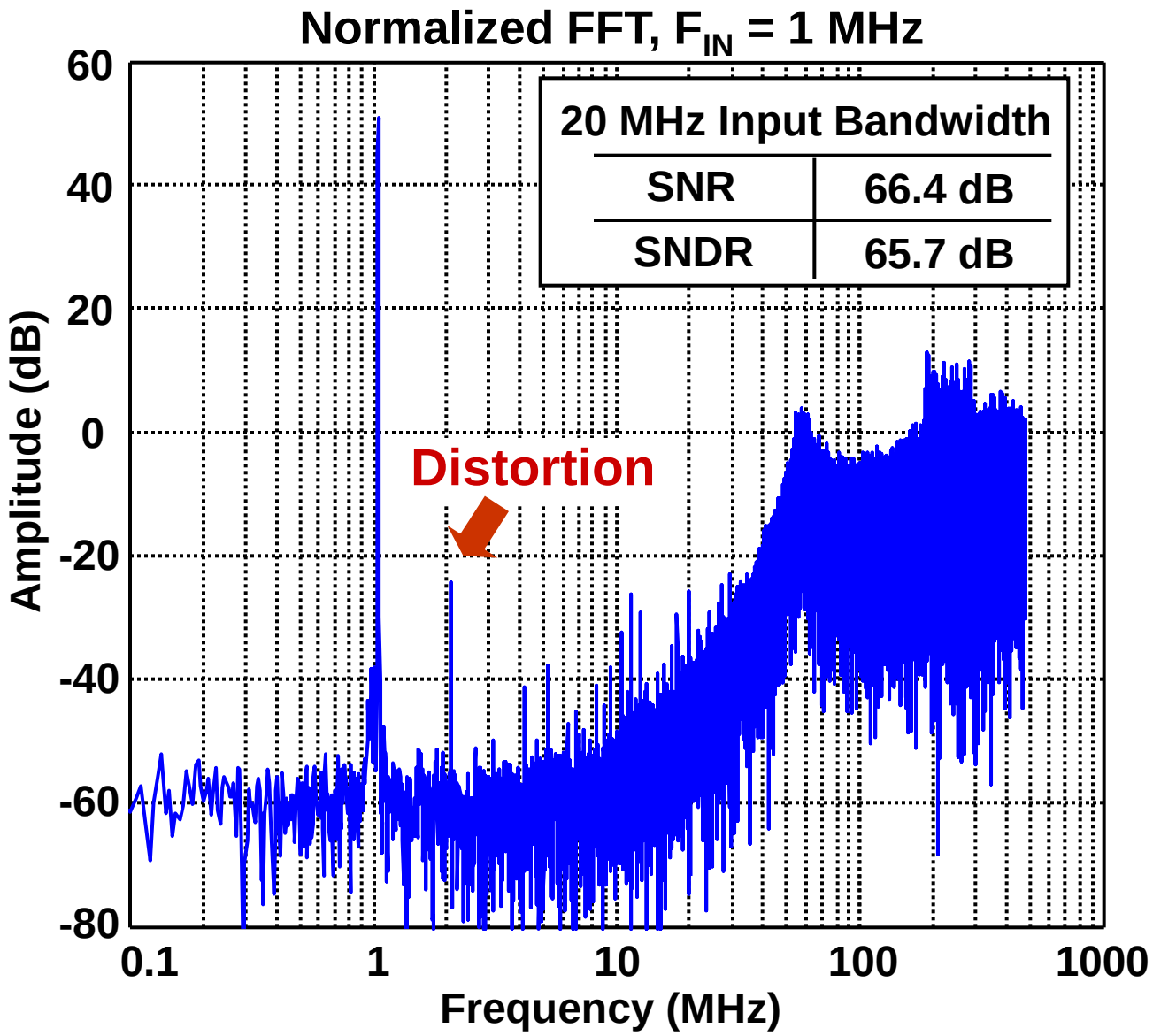


Primary Feedback DAC Schematic

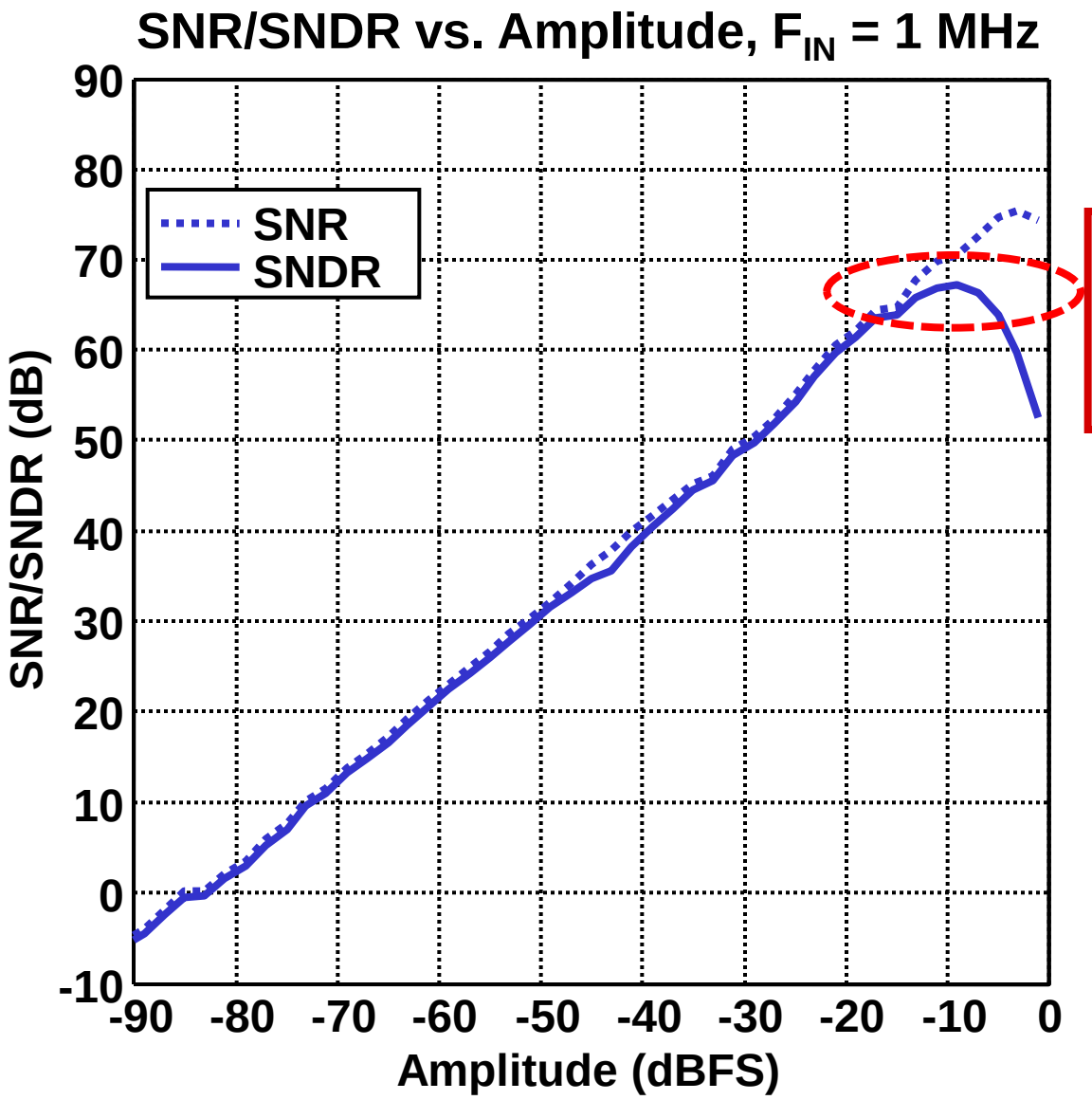
- **Fully differential RZ pulses**
- **Triple-source current steering**
- **I_{OFF} is terminated off-chip**



Measured Spectrum From Prototype



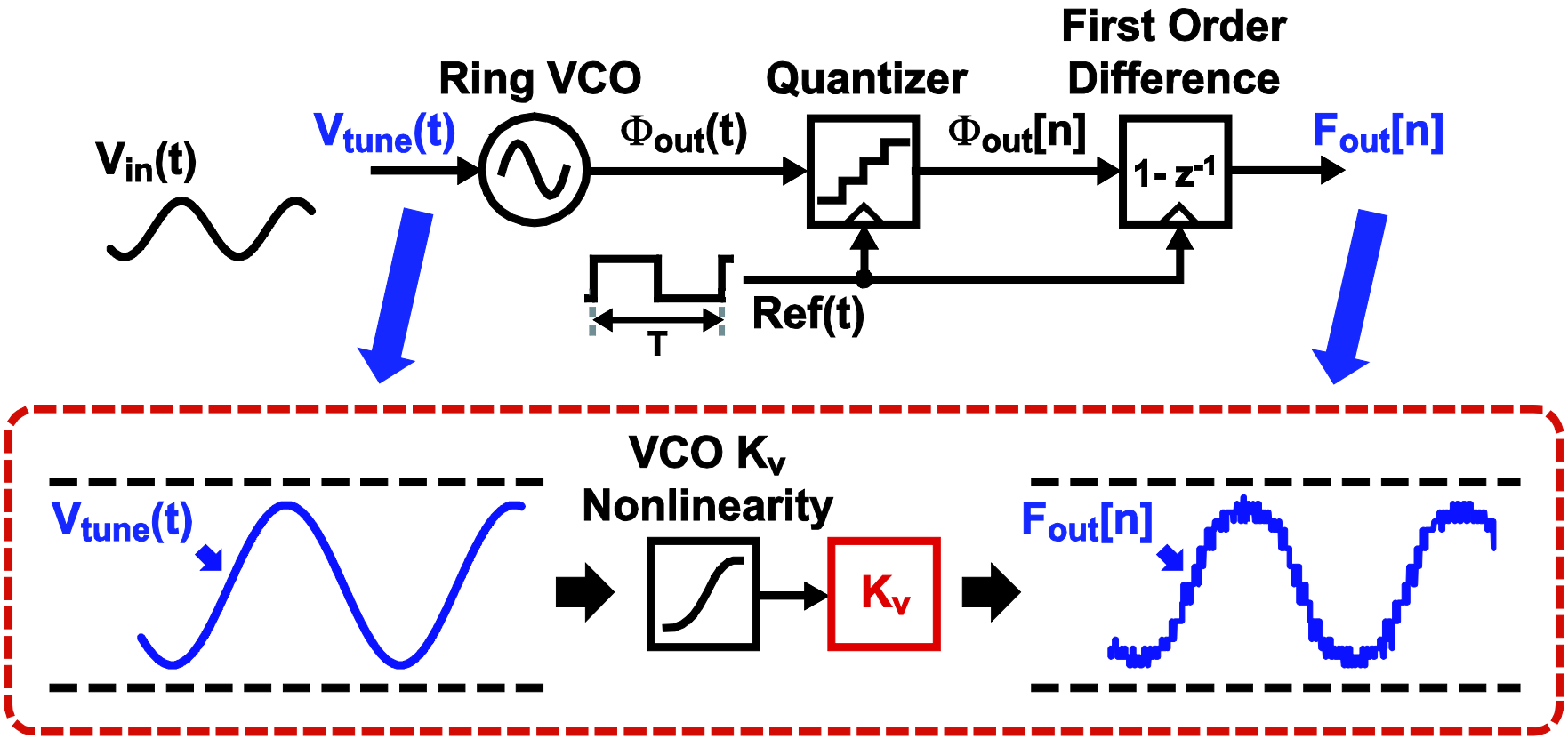
Measured SNR/SNDR Vs. Input Amplitude (20 MHz BW)



K_v nonlinearity limits SNDR to 67 dB

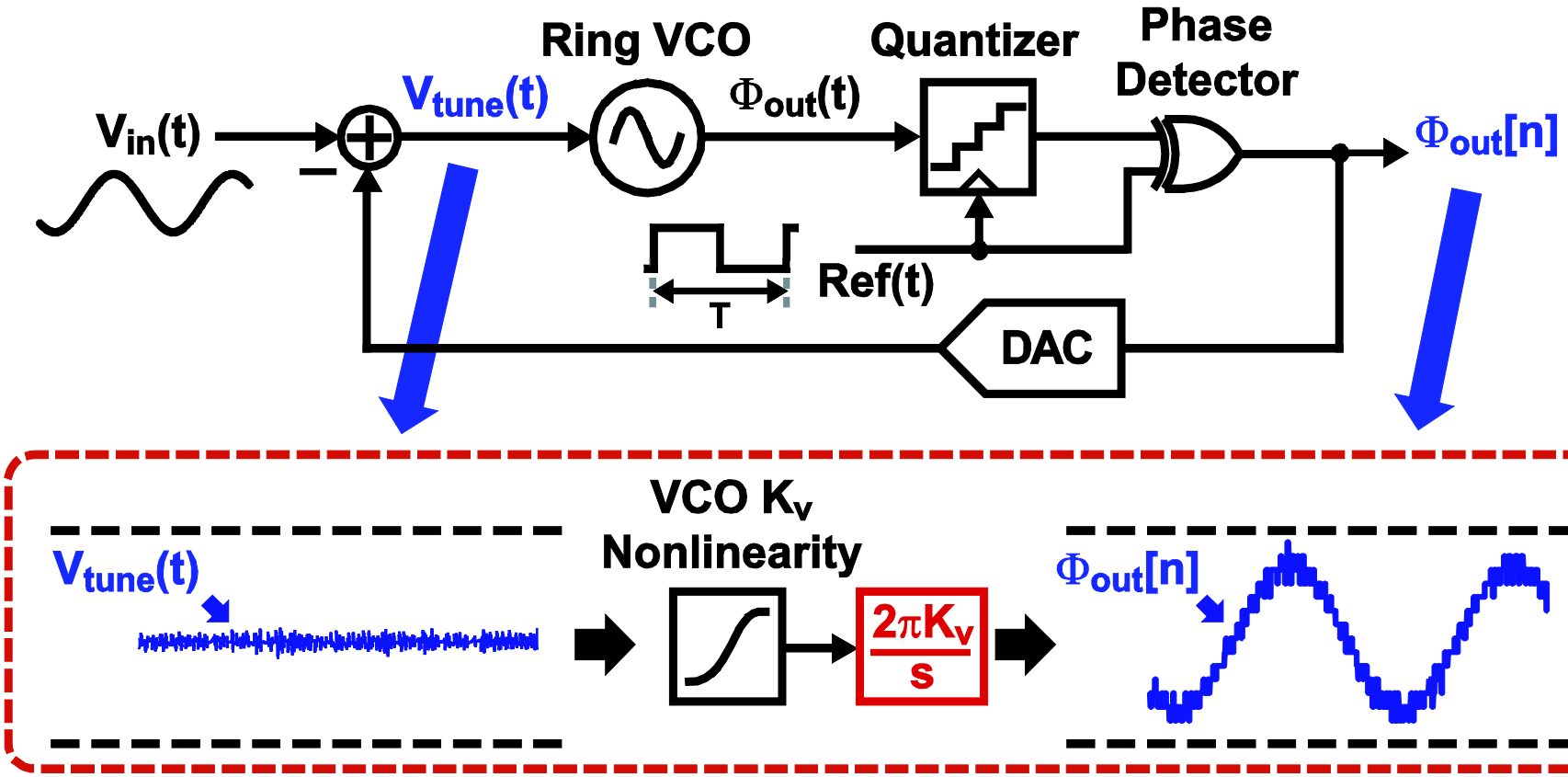
How Do We Overcome K_v Nonlinearity to Improve SNDR?

Voltage-to-Frequency VCO-based ADC (1st Order Σ–Δ)



- In prior work, VCO *frequency* is desired output variable
  - Input must span the entire non-linear voltage-to-frequency (K_v) characteristic to exercise full dynamic range
  - Strong distortion at extreme ends of the Kv curve

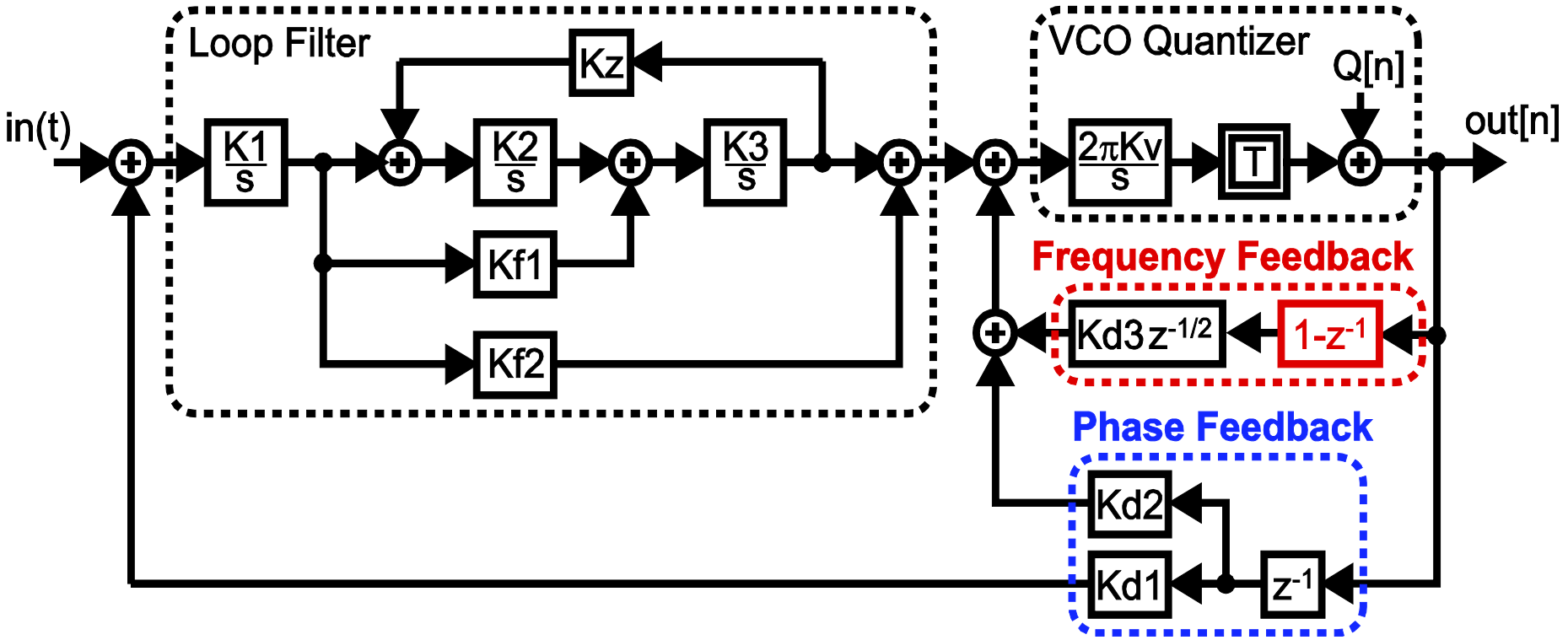
Proposed Voltage-to-Phase Approach (1st Order Σ–Δ)



- VCO output *phase* is now the output variable
  - Small perturbation on V_{tune} allows large VCO phase shift
  - VCO acts as a CT integrator with *infinite* DC gain

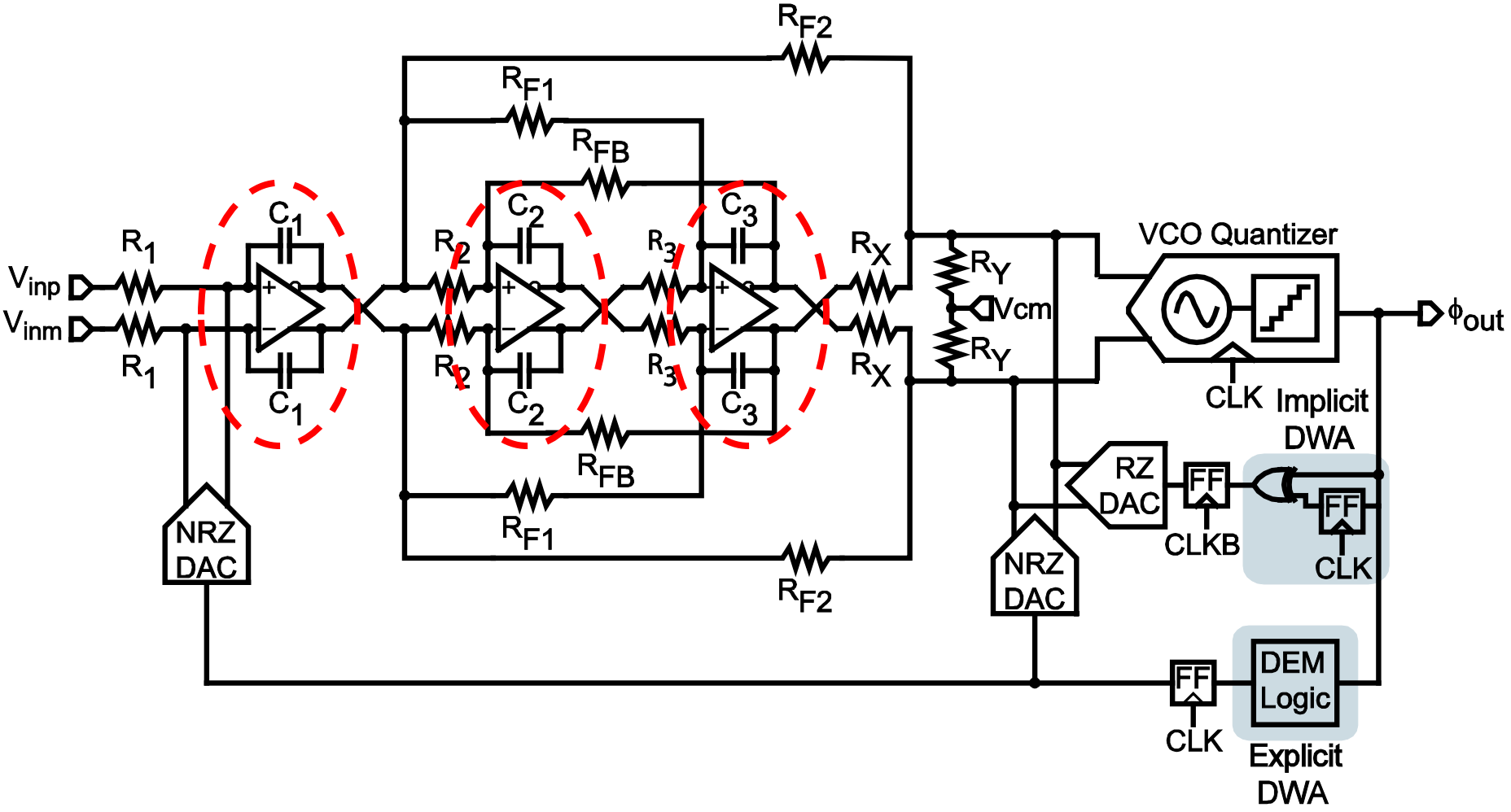
High SNDR requires higher order Σ–Δ …

Proposed 4th Order Architecture for Improved SNDR



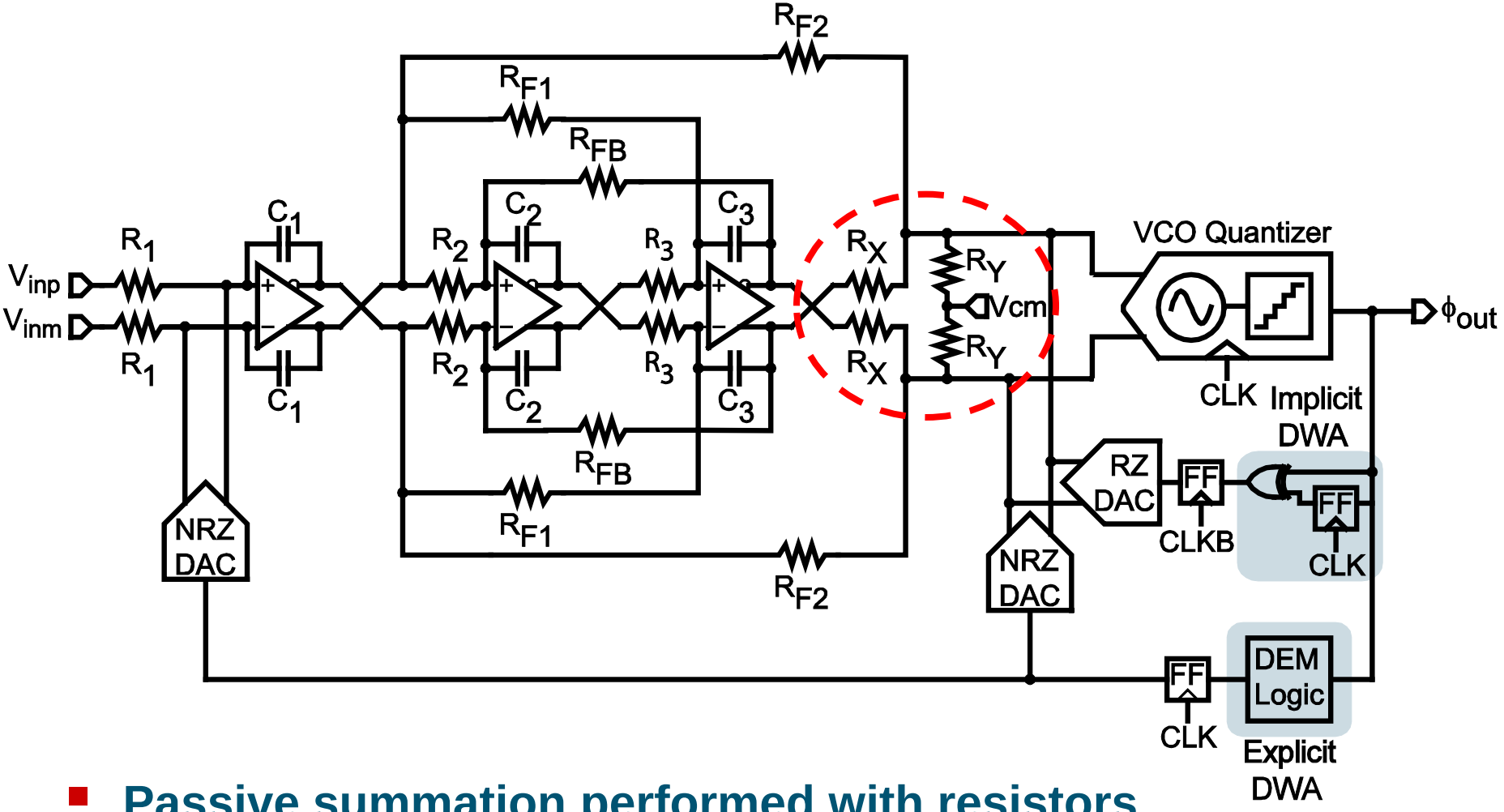
- **Goal: ~80 dB SNDR with 20 MHz bandwidth**
  - **Achievable with 4th order loop filter, 4-bit VCO-based quantizer**
  - **4-bit quantizer: tradeoff resolution versus DEM overhead**
- **Combined frequency/phase feedback for stability/SNDR**

Schematic of Proposed Architecture



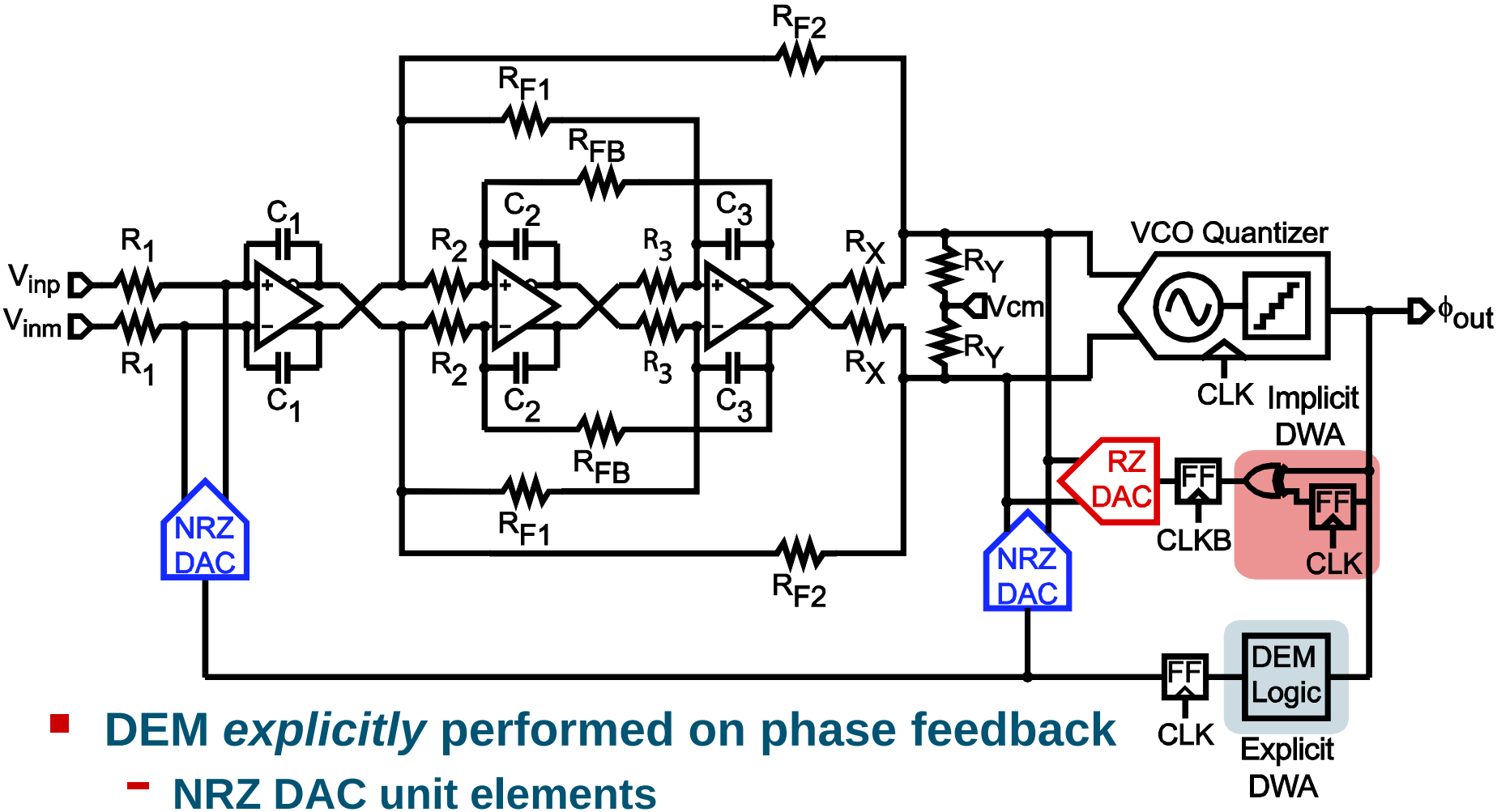
- Opamp-RC integrators
  - Better linearity than Gm-C, though higher power

Schematic of Proposed Architecture



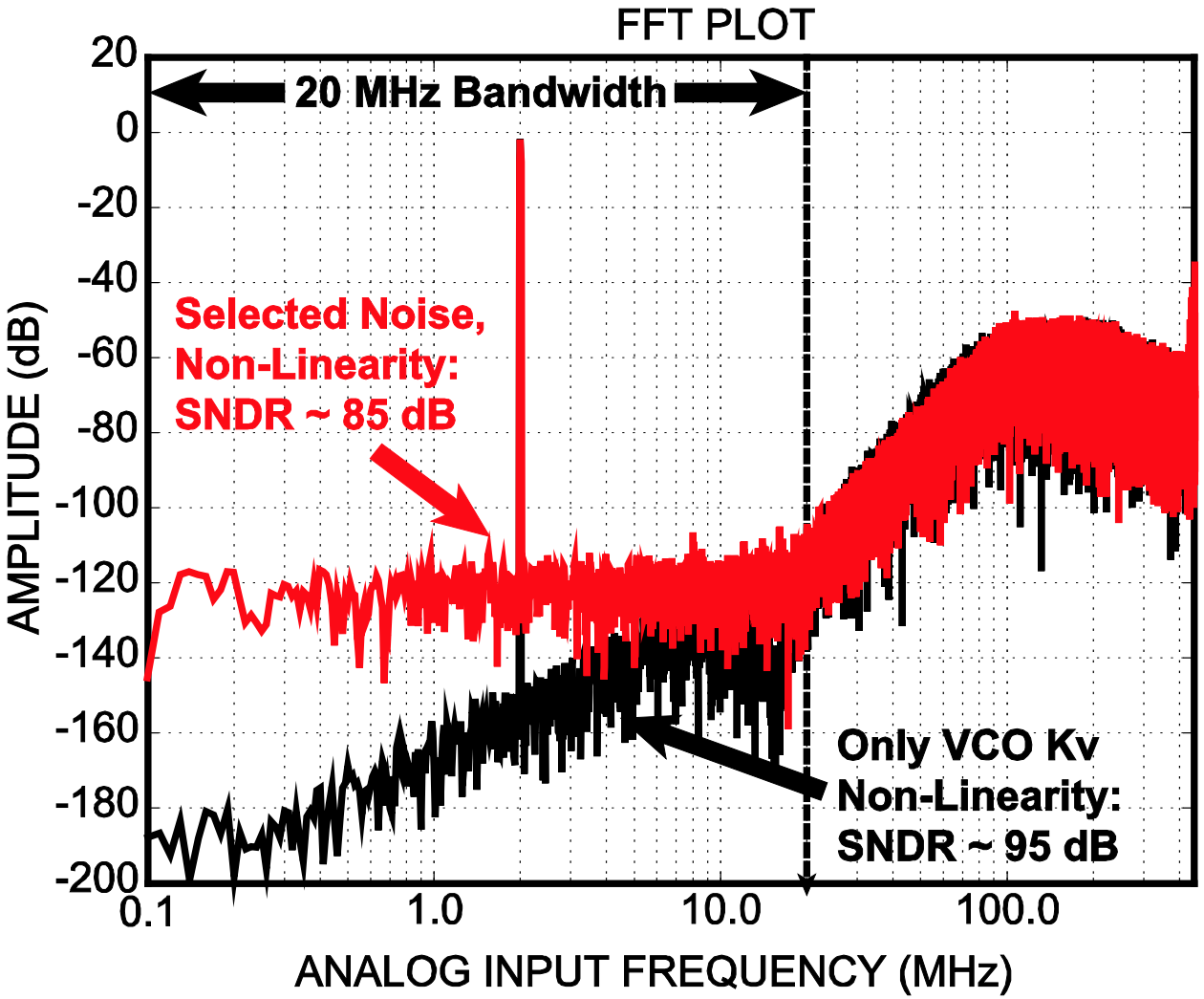
- Passive summation performed with resistors
  - Low power
  - Must design carefully to minimize impact of parasitic pole

Schematic of Proposed Architecture



- DEM *explicitly* performed on phase feedback
  - NRZ DAC unit elements
- DEM *implicitly* performed on frequency feedback (Miller)
  - RZ DAC unit elements

Behavioral Simulation (available at www.cppsim.com)



Key Nonidealities

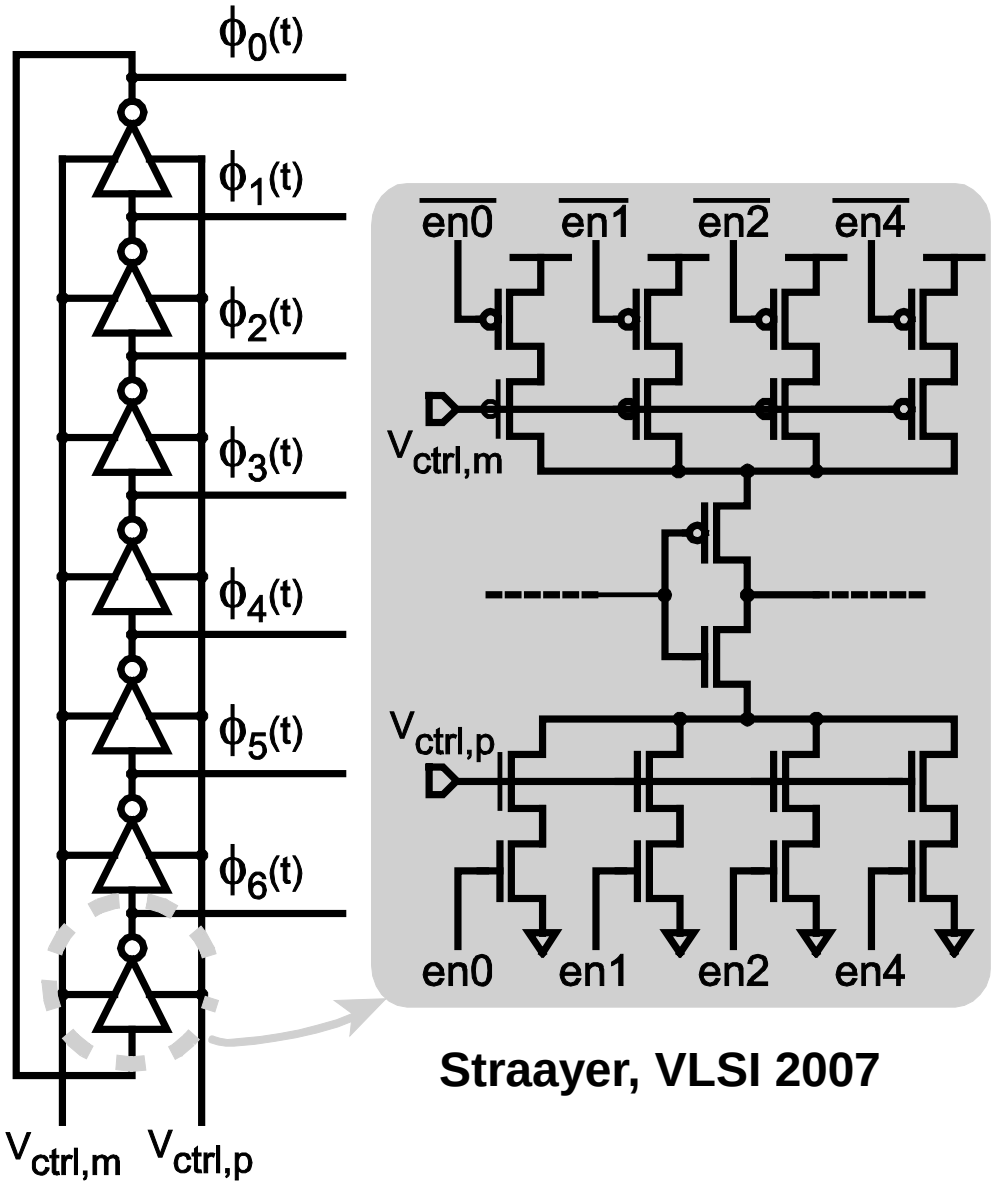
- VCO Kv non-linearity
- Device noise
- Amplifier finite gain, finite BW
- DAC and VCO unit element mismatch

85 dB SNDR!

VCO nonlinearity is *not* the bottleneck for achievable SNDR!

Circuit Details

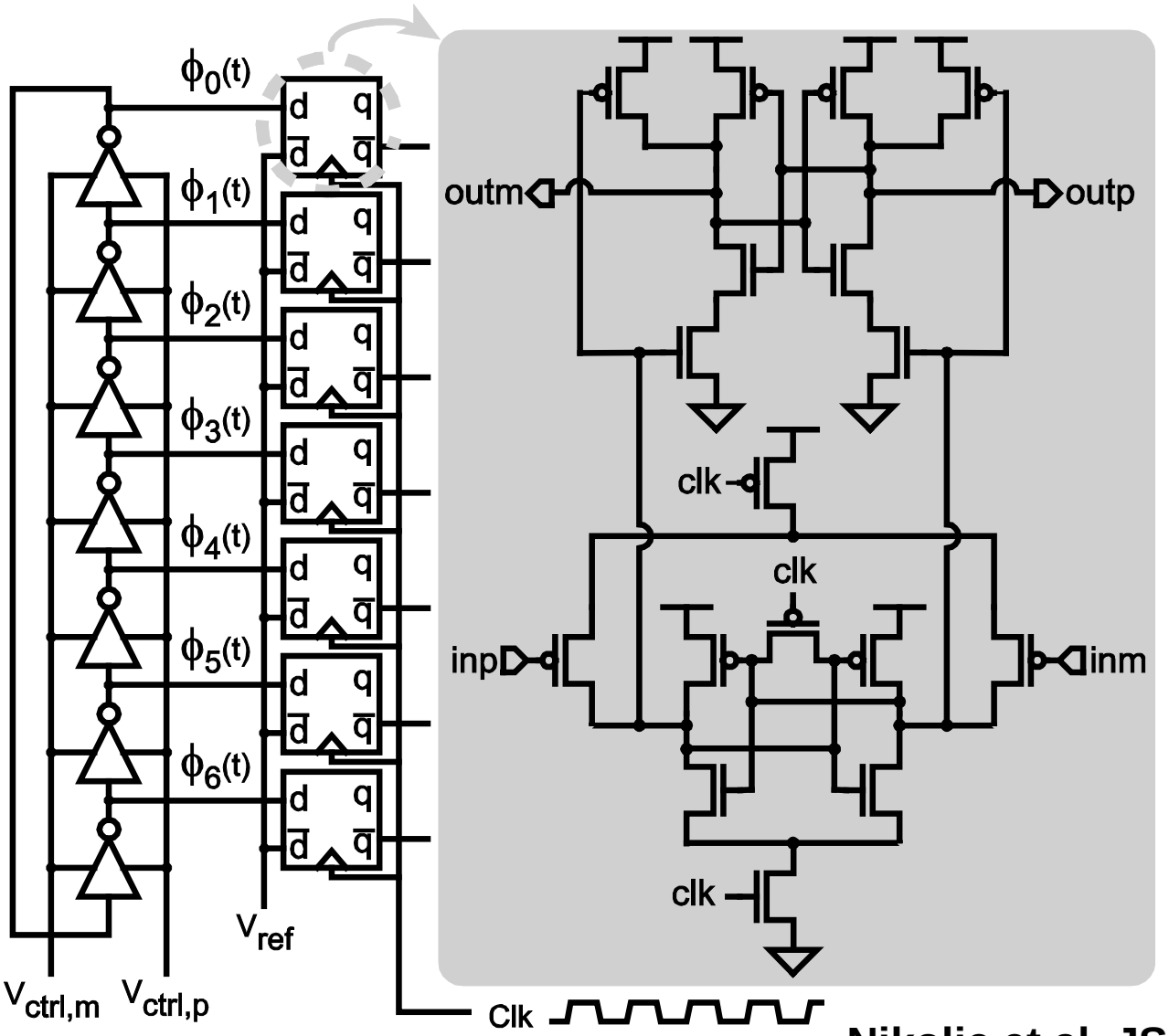
VCO Integrator Schematic



Straayer, VLSI 2007

- 15 stage current starved ring-VCO
  - 7 stage ring-VCO shown for simplicity
  - Pseudo differential control
  - PVT variation accommodated by enable switches on PMOS/NMOS
- Rail-to-rail VCO output phase signals (VDD to GND)

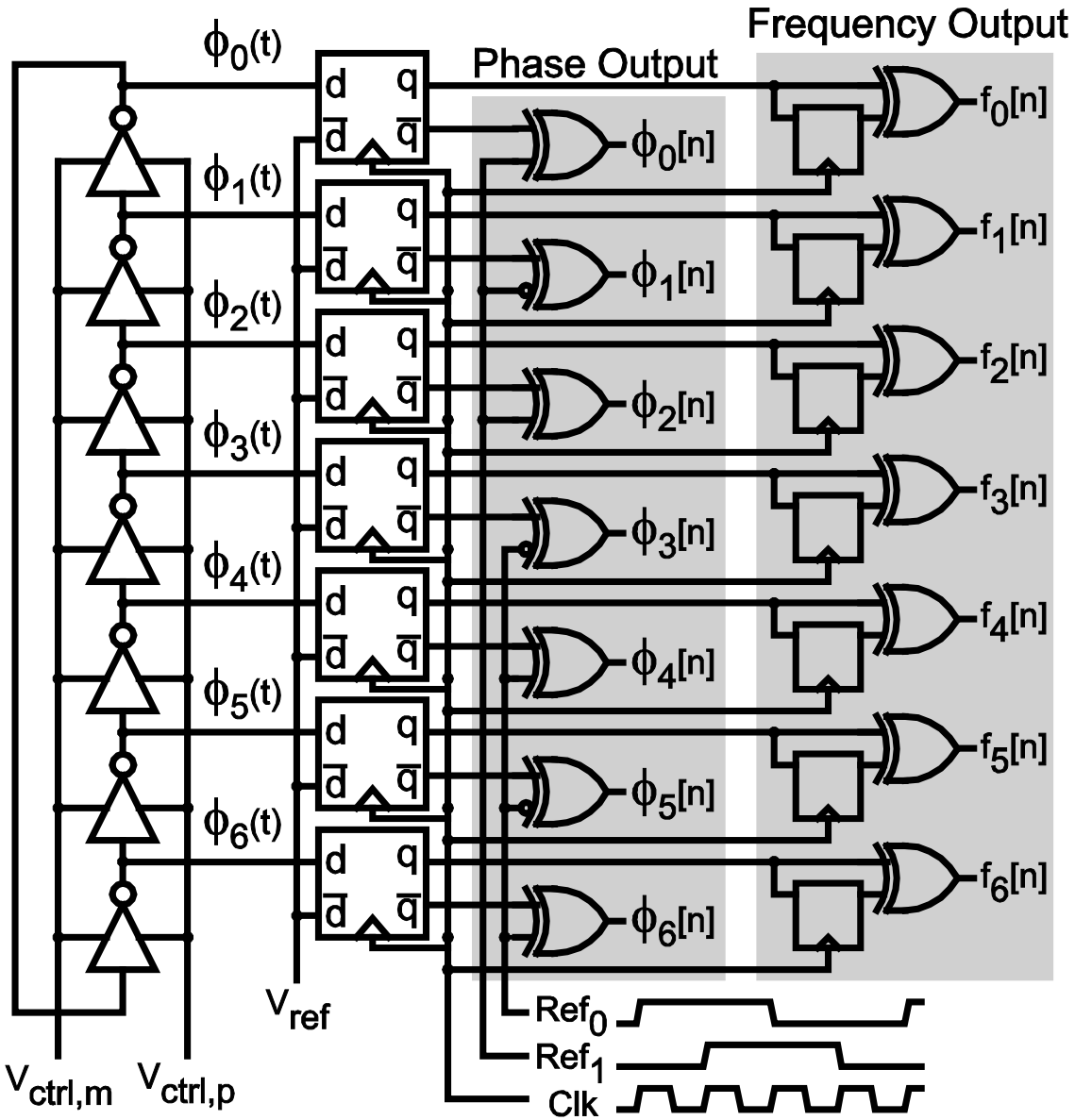
VCO Quantizer Schematic



- **Phase quantization with sense-amp flip-flop**
  - **Single phase clocking**
- **Rail-to-rail quantizer output signals (VDD to GND)**

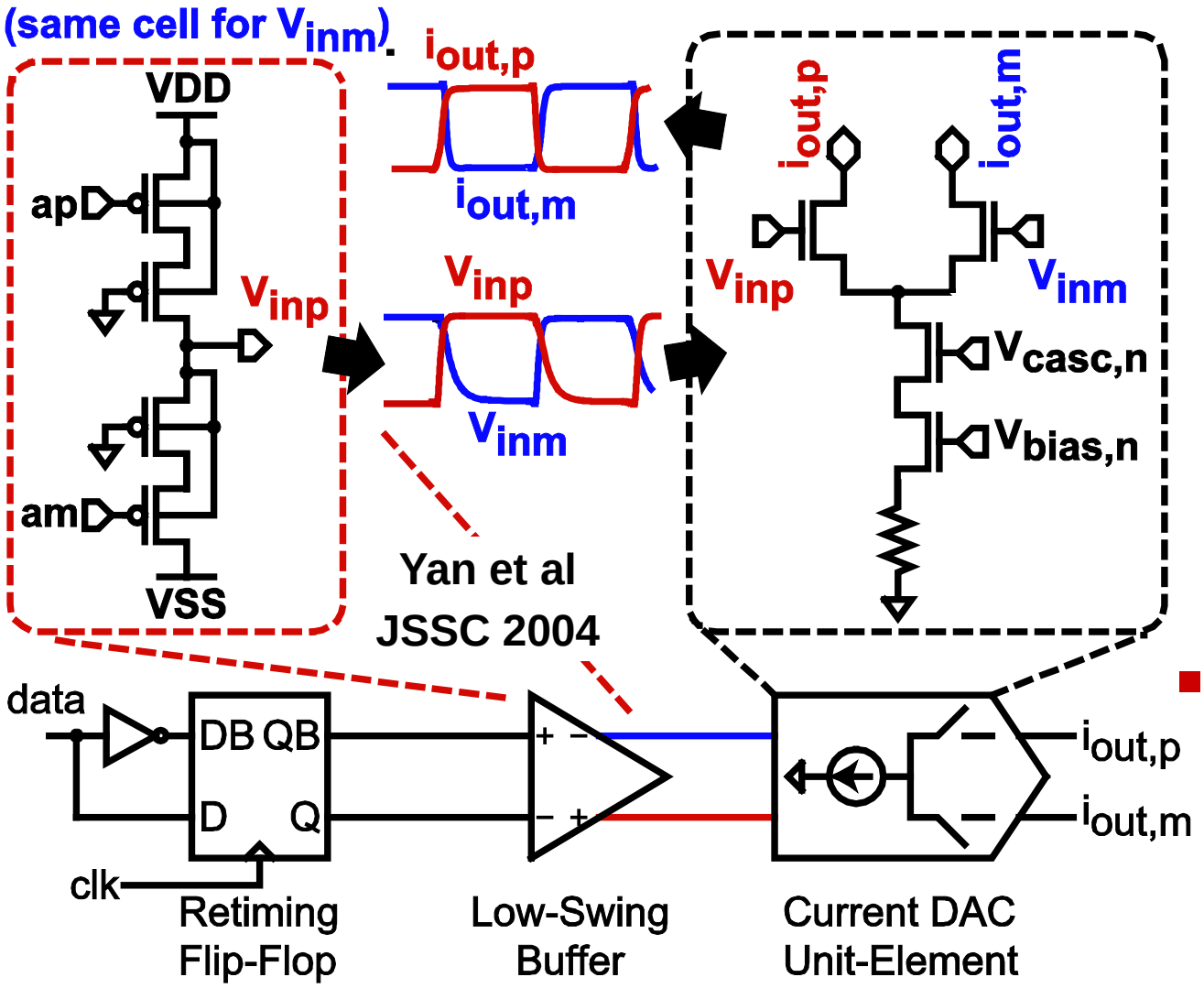
Nikolic et al, JSSC 2000

Phase Quantizer, Phase and Frequency Detector



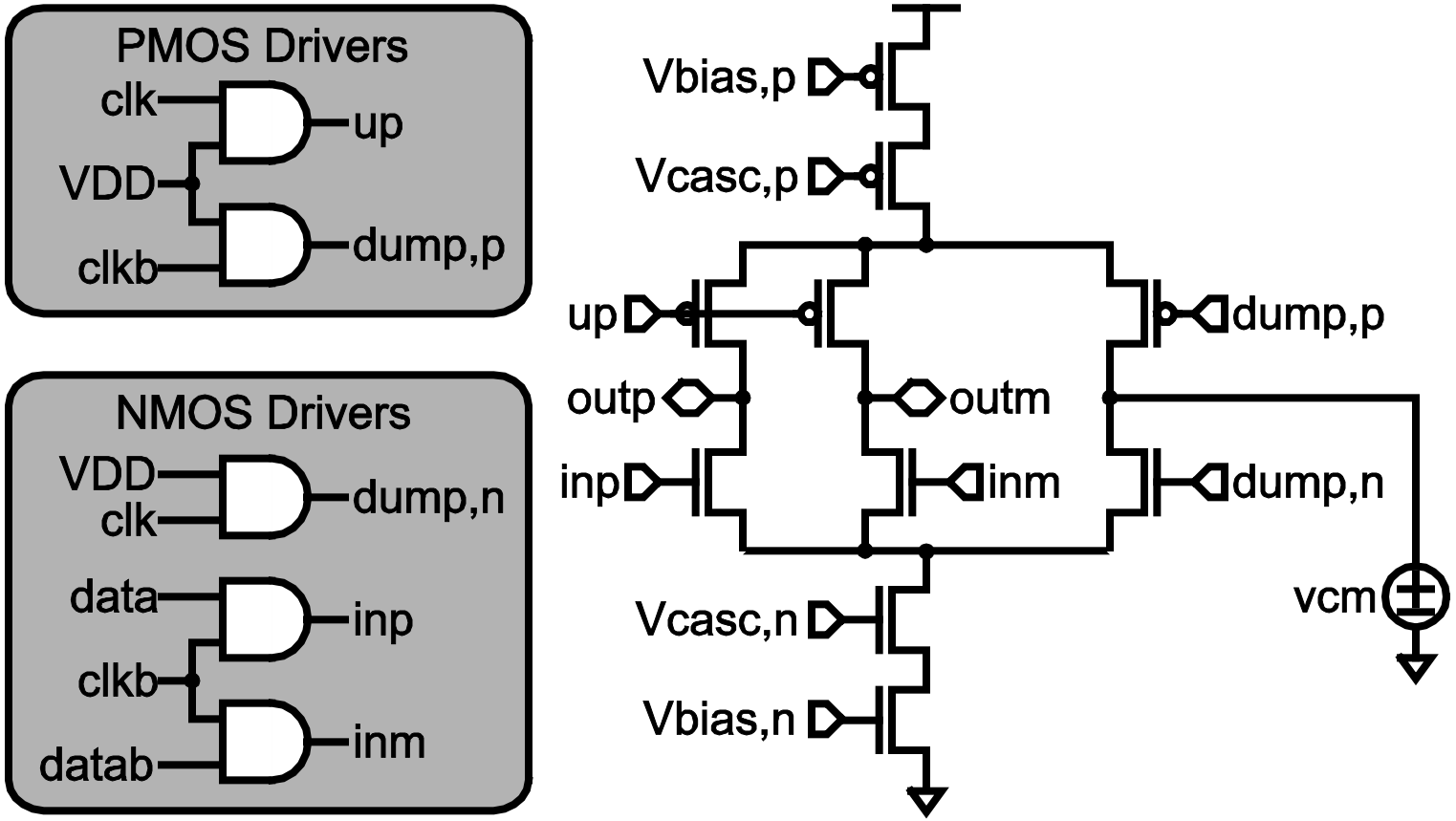
- **Highly digital implementation**
  - Phase sampled & quantized by SAFF
  - XOR phase and frequency detection with FF and XOR
- **Automatic DWA for frequency detector output code**
  - Must explicitly perform DWA on phase detector output code

Main Feedback DAC Schematic



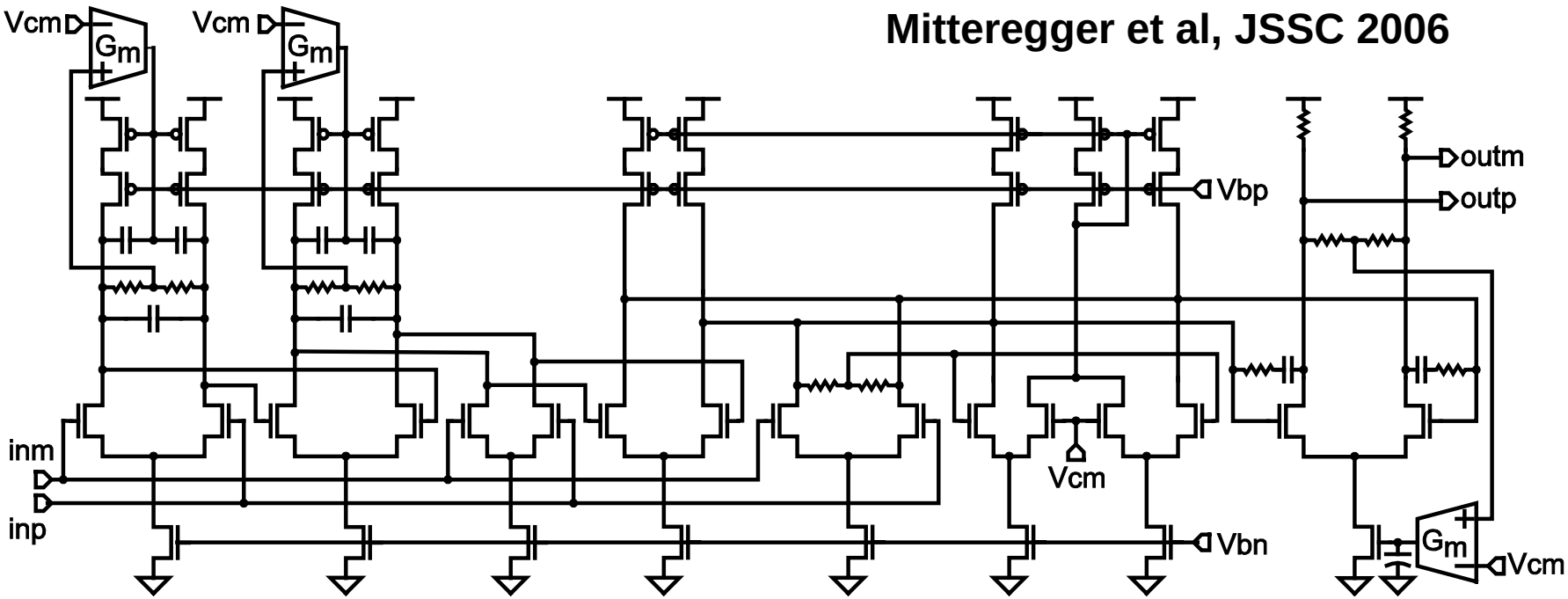
- Low-swing buffers
  - Keeps switch devices in saturation
  - Fast “on” / Slow “off” reduces glitches at DAC output
  - Uses external Vdd/Vss
- Resistor degeneration minimizes 1/f noise

Bit-Slice of Minor Loop RZ DAC



- RZ DAC unit elements transition every sample period
  - Breaks code-dependency of transient mismatch (ISI)
  - Uses full-swing logic signals for switching

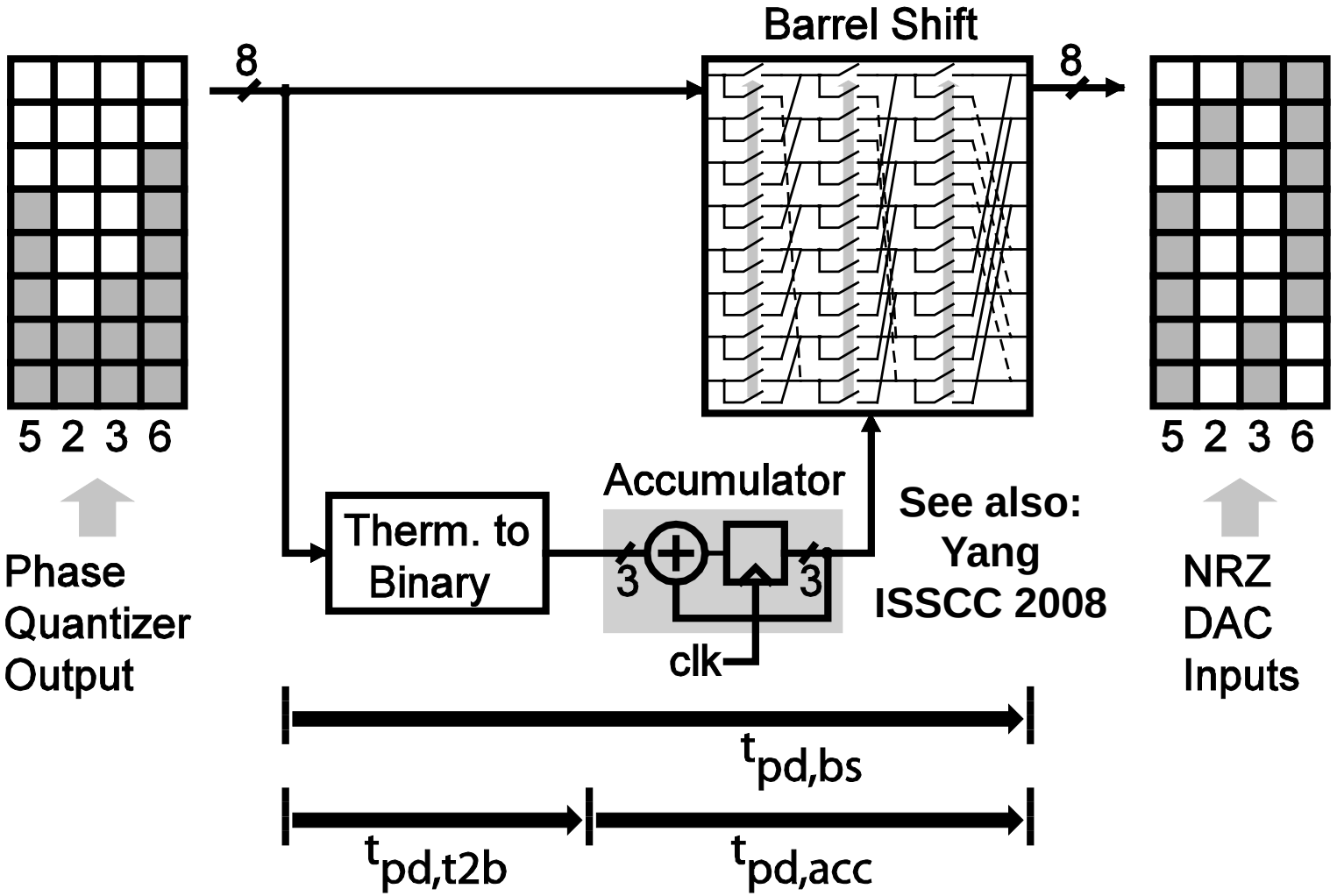
Opamp Schematic



Parameter	Value
DC Gain	63 dB
Unity-Gain Frequency	4.0 GHz
Phase Margin	55°
Input Referred Noise Power (20 MHz BW)	11 uV (rms)
Power (V_{DD} = 1.5 V)	22.5 mW

- Modified nested Miller opamp
  - 4 cascaded gain stages, 2 feedforward stages
  - Behaves as 2-stage Miller near cross-over frequencies
  - Opamp 1 power is 2X of opamps 2 and 3 (for low noise)

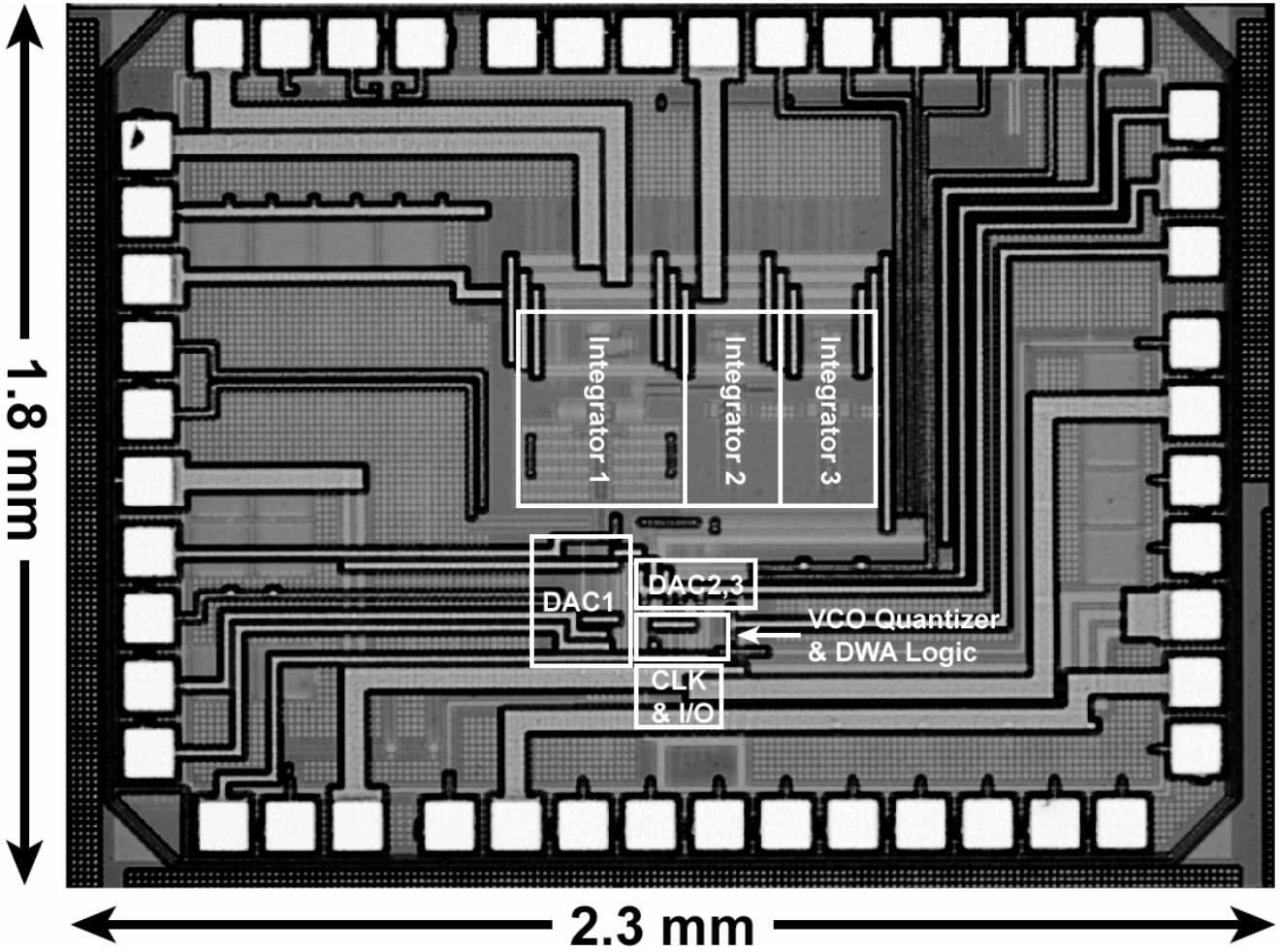
DEM Architecture (3-bit example)



- Achieves low-delay to allow 4-bit DEM at 900 MHz
  - Code through barrel shift propagates in half a sample period

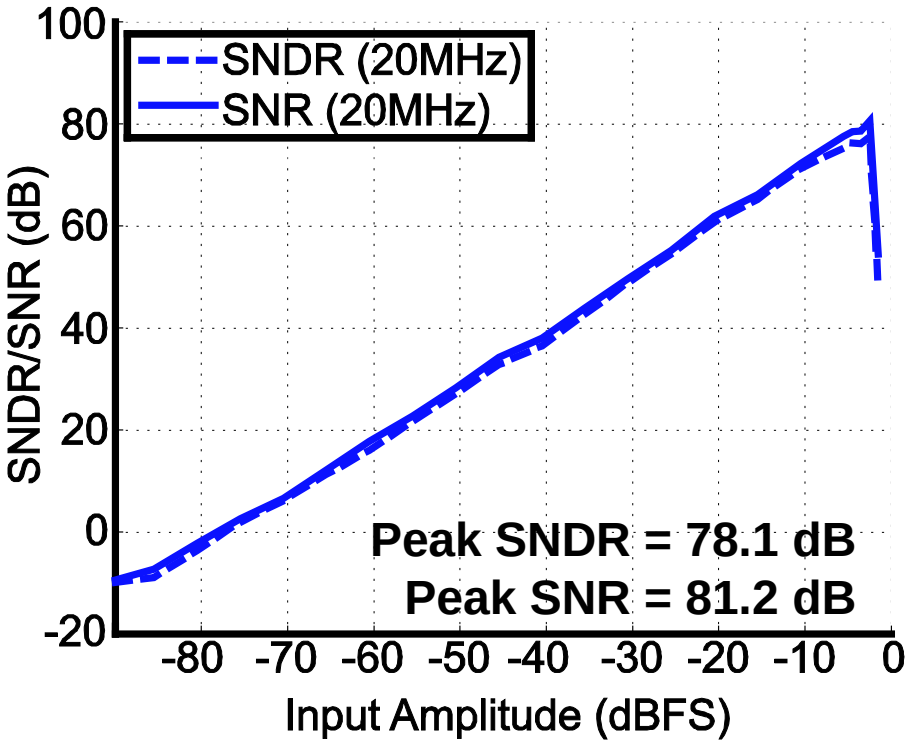
Die Photo (0.13u CMOS)

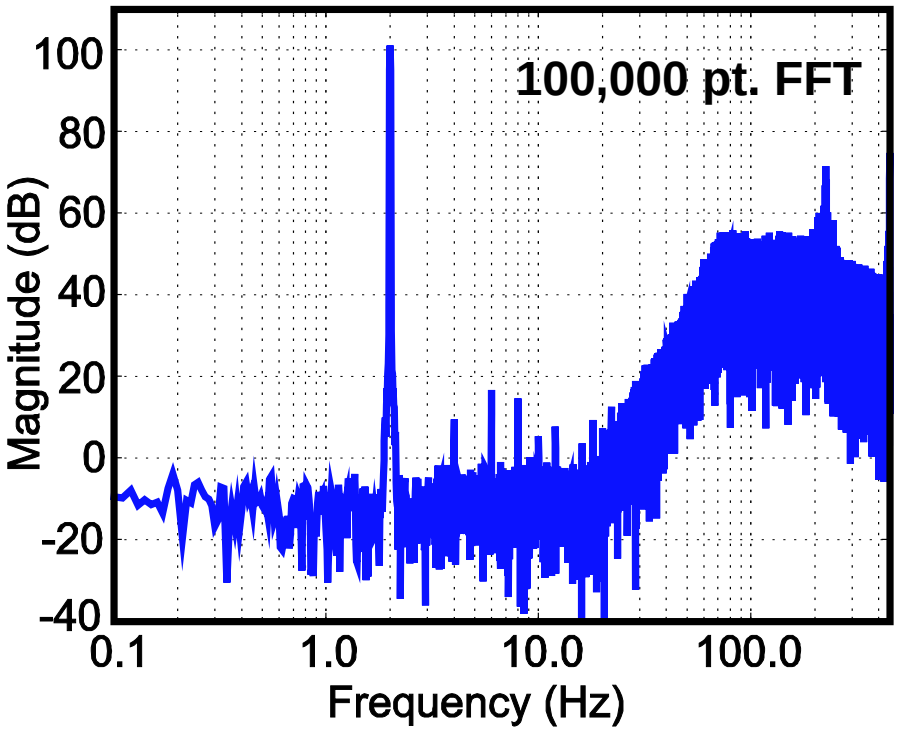
Die photo courtesy of Annie Wang (MTL)



- Active area
  - 0.45 mm^2
- Sampling Freq
  - 900 MHz
- Input BW
  - 20 MHz
- Supply Voltage
  - 1.5 V
- Analog Power
  - 69 mW
- Digital Power
  - 18 mW

Measured Results

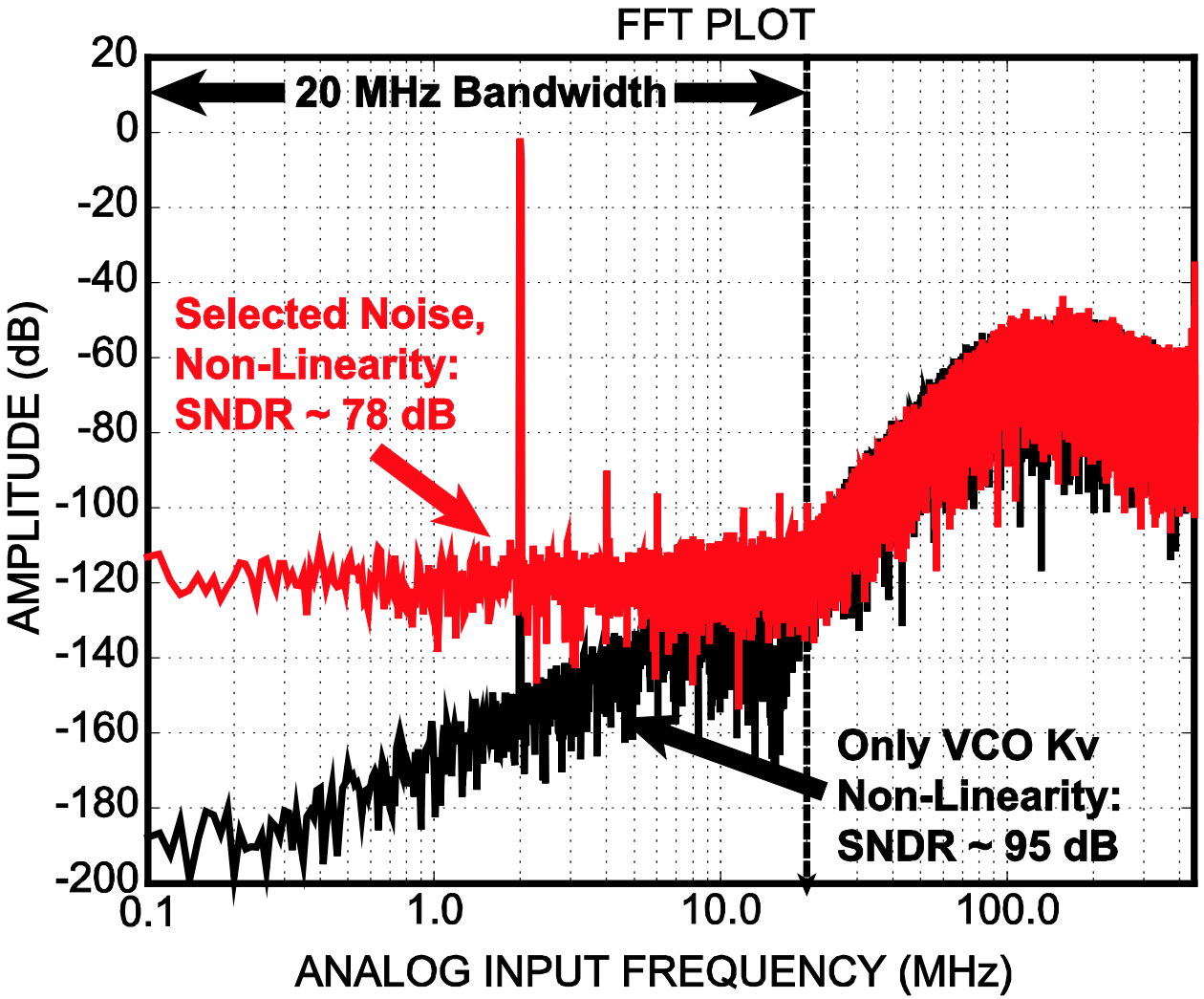




- 78 dB Peak SNDR performance in 20 MHz
  - Bottleneck: transient mismatch from main feedback DAC
- Architecture robust to VCO K_v non-linearity

Figure of Merit: 330 fJ/Conv with 78 dB SNDR

Behavioral Model Reveals Key Performance Issue



- Amplifier nonlinearity degrades SNDR to 81 dB
- DAC transient mismatch degrades SNDR to 78 dB
  - DEM does not help this
  - Could be improved with dual RZ structure

Transient DAC mismatch is likely the key bottleneck

Conclusion

- **VCO-based quantization is a promising component to achieve high performance Σ–Δ ADC structures**
  - **High speed, low power, low area implementation**
  - **First order shaping of quantization noise and mismatch**
  - **K_v non-linearity can be a limitation**

- **Demonstrated a 4th-order CT ΔΣ ADC with a VCO-based integrator and quantizer**
  - **Proposed voltage-to-phase conversion to avoid distortion from Kv non-linearity**
  - **Achieved 78 dB SNDR in 20 MHz BW with 87 mW power**
    - Key performance bottleneck: transient DAC mismatch