Short Course On
Phase-Locked Loops and Their Applications
Day 4, PM Lecture

Examples of Leveraging Digital Techniques in PLLs

Michael Perrott

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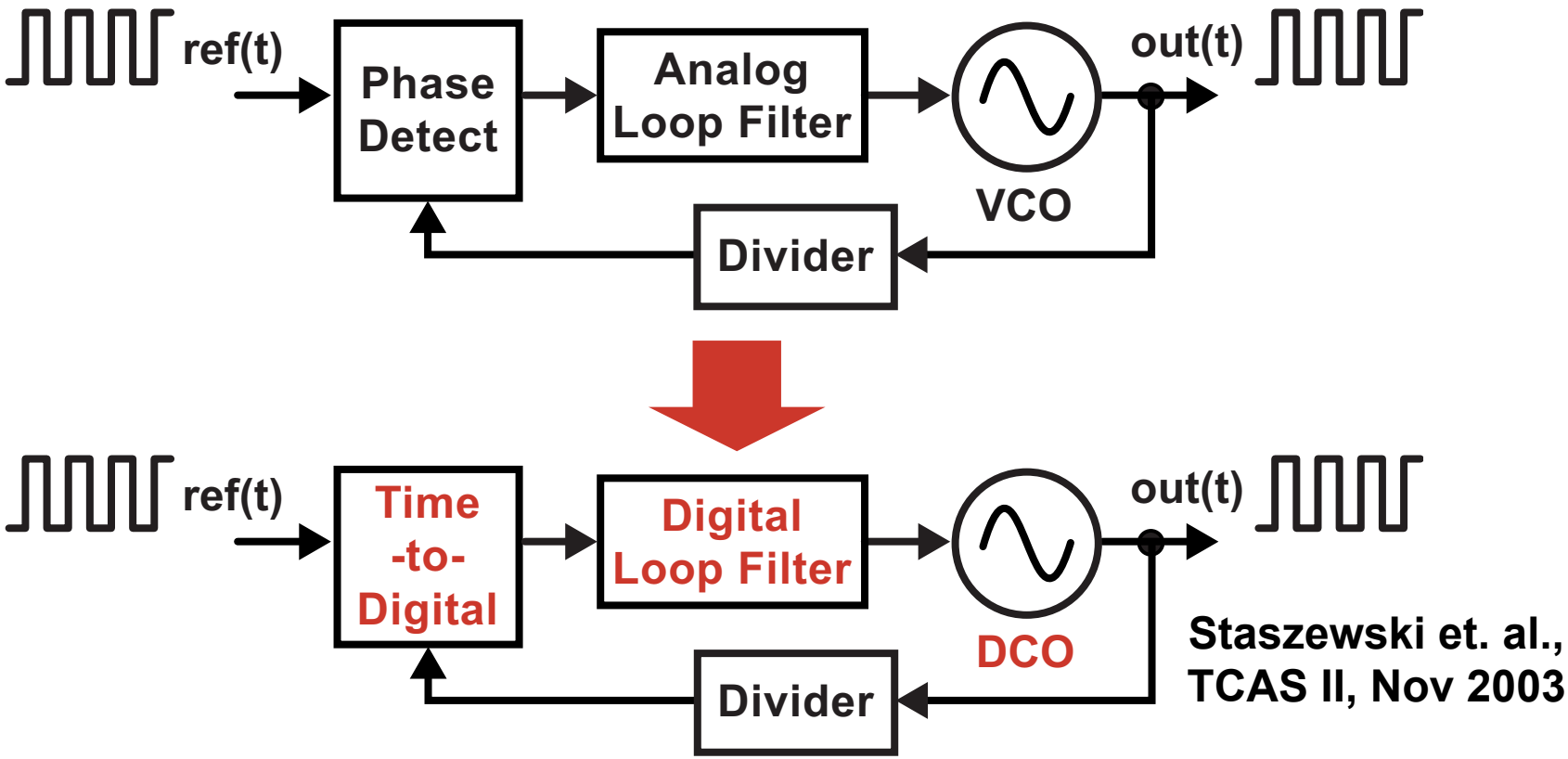
Outline

- Example of high performance digital frequency synthesizer
  - Goal: wide bandwidth (500 kHz) and low phase noise
  - Techniques to achieve low implementation complexity
- Example of high performance mixed-signal clock and data recovery
  - Goal: low jitter and full integration with compact area
  - Techniques to achieve low implementation complexity

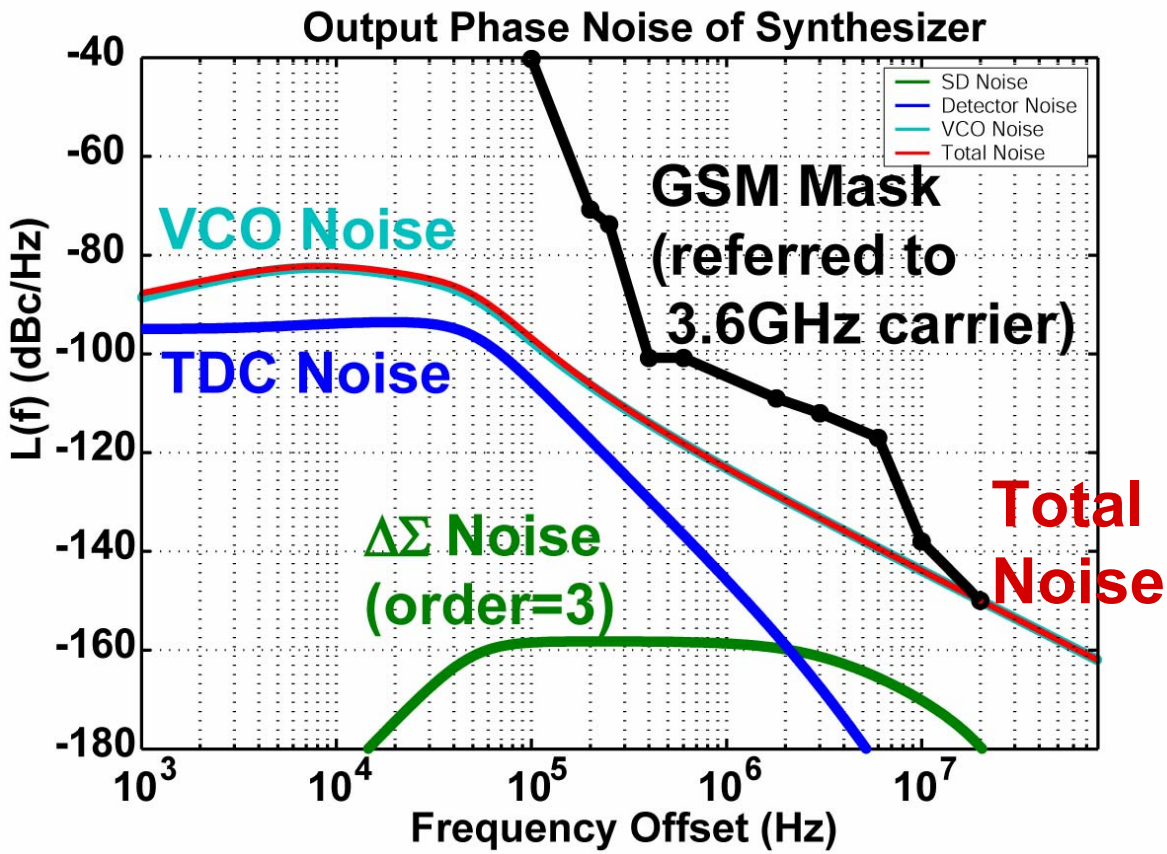
Going Digital …



- Digital loop filter: compact area, insensitive to leakage
- Challenges:
  - Time-to-Digital Converter (TDC)
  - Digitally-Controlled Oscillator (DCO)

Examine Noise Performance: Narrow-Bandwidth Case

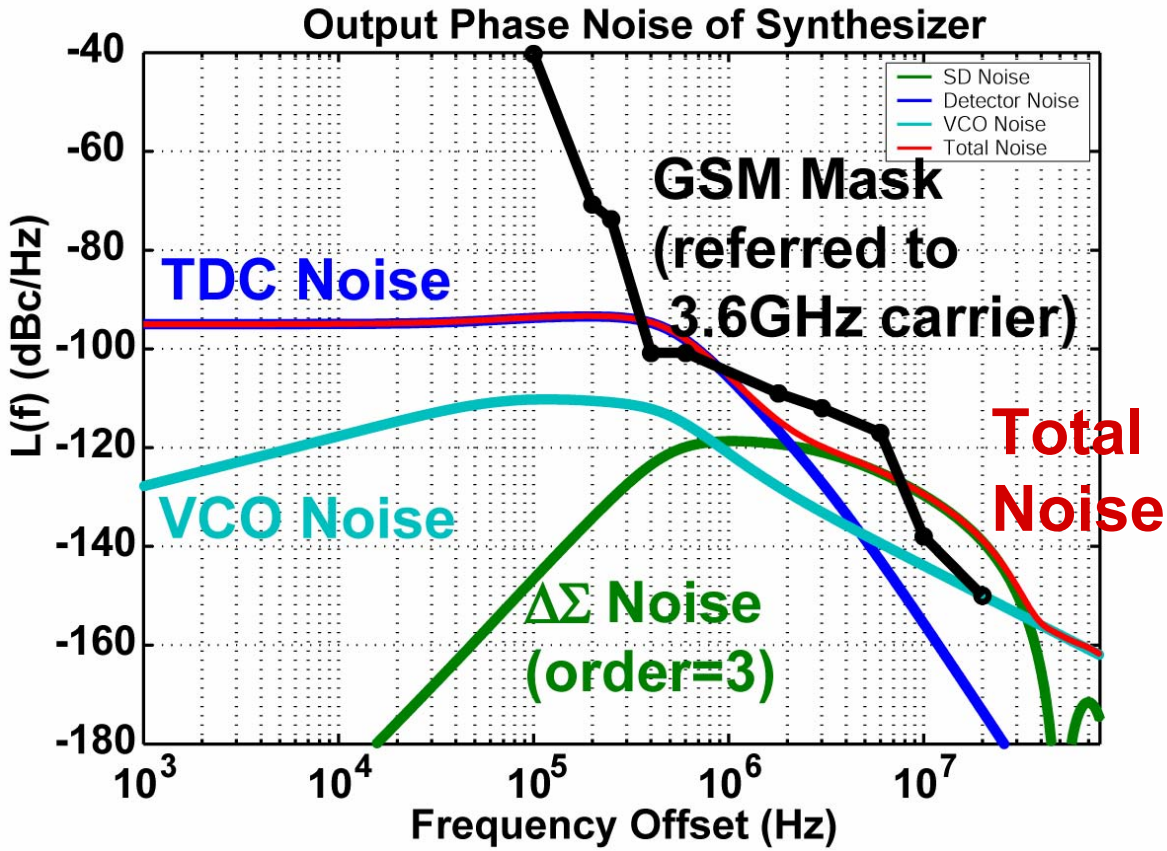
- **Assumptions:**
  - delay = 20ps
  - carrier freq. = 3.6GHz
  - reference freq. = 50MHz
  - PLL BW = 50kHz
  - 3rd order ΔΣ



- VCO noise dominates performance everywhere …
- Don't need very high TDC resolution
- Δ–Σ fractional-N quantization noise is not an issue

Examine Noise Performance: Wide-Bandwidth Case

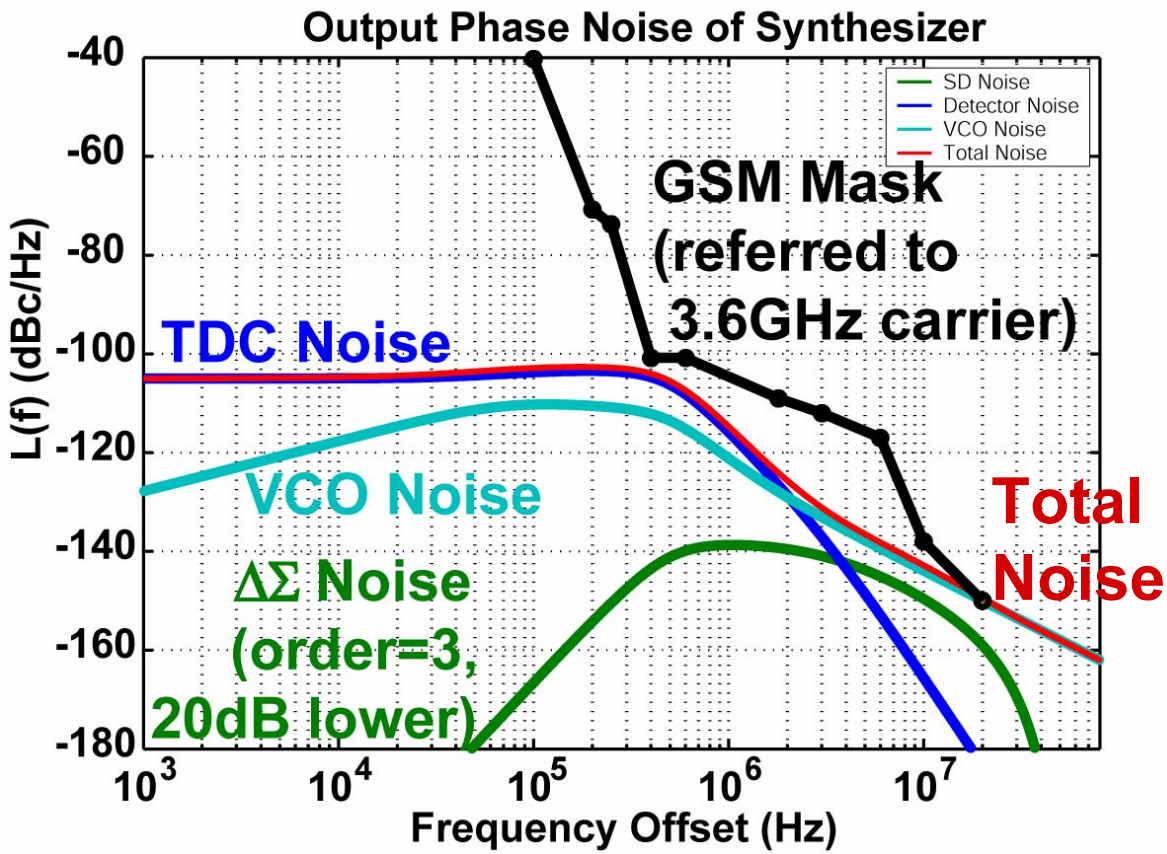
- **Assumptions:**
  - delay = 20ps
  - carrier freq. = 3.6GHz
  - reference freq. = 50MHz
  - PLL BW = 500kHz
  - 3rd order ΔΣ



- **Noise dominated by TDC at low frequencies**
- **Noise dominated by ΔΣ fractional-N noise at high frequencies**

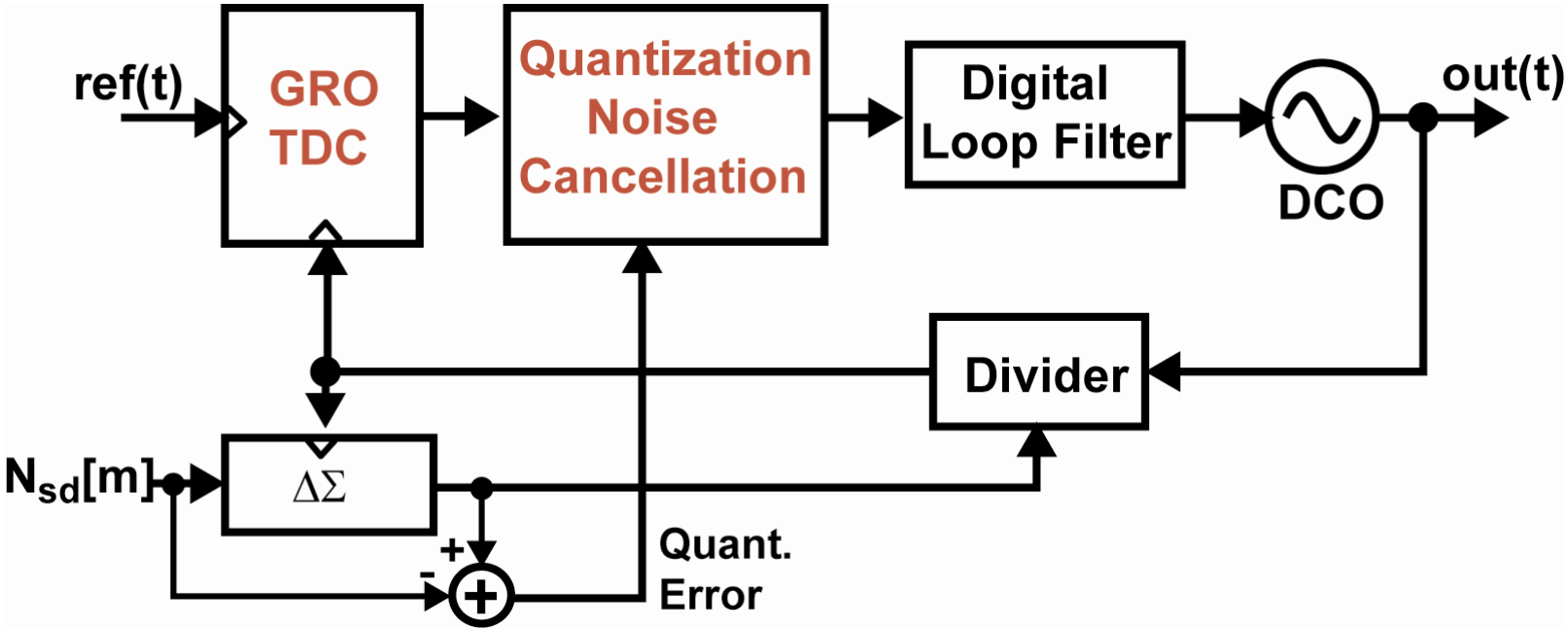
To Meet High Performance Applications like GSM….

- **Assumptions:**
  - delay = 6ps
  - carrier freq. = 3.6GHz
  - reference freq. = 50MHz
  - PLL BW = 500kHz
  - 3rd order ΔΣ (20dB lower)



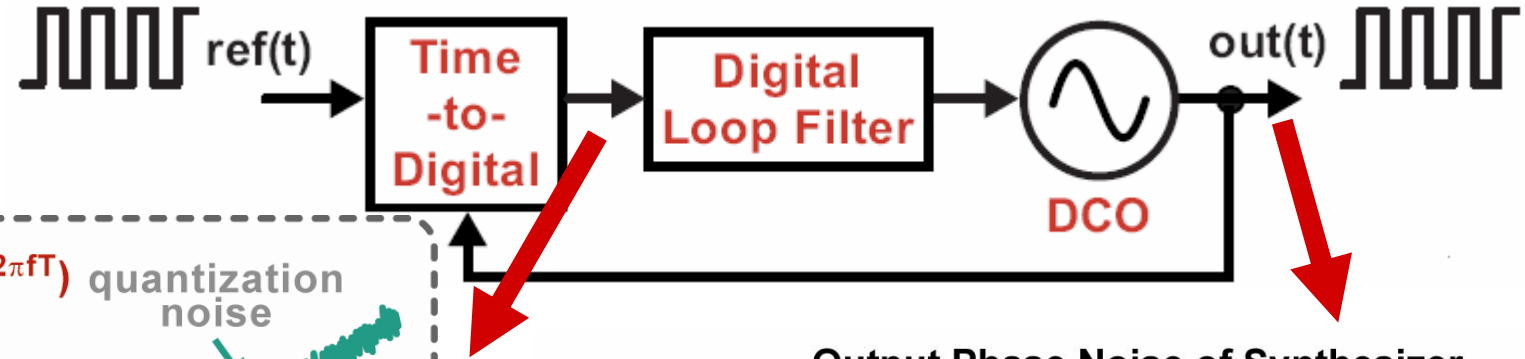
Need *6-ps* TDC resolution and *20dB* cancellation of Δ–Σ fractional-N noise to achieve 500kHz bandwidth

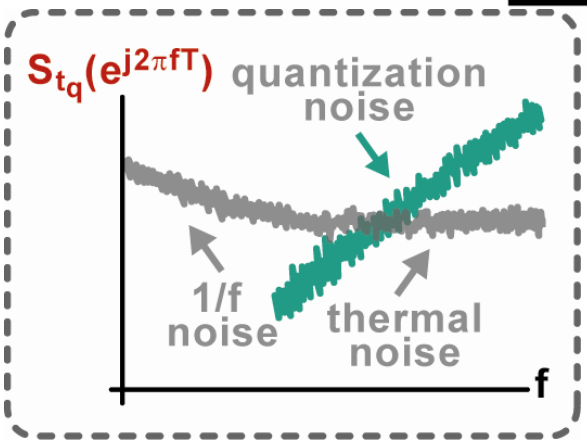
Proposed Digital Wide BW Synthesizer



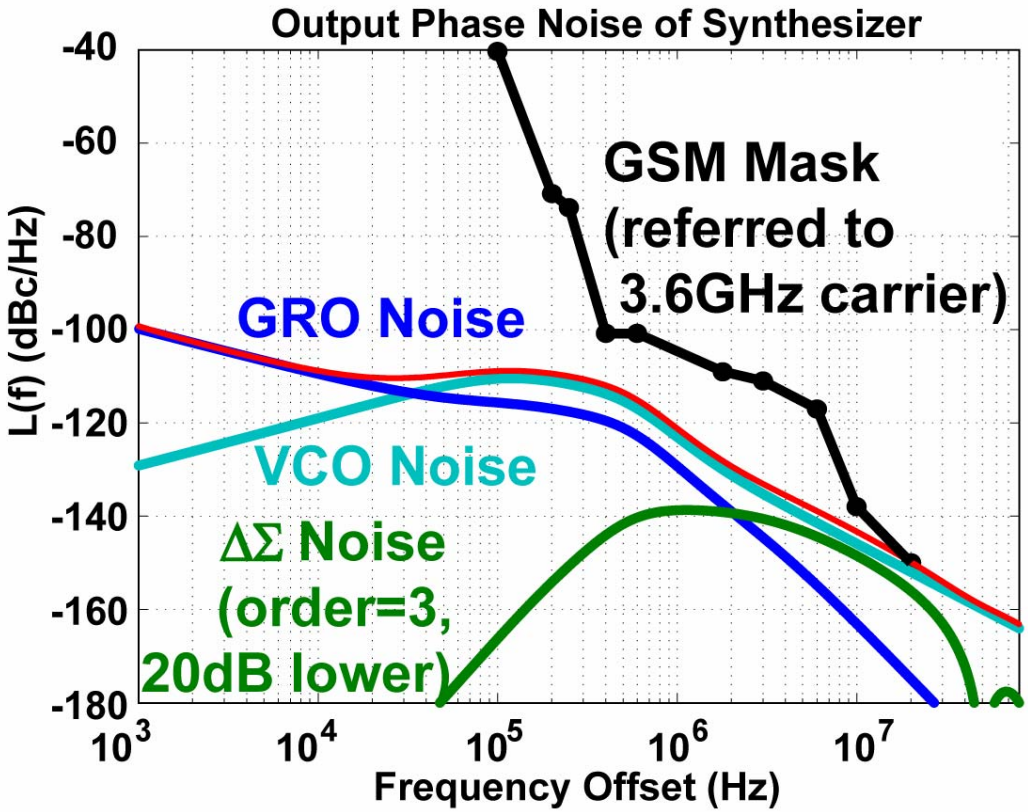
- *Gated-ring-oscillator (GRO) TDC* achieves low in-band noise
- *All-digital quantization noise cancellation* achieves low out-of-band noise
- Design goals:
  - 3.6-GHz carrier, 500-kHz bandwidth
  - <-100dBc/Hz in-band, <-150 dBc/Hz at 20 MHz offset

Key Enablers: GRO and ΔΣ Frac-N Noise Cancellation

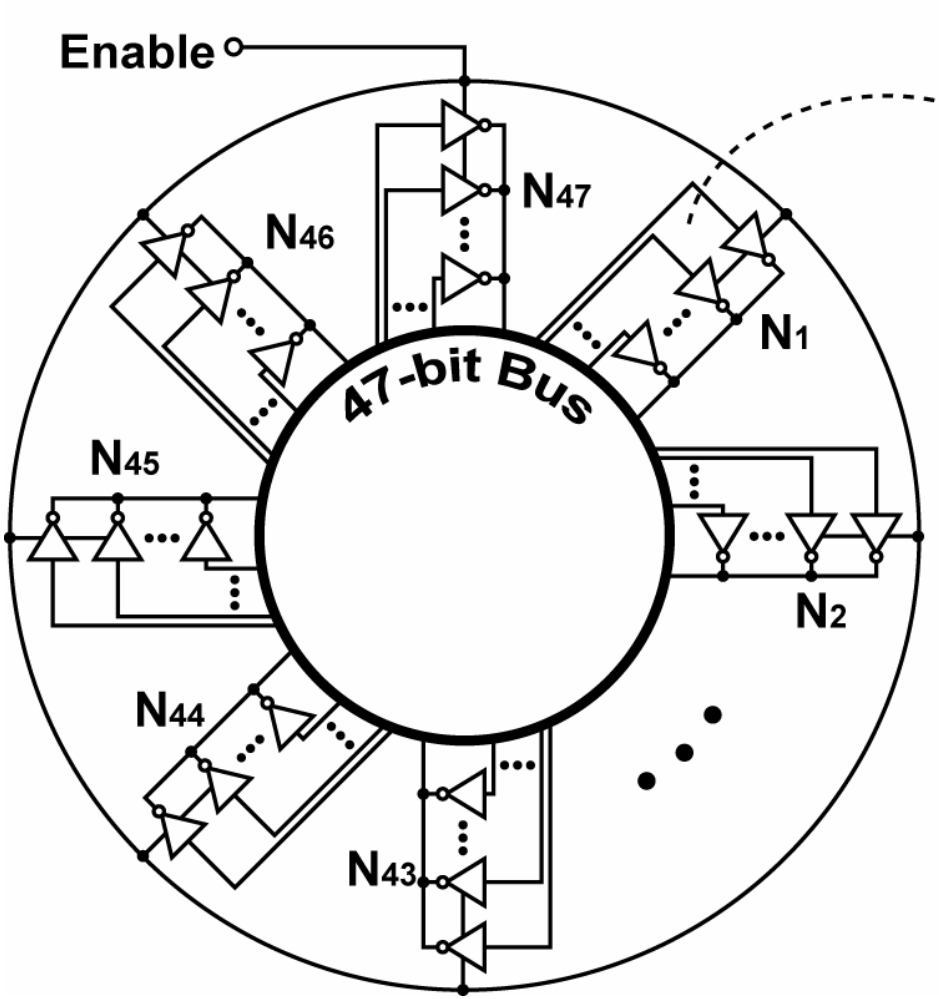


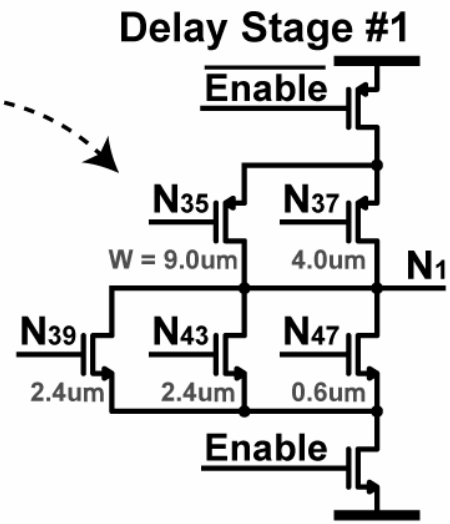


- GRO offers low noise at low frequency offsets
- ΔΣ fractional-N noise cancellation offers low noise at high frequency offsets



Proposed Multi-Path GRO TDC

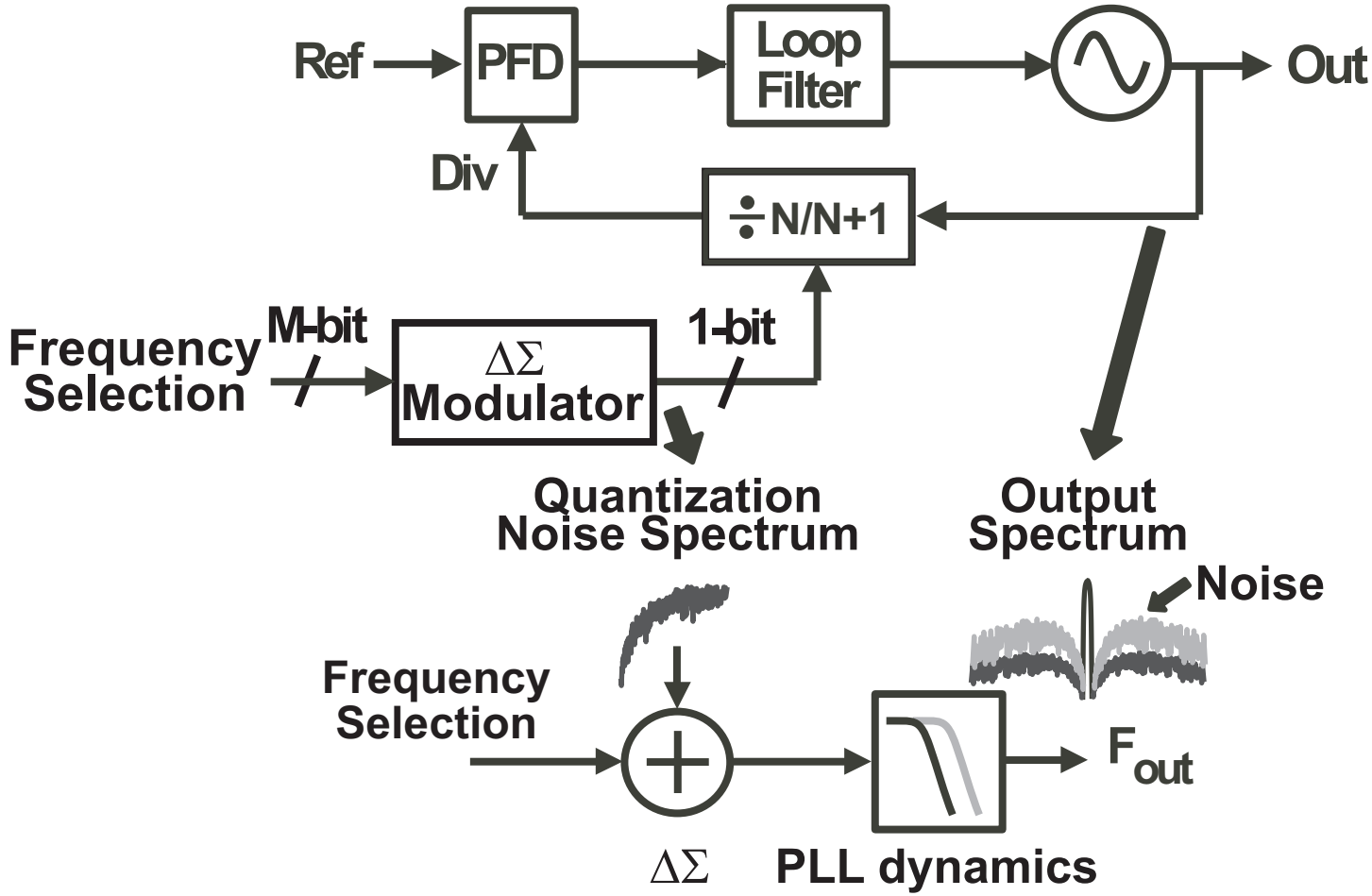




Hsu, Straayer, Perrott
ISSCC 2008

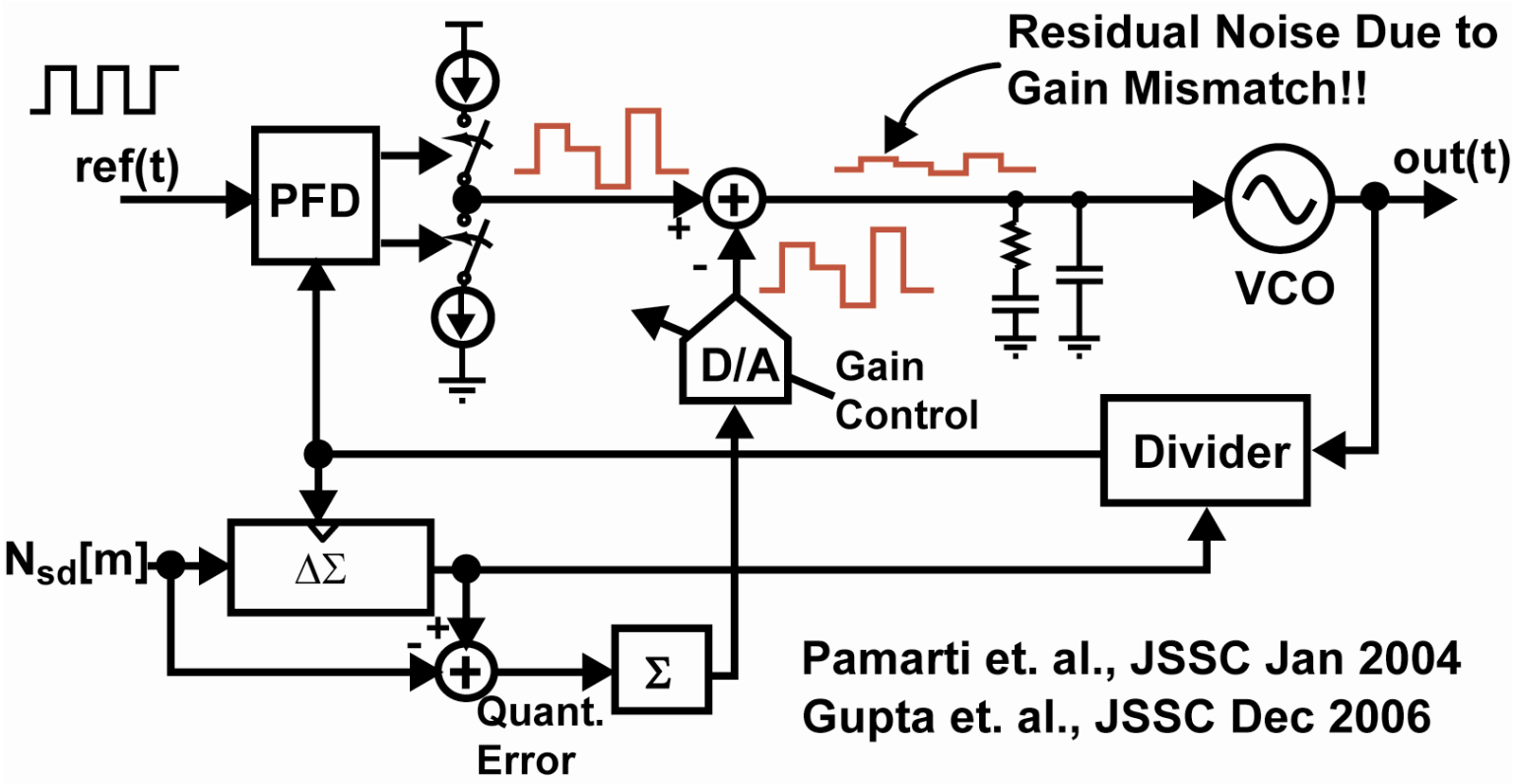
- **Average delay per stage is reduced from 35ps to 6ps**
  - **Noise shaping further improves effective resolution**

Reduction of Fractional-N Quantization Noise



- Increasing PLL bandwidth increases impact of ΔΣ fractional-N noise
  - Cancellation offers a way to counter this effect

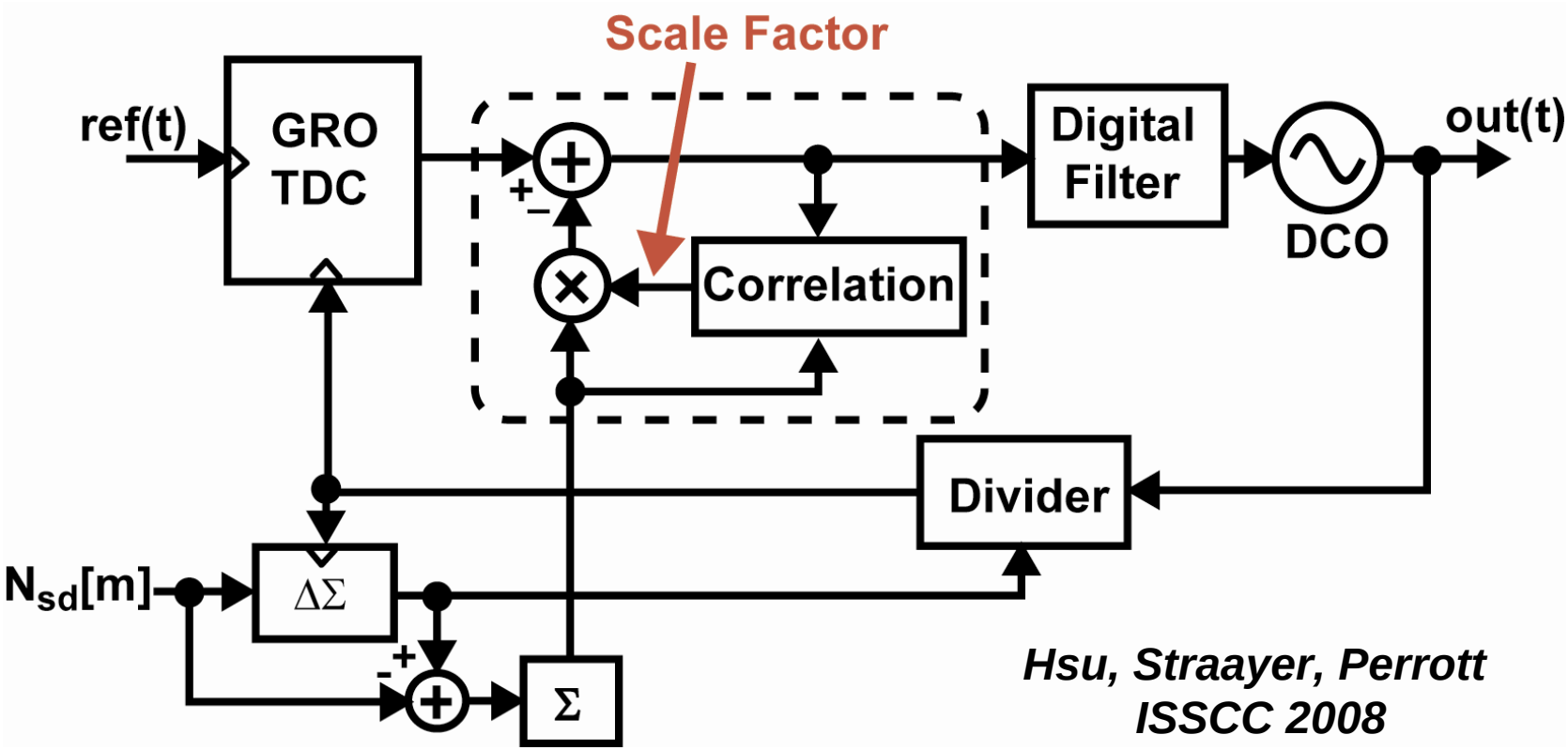
Previous Analog Quantization Noise Cancellation



- Phase error due to ΔΣ is predicted by accumulating ΔΣ quantization error
- Gain matching between PFD and D/A must be precise

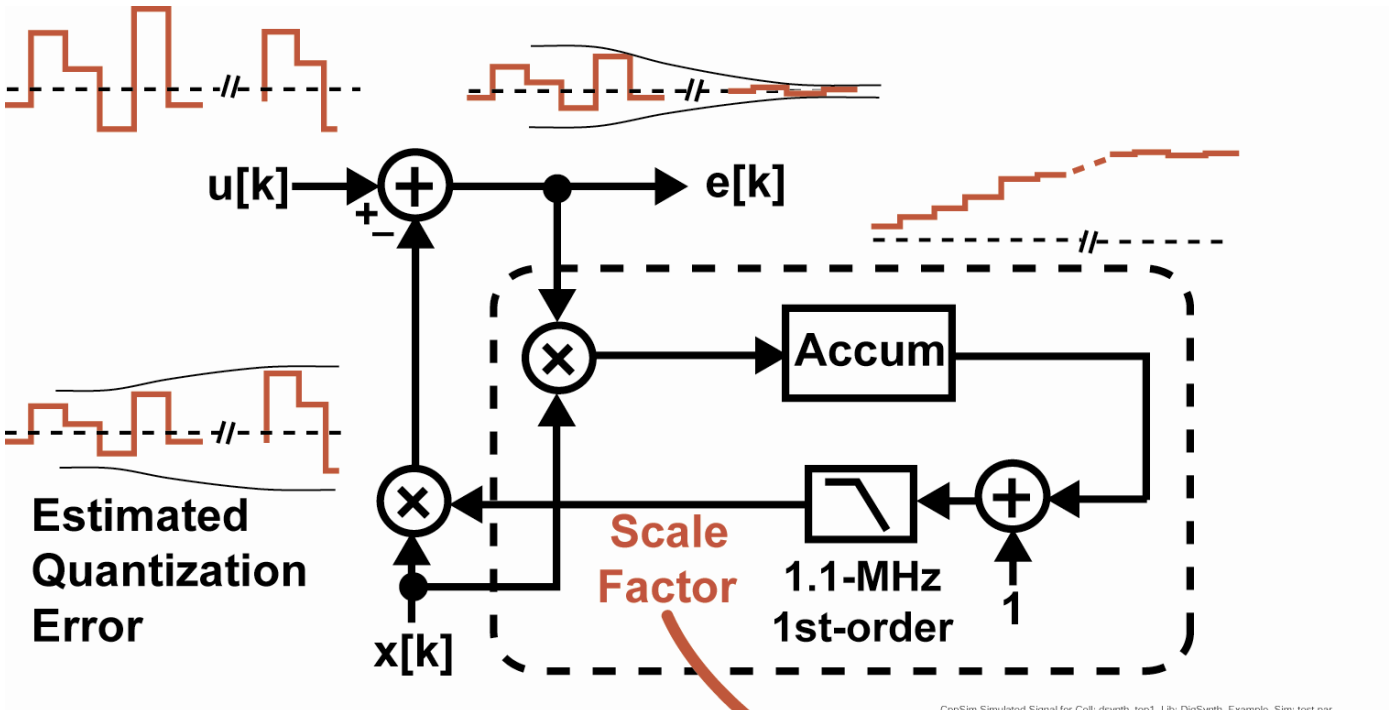
Matching in *analog* domain limits performance

Proposed All-digital Quantization Noise Cancellation



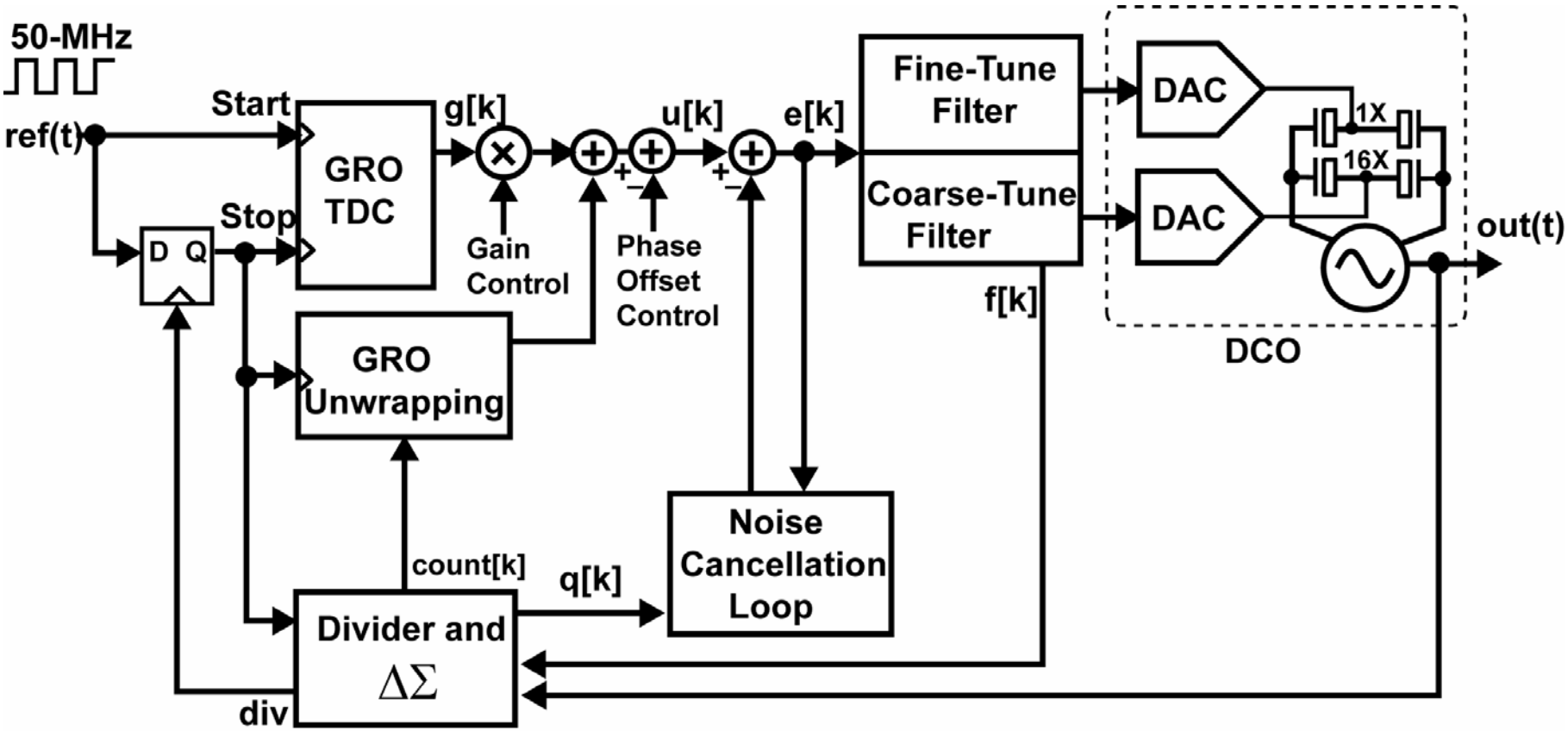
- Scale factor determined by simple digital correlation
- Analog non-idealities such as DC offset are completely eliminated

Details of Proposed Quantization Noise Cancellation



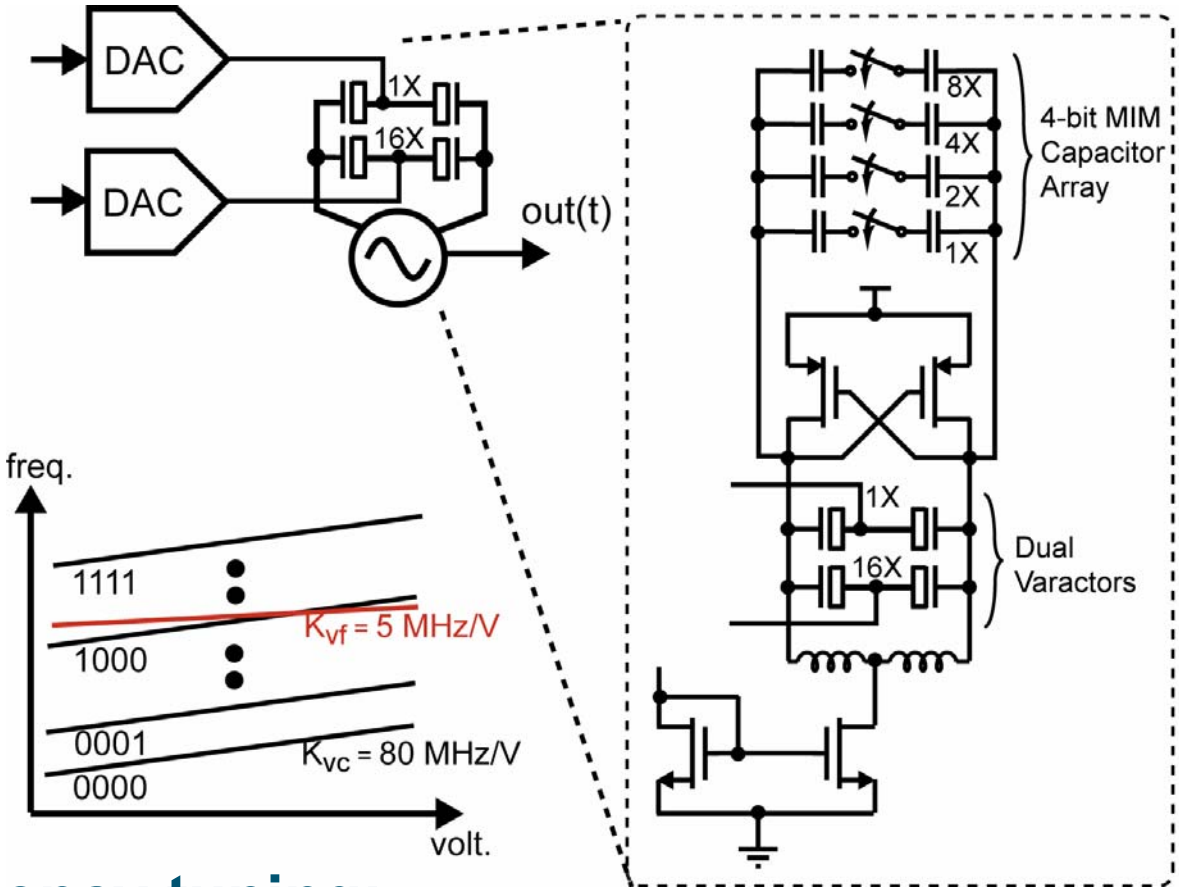
- Correlator out is accumulated and filtered to achieve scale factor
  - Settling time chosen to be around 10 us
- See *analog* version of this technique in *Swaminathan et.al., ISSCC 2007*

Overall Synthesizer Architecture



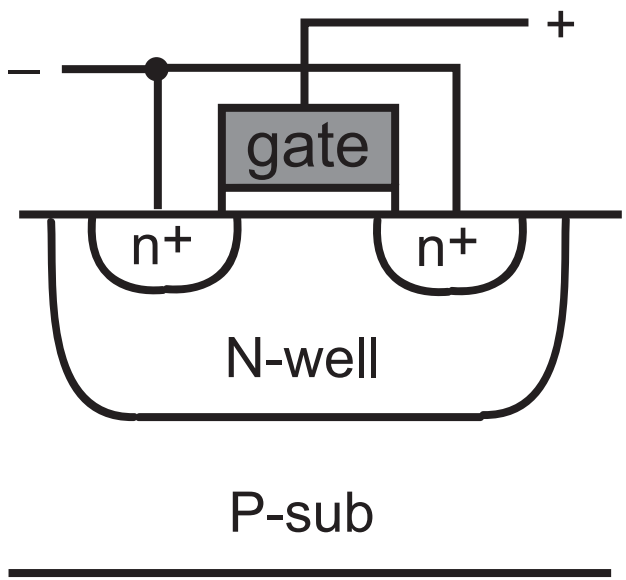
Note: Detailed behavioral simulation model available at http://www.cppsim.com

Dual-Port LC VCO



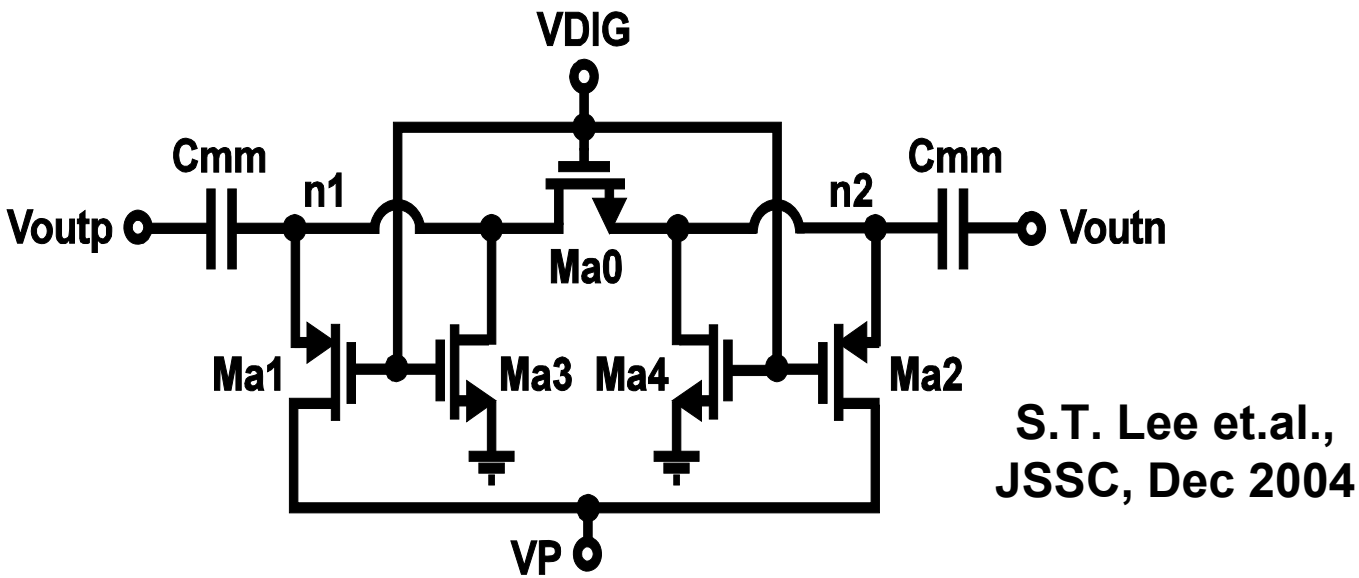
- **Frequency tuning:**
  - Use a small 1X varactor to minimize noise sensitivity
  - Use another 16X varactor to provide moderate range
  - Use a four-bit capacitor array to achieve 3.3-4.1 GHz range

VCO Varactor



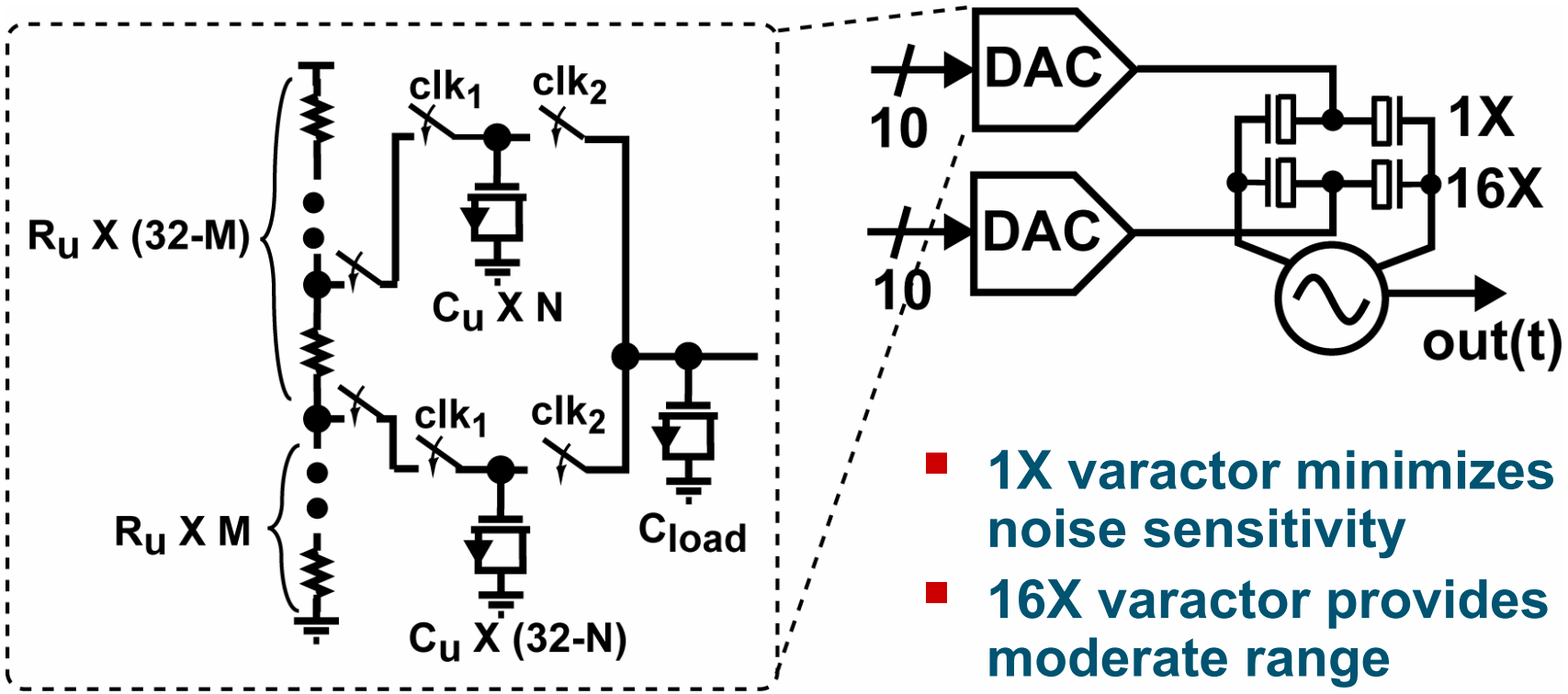
- **Accumulation-mode varactor used for both coarse and fine frequency tuning**
  - **Coarse varactor is 16 times the size of fine varactor**
  - **Provides good ratio of capacitance versus voltage variation with limited supply voltage**

Switched Structure for Coarse Cap Tuning



- **Ma0 provides low differential resistance for caps**
  - **Ma3 and Ma4 provide low bias voltage to minimize Ma0 channel resistance when Ma0 is turned on**
    - Minimizes impact on Q of tank
- **Ma2 provides high bias when Ma0 is turned off**
  - **Keeps voltage at n1 and n2 defined and prevents turn-on of Ma0**

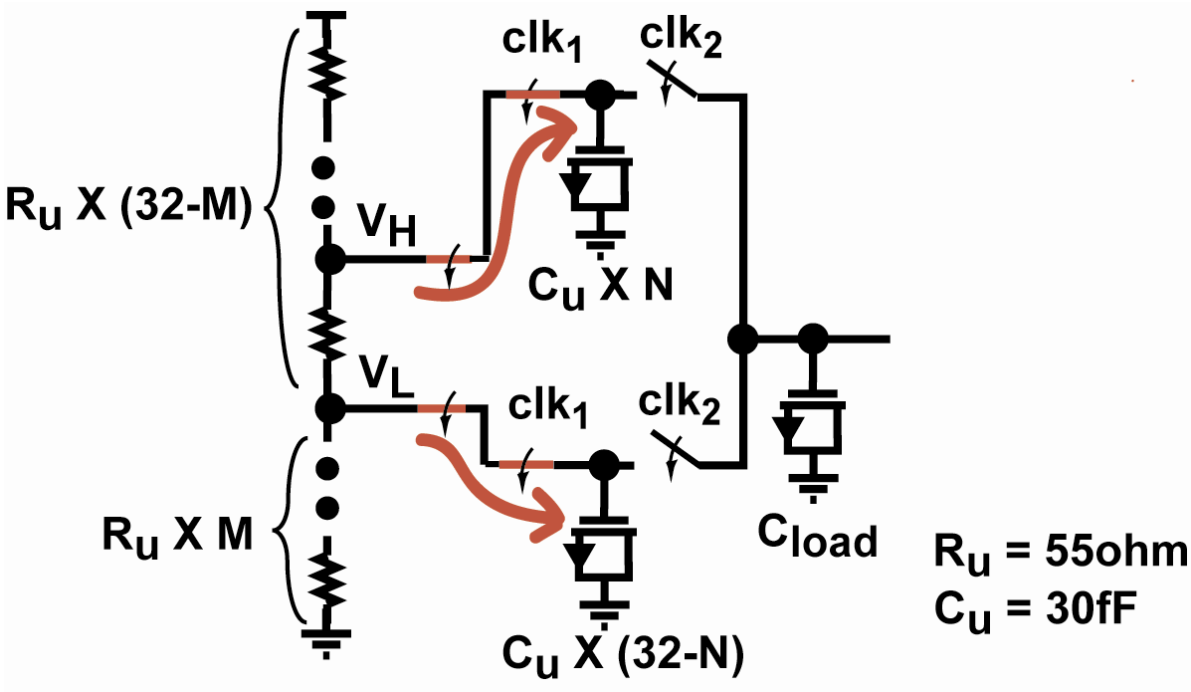
Digitally-Controlled Oscillator with Passive DAC



- 1X varactor minimizes noise sensitivity
- 16X varactor provides moderate range
- A four-bit capacitor array covers 3.3-4.1GHz

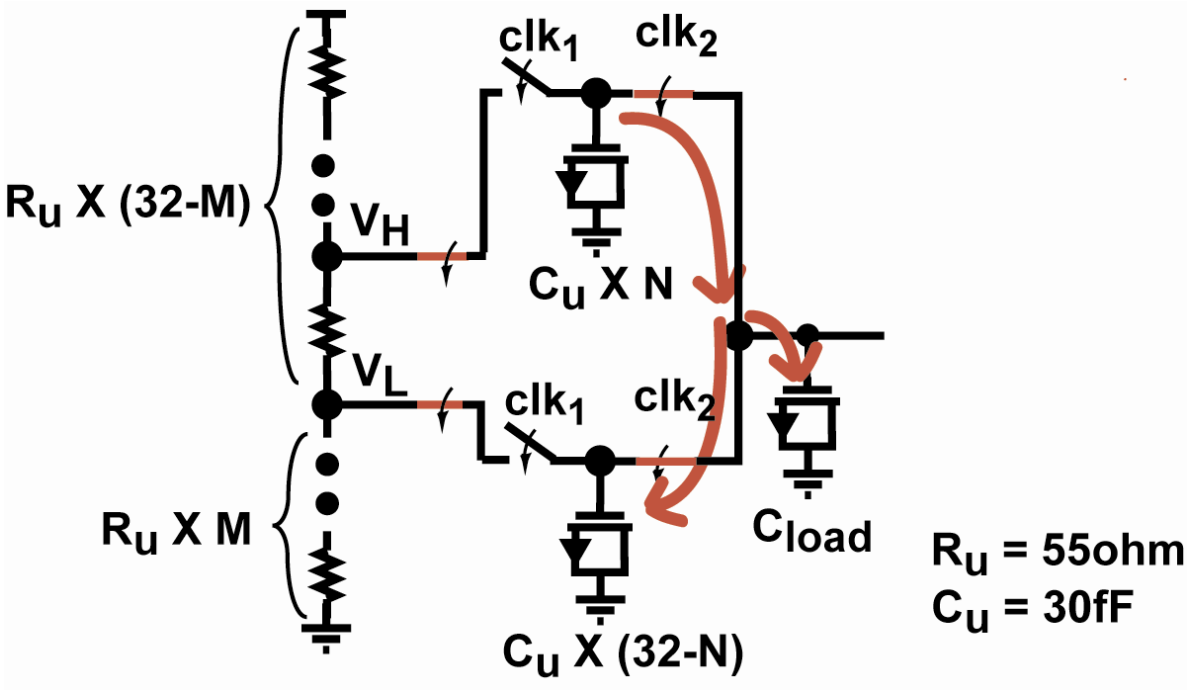
- Goals of 10-bit DAC
  - Monotonic
  - Minimal active circuitry and no transistor bias currents
  - Full-supply output range

Operation of 10-bit Passive DAC (Step 1)



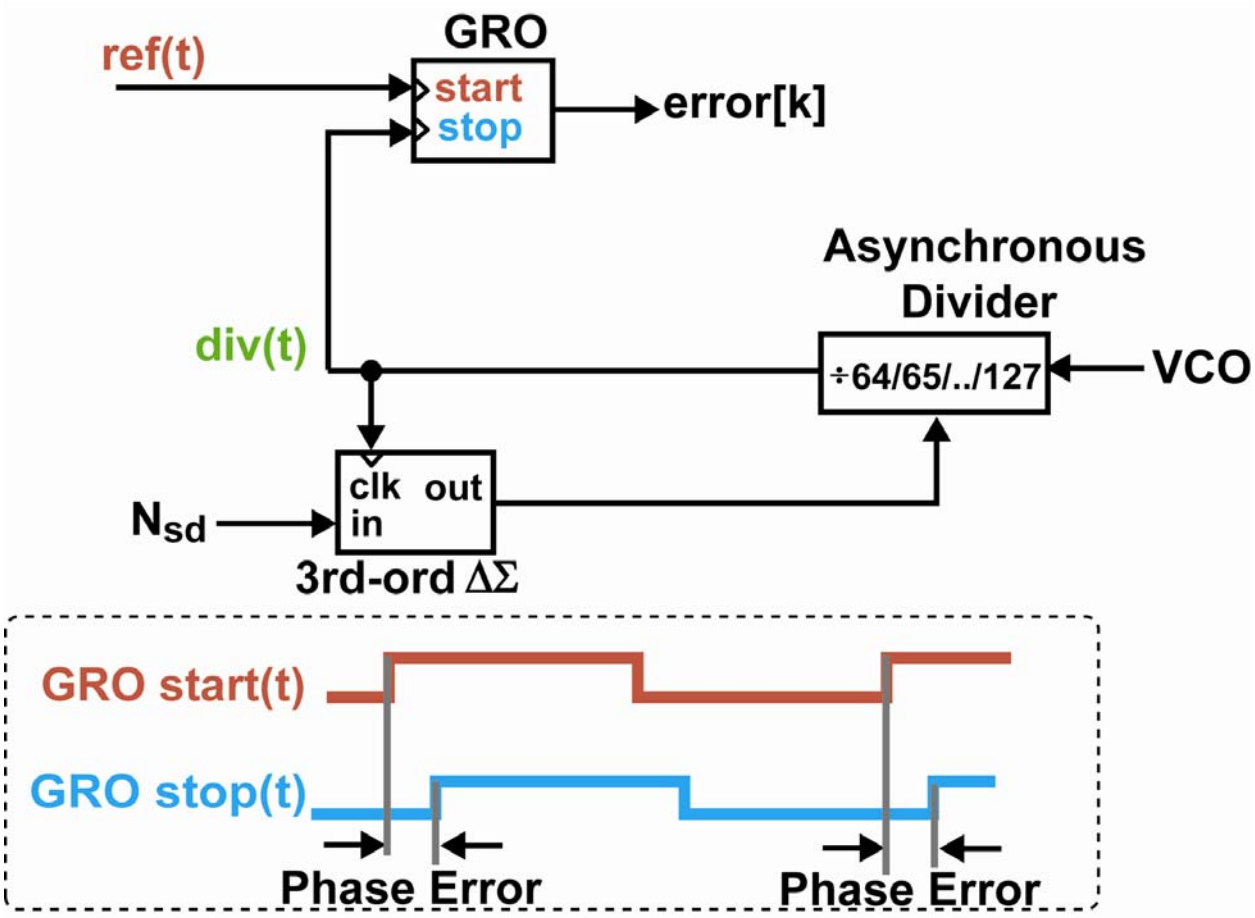
- 5-bit resistor ladder; 5-bit switch-capacitor array
- Step 1: *Capacitors Charged*
  - Resistor ladder forms $V_L = M/32 \cdot V_{DD}$ and $V_H = (M+1)/32 \cdot V_{DD}$, where M ranges from 0 to 31
  - N unit capacitors charged to V_H, and (32-N) unit capacitors charged to V_L

Operation of 10-bit Passive DAC (Step 2)



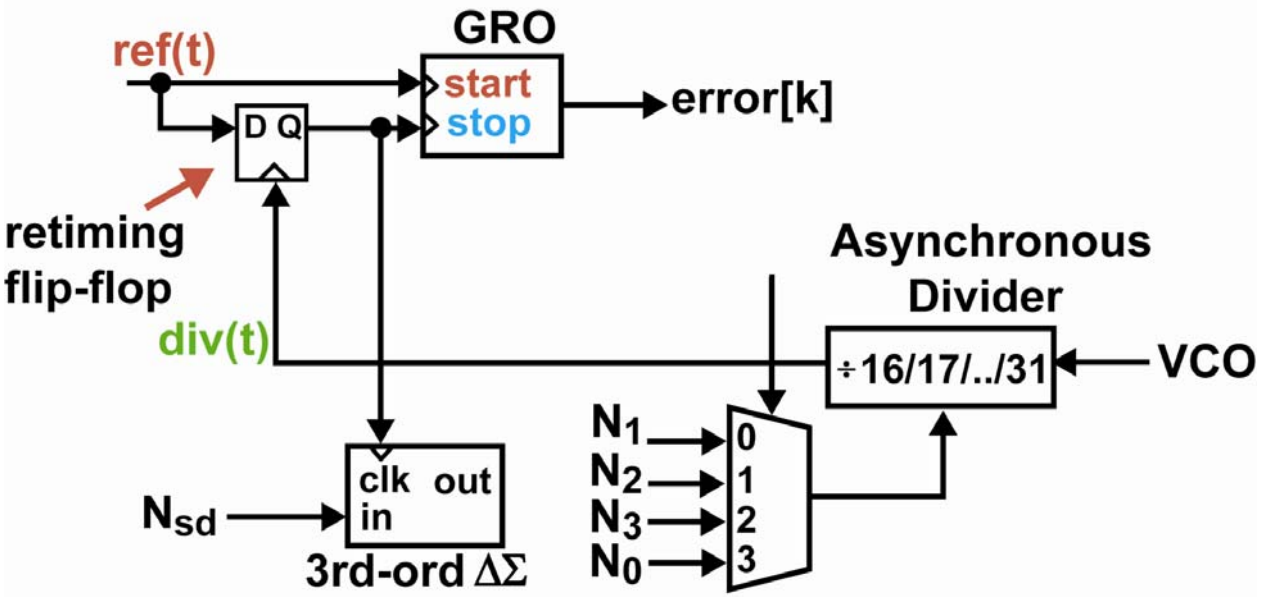
- **Step 2:** ***Disconnect Capacitors from Resistors, Then Connect Together***
  - **Achieves DAC output with first-order filtering**
  - **Bandwidth = 32• C_u/(2π•C_{load})•50MHz**
    - Determined by capacitor ratio
    - Easily changed by using different C_{load}

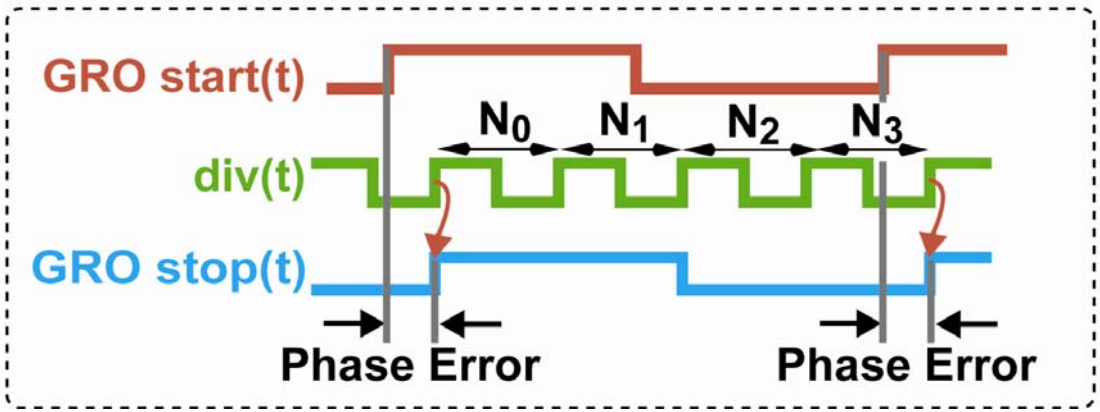
Now Let's Examine Divider …



- **Issues:**
  - GRO range must span entire reference period during initial lock-in

Proposed Divider Structure

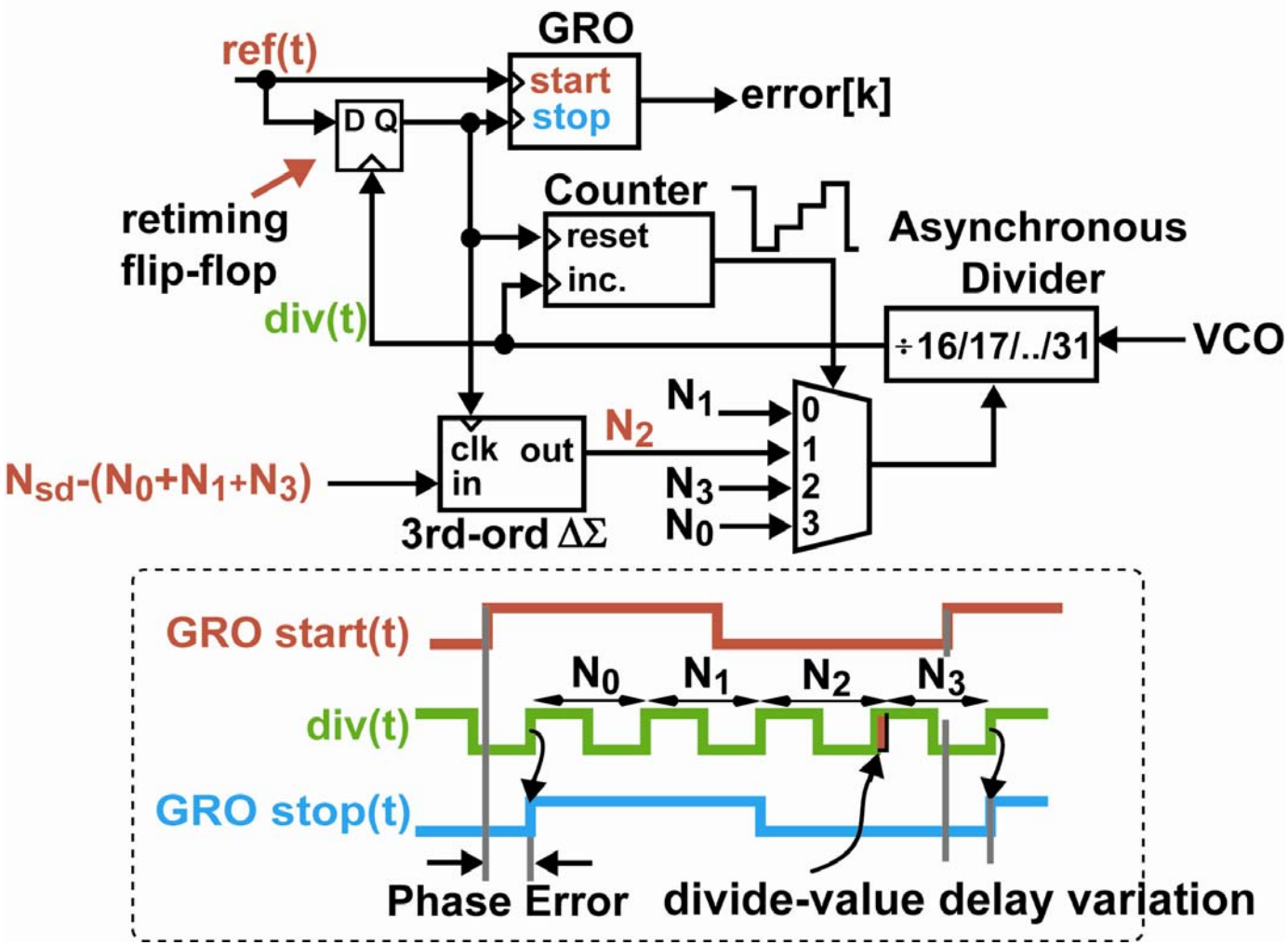




Divide value
$=N_0+N_1+N_2+N_3$

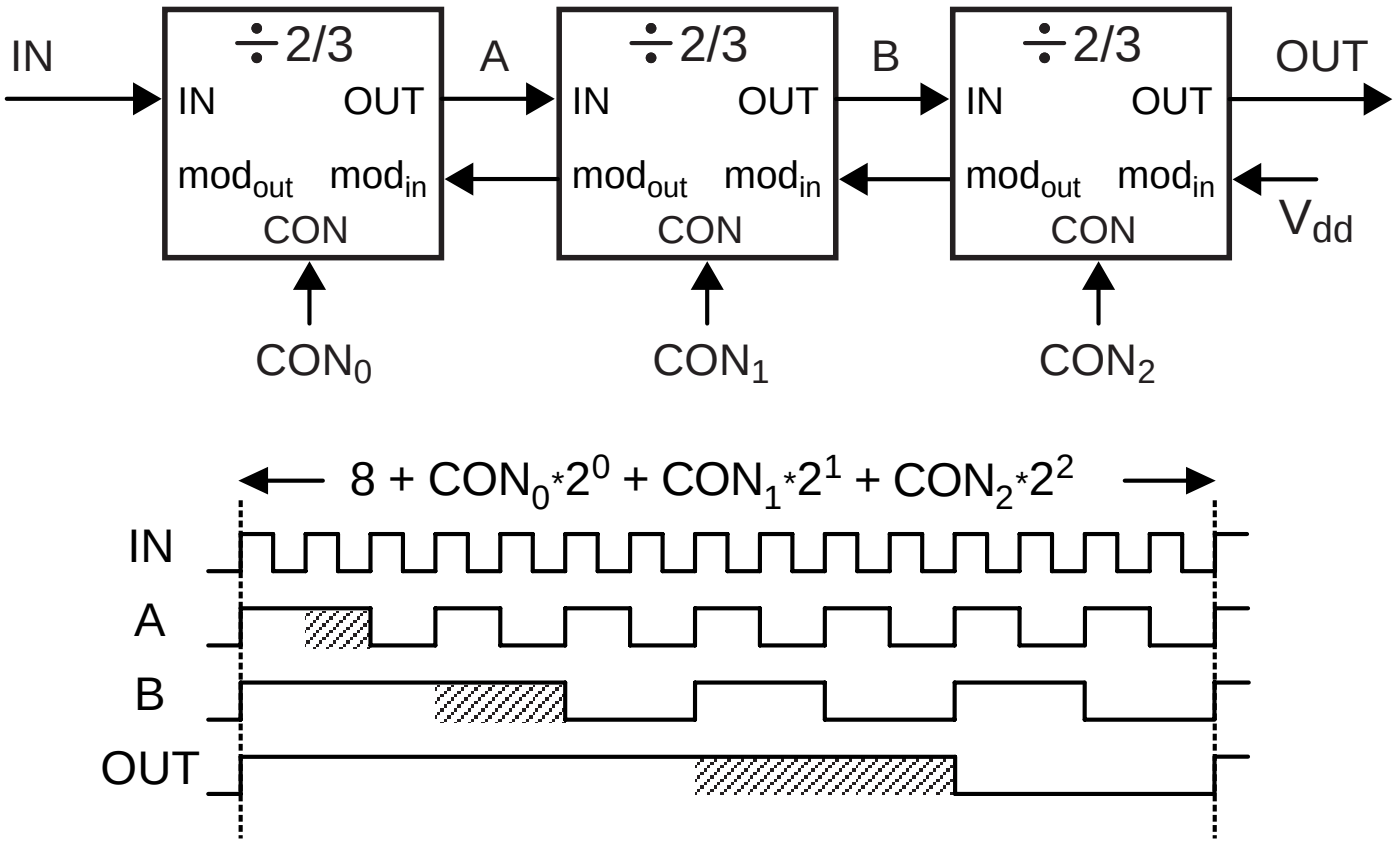
- **Resample reference with 4x division frequency**
  - **Lowers GRO range to one fourth of the reference period**

Proposed Divider Structure (cont'd)



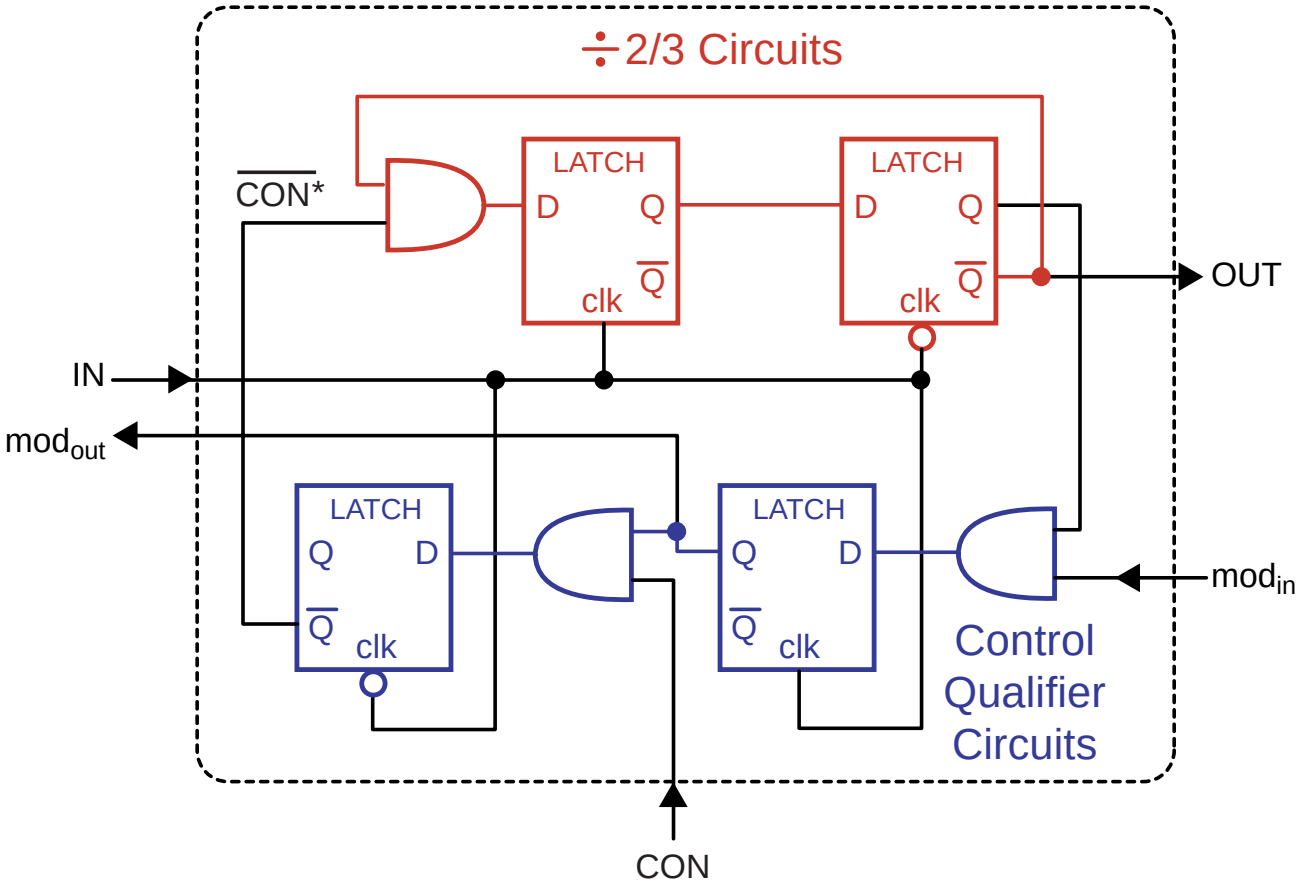
- Place ΔΣ dithered edge away from GRO edge
  - Prevents extra jitter due to divide-value dependent delay

Asynchronous Divider Structure



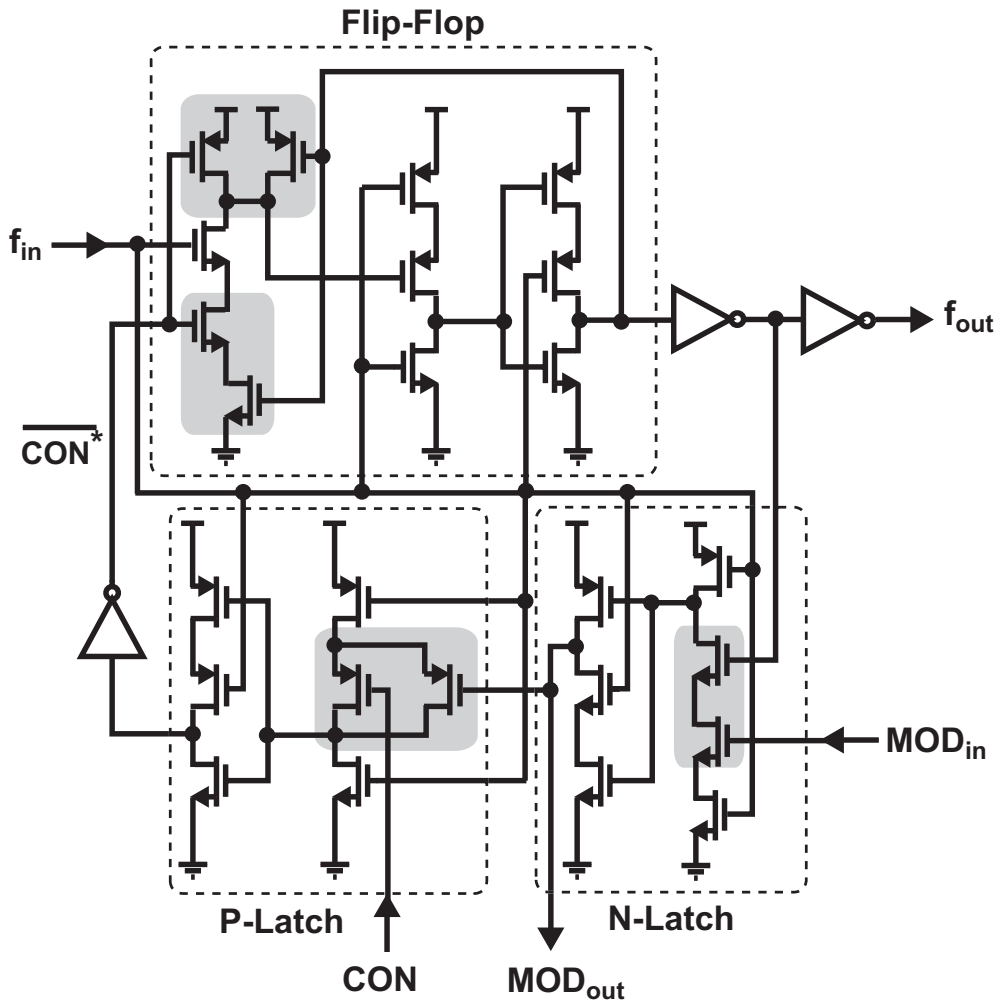
- **Vaucher et. al., "A Family of Low-Power Truly Modular Programmable Dividers …", JSSC, July 2000**

Implementation of 2/3 Sections in Modular Approach



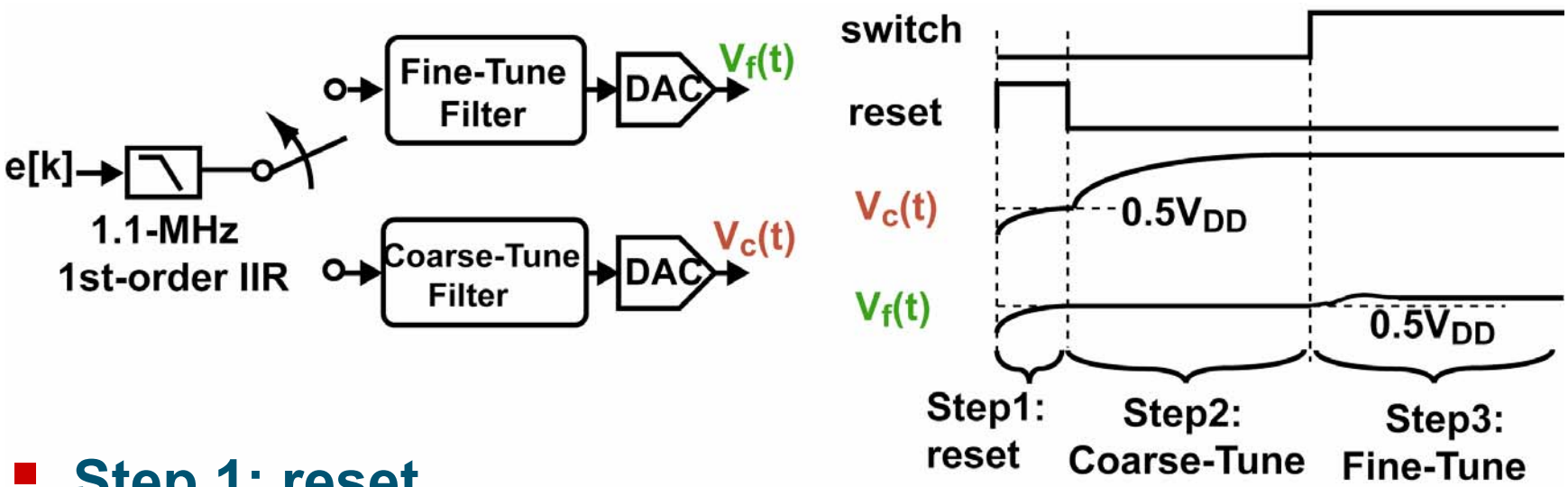
- **Same as discussed on day 2 of this class**

Implementation of 2/3 Section



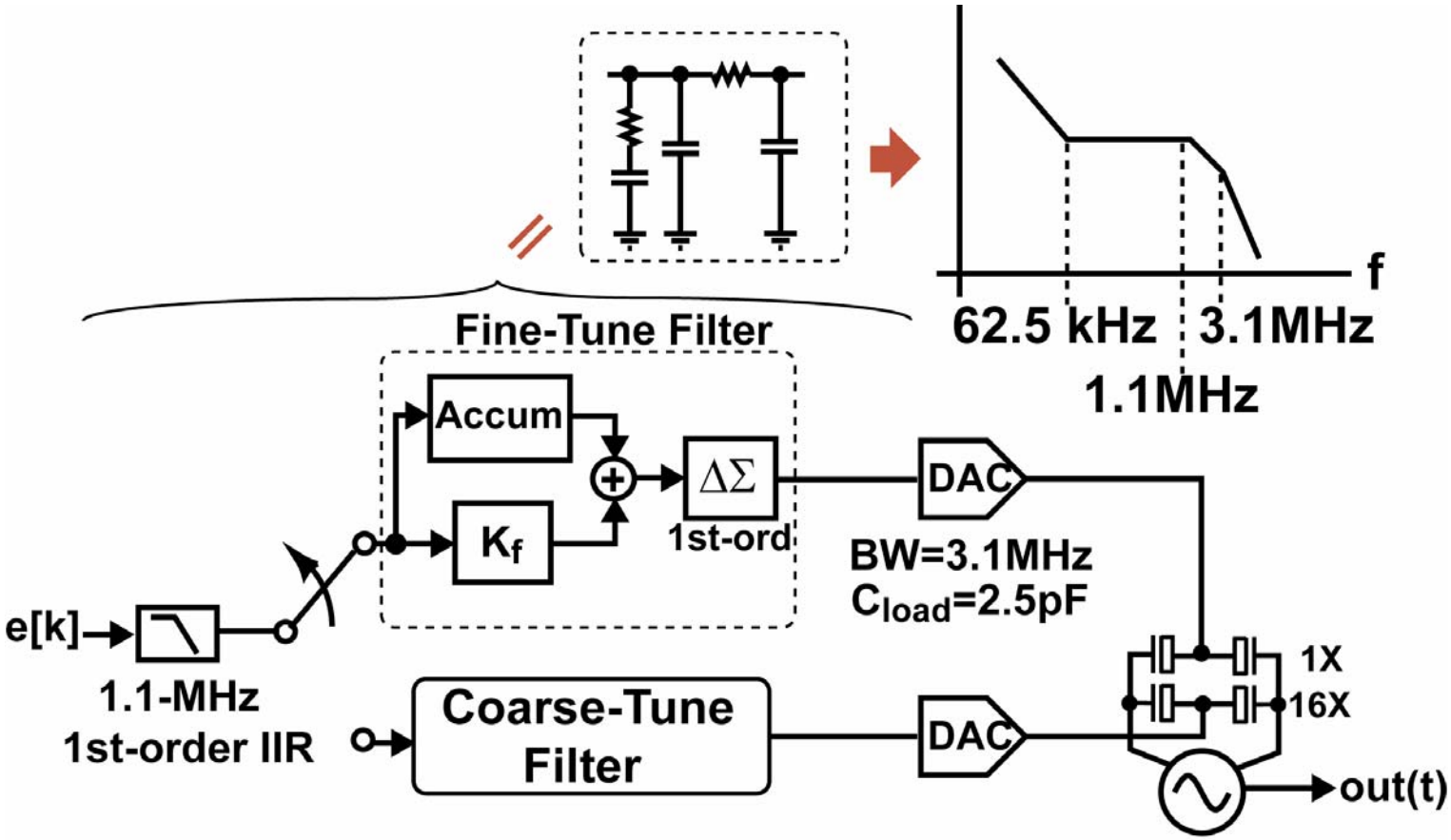
- Combines logic gates into TSPC latches
  - Requires only 1 ma at 3.6 GHz operation in 0.13u CMOS!

Dual-Path Loop Filter



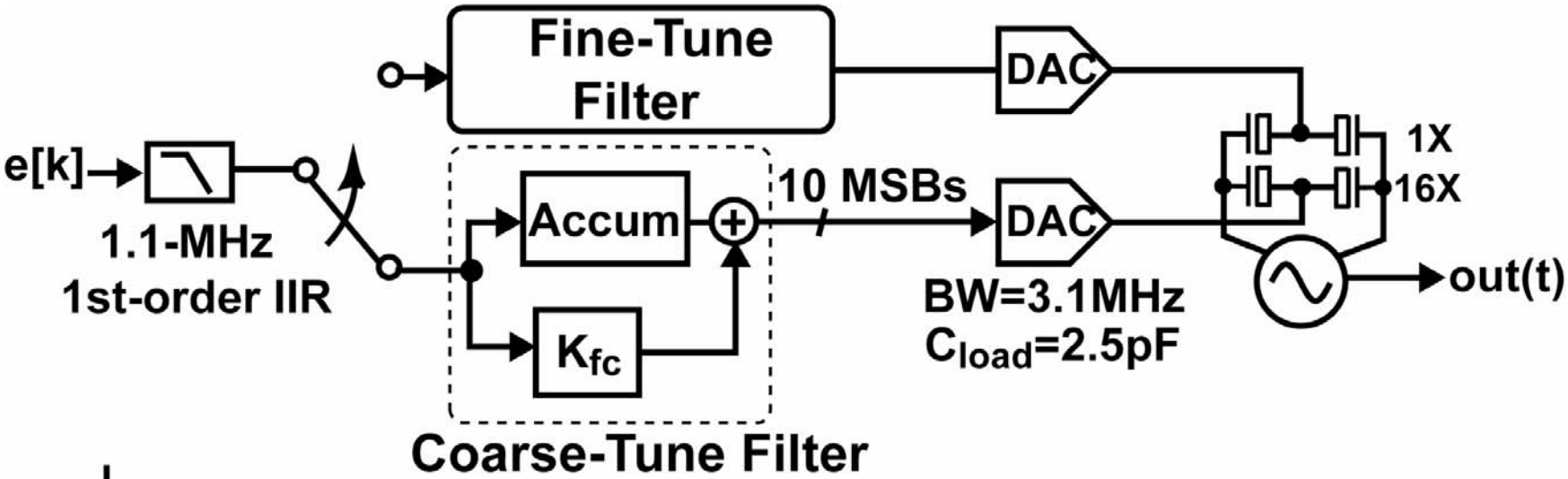
- Step 1: reset
- Step 2: frequency acquisition
  - $V_c(t)$ varies
  - $V_f(t)$ is held at midpoint
- Step 3: steady-state lock conditions
  - $V_c(t)$ is frozen to take quantization noise away
  - ΔΣ quantization noise cancellation is enabled

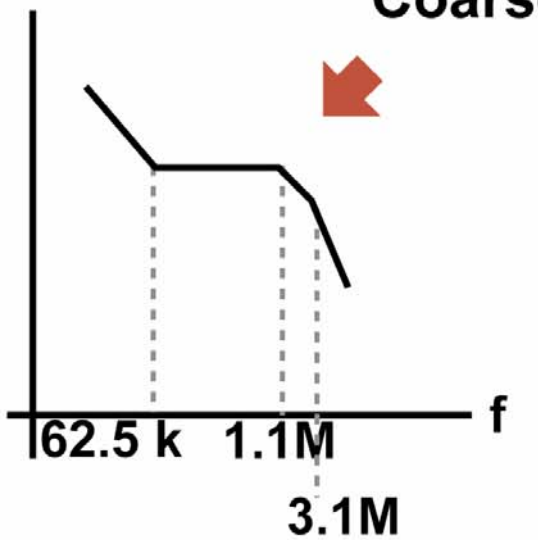
Fine-Path Loop Filter



- Equivalent to an analog lead-lag filter
  - Set zero (62.5kHz) and first pole (1.1MHz) digitally
  - Set second pole (3.1MHz) by capacitor ratio
- First-order ΔΣ reduces in-band quantization noise

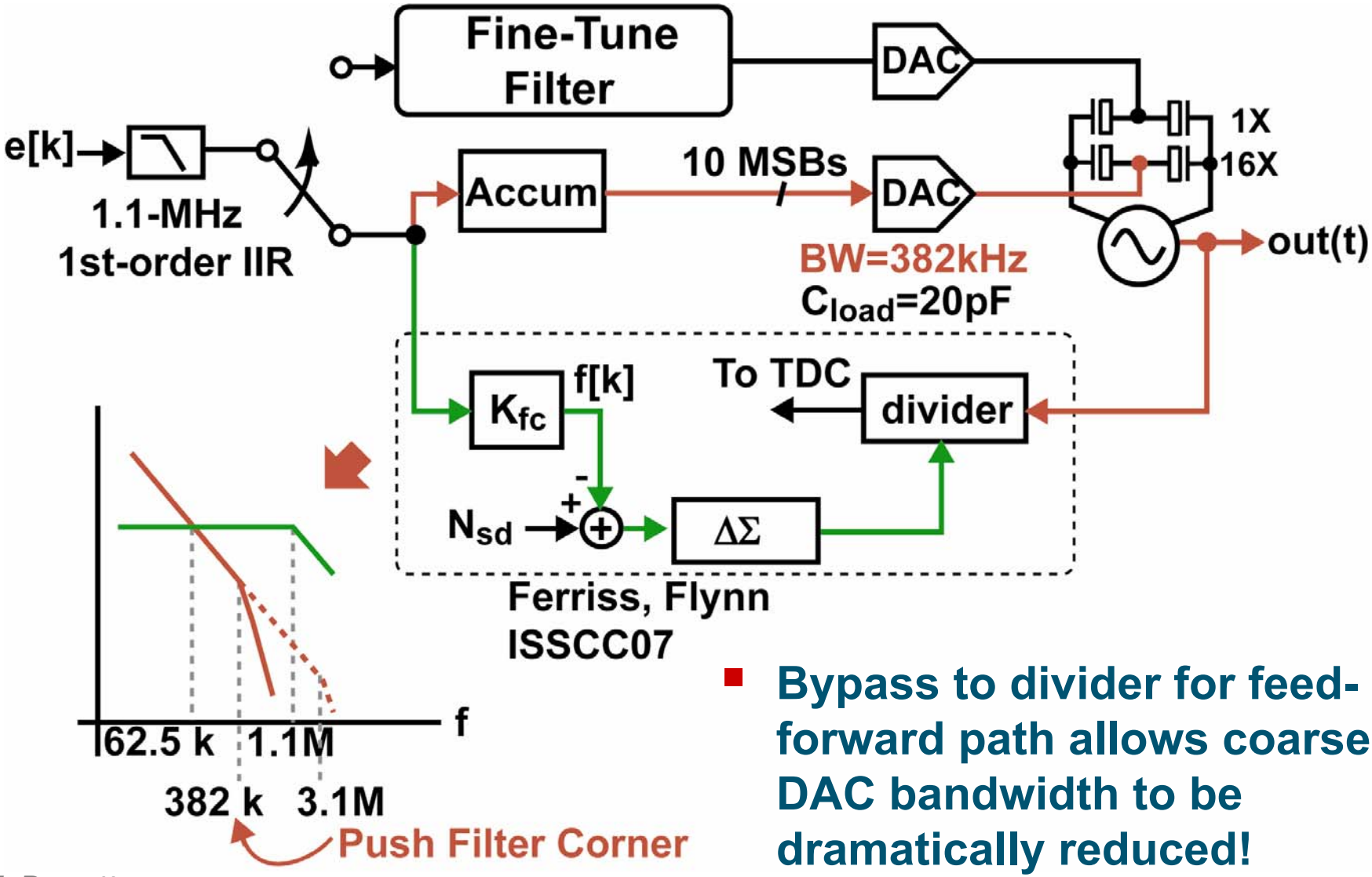
Same Technique Poses Problems for Coarse-Tune





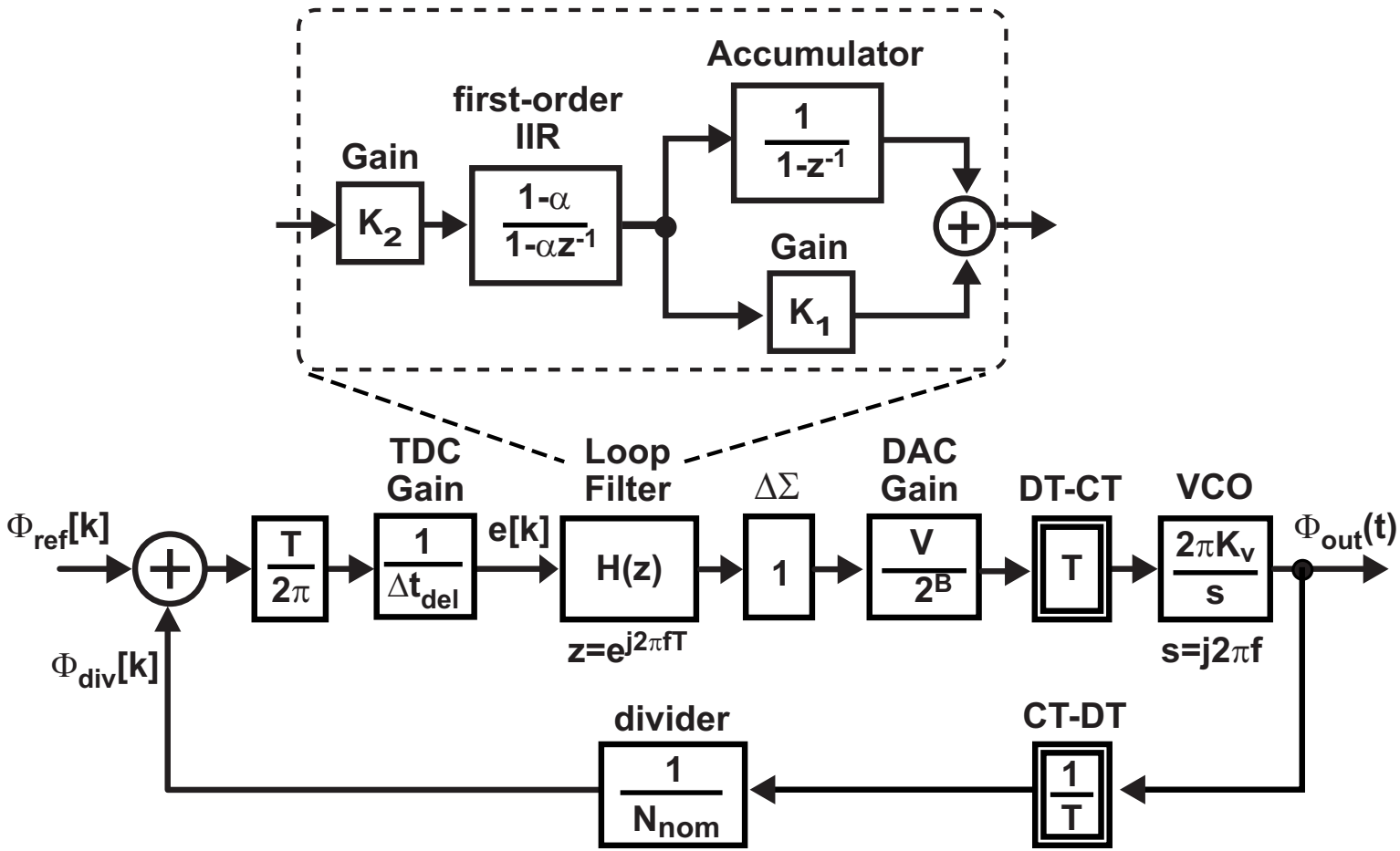
- DAC thermal noise impacts performance due to the higher coarse VCO gain
  - Can we somehow lower the DAC bandwidth?

Fix: Leverage the Divider as a Signal Path



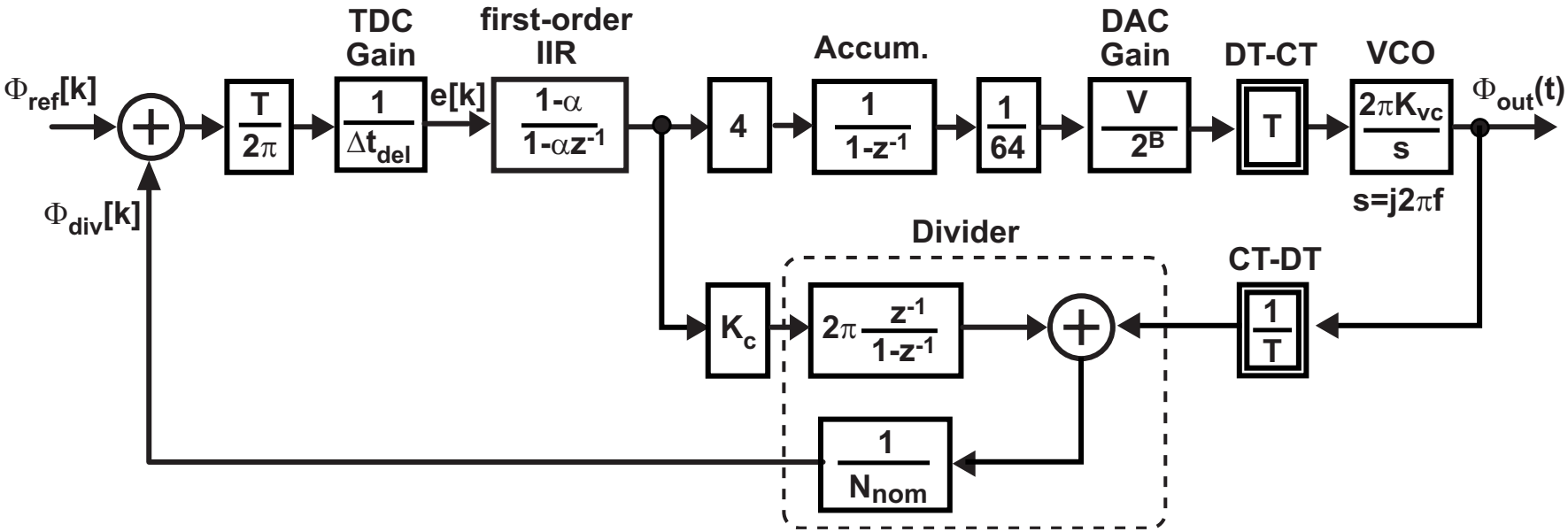
- Bypass to divider for feed-forward path allows coarse DAC bandwidth to be dramatically reduced!

Linearized Model of PLL Under Fine-Tune Operation



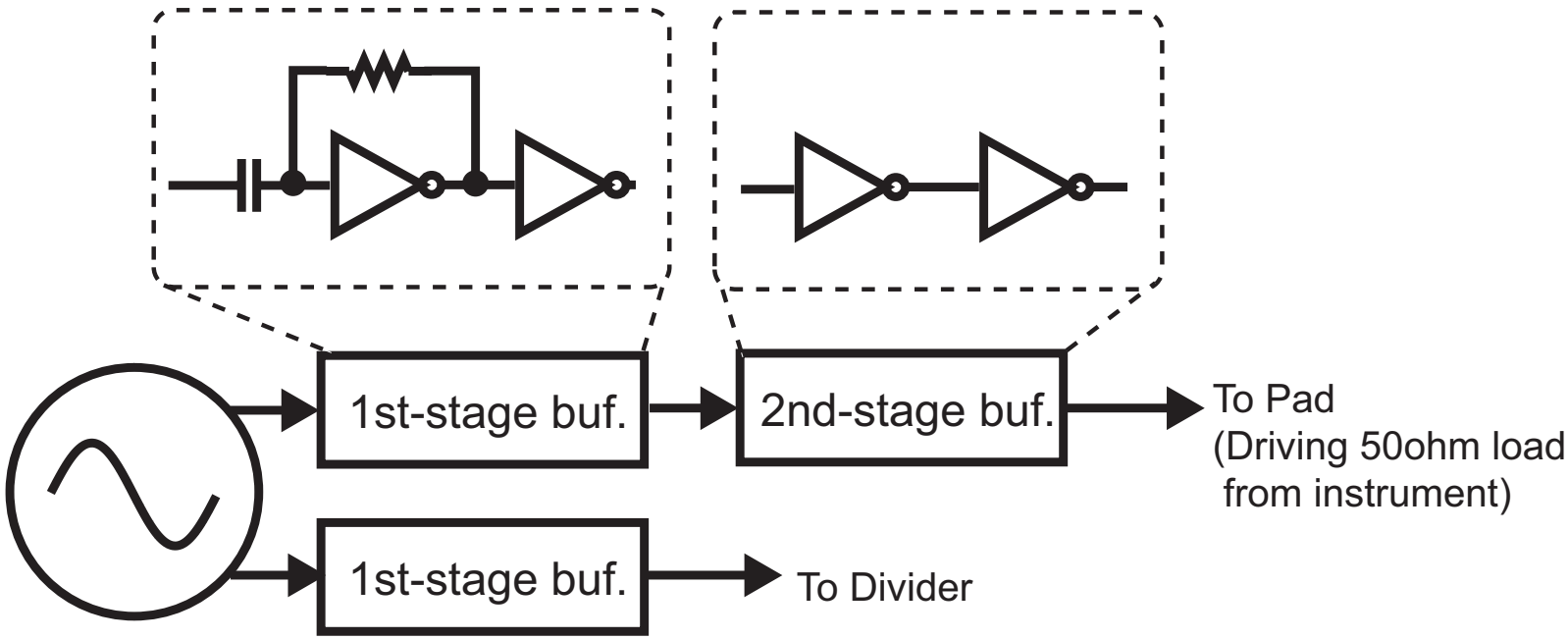
- Standard lead-lag filter topology but implemented in digital domain
  - Consists of accumulator plus feedforward path

Linearized Model of PLL Under Coarse-Tune Operation



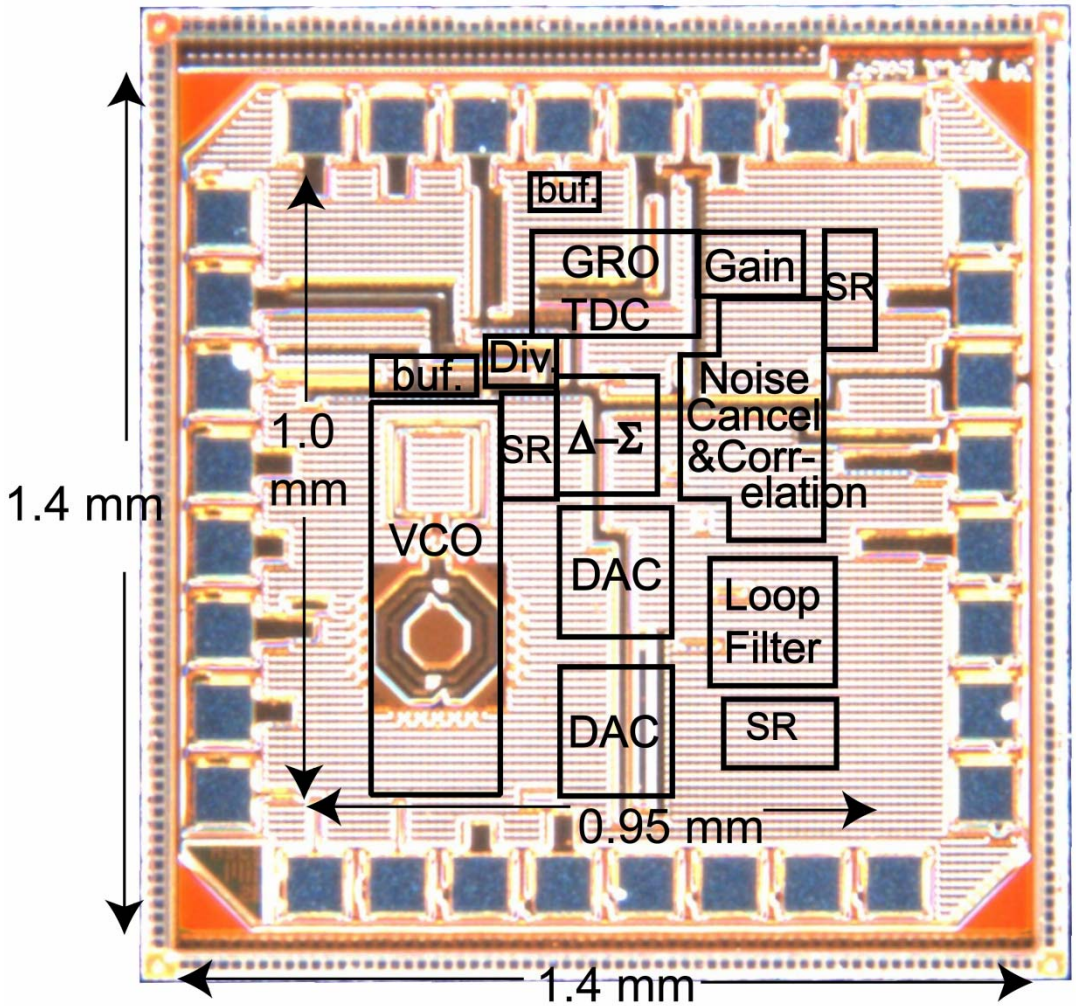
- **Routing of signal path into Sigma-Delta controlling the divider yields a feedforward path**
  - **Adds to accumulator path as both signals pass back through the divider**
  - **Allows reduction of coarse DAC bandwidth**
    - Noise impact of coarse DAC on VCO is substantially lowered

VCO Buffer Implementation



- Consists of inverters with self-biased first stage
  - AC coupling from VCO output into buffer
  - Achieves low noise (as will be seen in far-out phase noise in measured results)

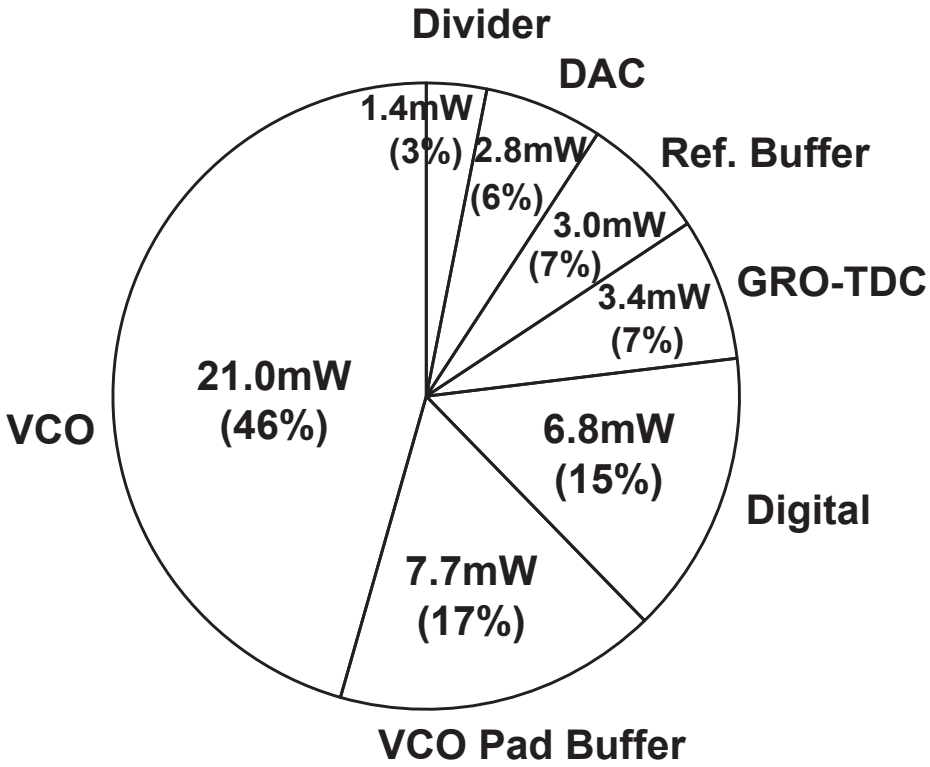
Die Photo



- 0.13-µm CMOS
- Active area: 0.95 mm^2
- Chip area: 1.96 mm^2
- V_{DD}: 1.5V
- Current:
  - 26mA (Core)
  - 7mA (VCO output buffer at 1.1V)

GRO-TDC:
- 2.3mA
- 157X252 um^2

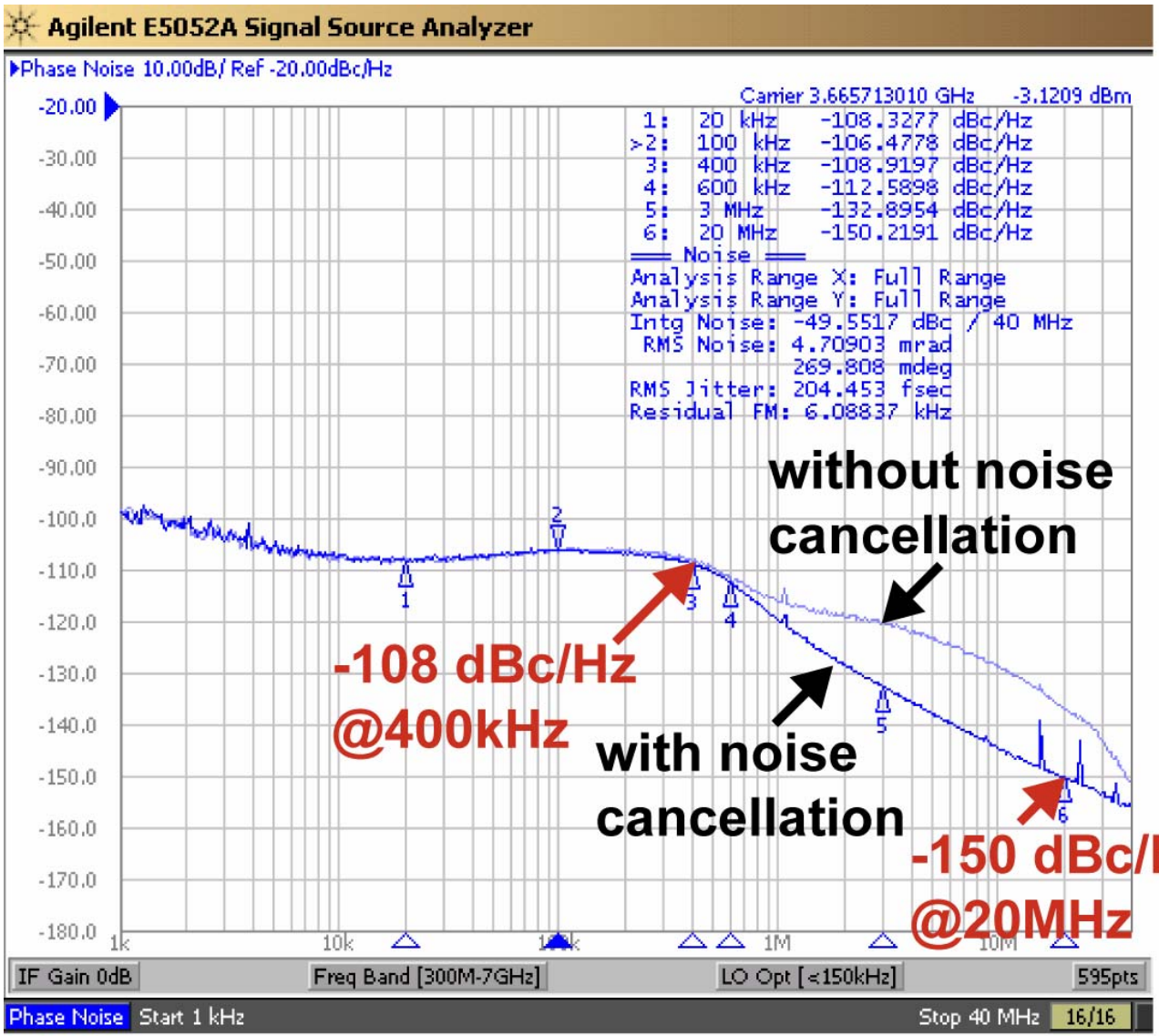
Power Distribution of Prototype IC



Total Power: 46.1mW

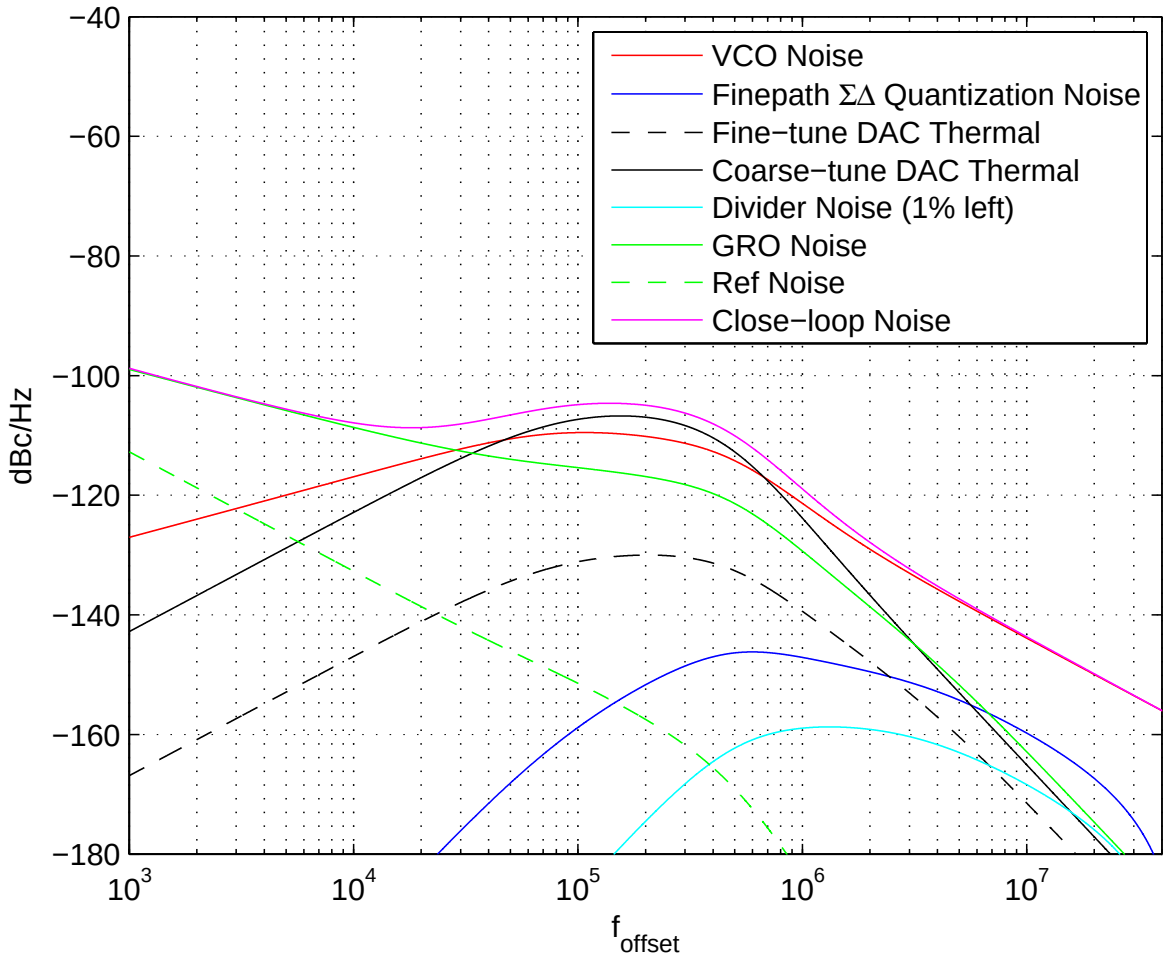
- Notice GRO and digital quantization noise cancellation have only minor impact on power (and area)

Measured Phase Noise at 3.67GHz



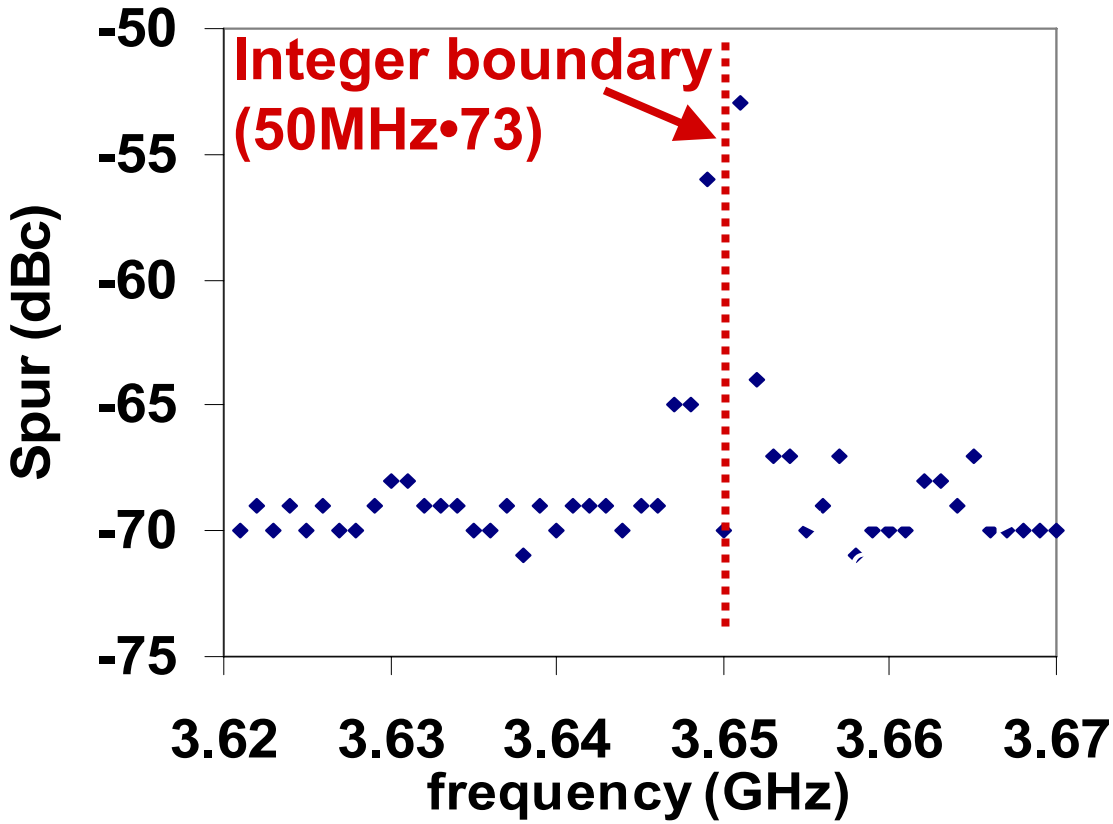
- Suppresses quantization noise by more than 15 dB
- Achieves 204 fs (0.27 degree) integrated noise (jitter)
- Reference spur: -65dBc

Calculation of Phase Noise Components



- **See wideband digital synthesizer tutorial available at http://www.cppsim.com**

Measured Worst Spurs over Fifty Channels



- Tested from 3.620 GHz to 3.670 GHz at intervals of 1 MHz
  - Worst spurs observed close to integer-N boundary (multiples of 50 MHz)
- -42dBc worst spur observed at 400kHz offset from boundary

Conclusions

- **Digital Phase-Locked Loops look extremely promising for future applications**
  - **Very amenable to future CMOS processes**
  - **Excellent performance can be achieved**

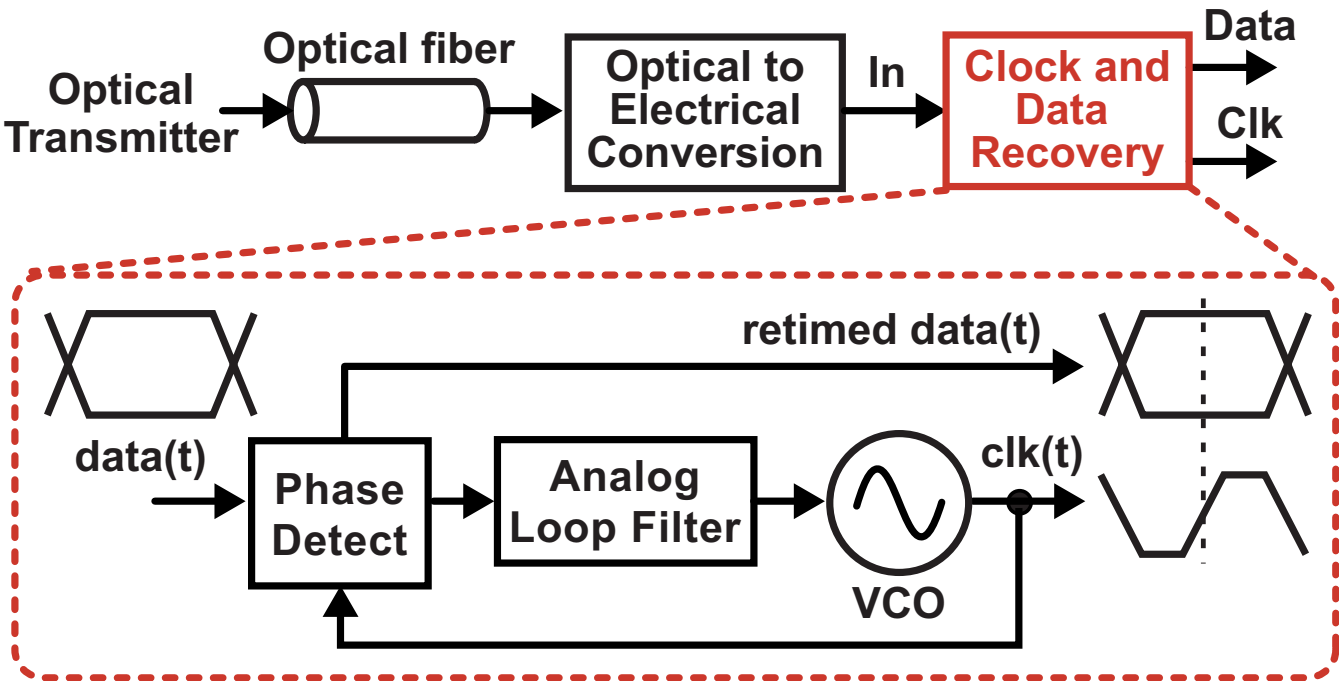
- **A low-noise, wide-bandwidth digital ΔΣ fractional-N frequency synthesizer is achieved with**
  - **High performance *noise-shaping* GRO TDC**
  - **Quantization noise cancellation in *digital* domain**

- **Key result: < *250 fs* integrated noise with 500 kHz bandwidth**

Innovation of future digital PLLs will involve joint circuit/algorithm development

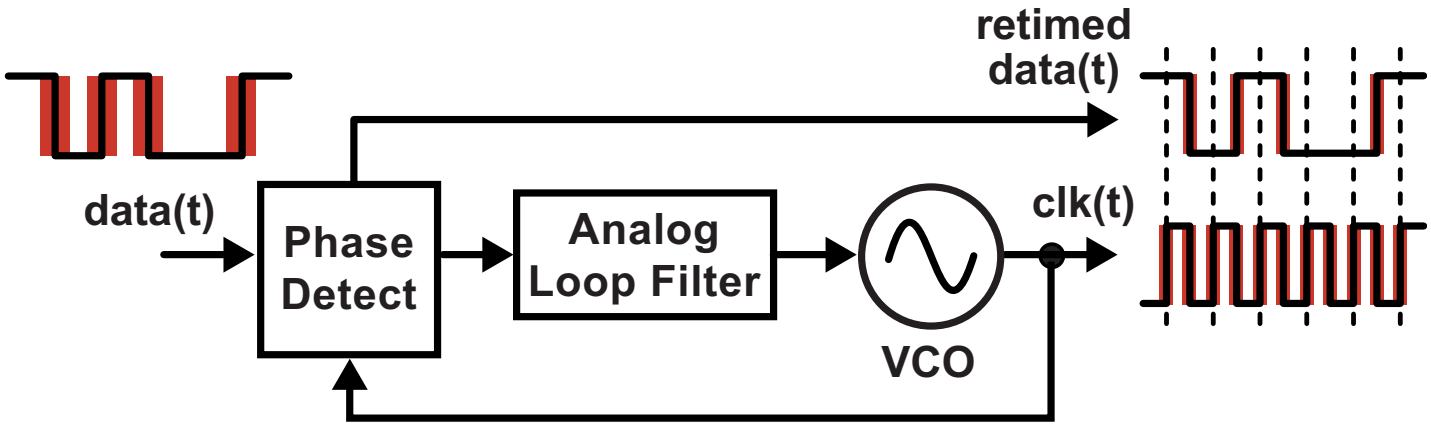
Mixed Signal CDR Example

Clock and Data Recovery Circuits for SONET



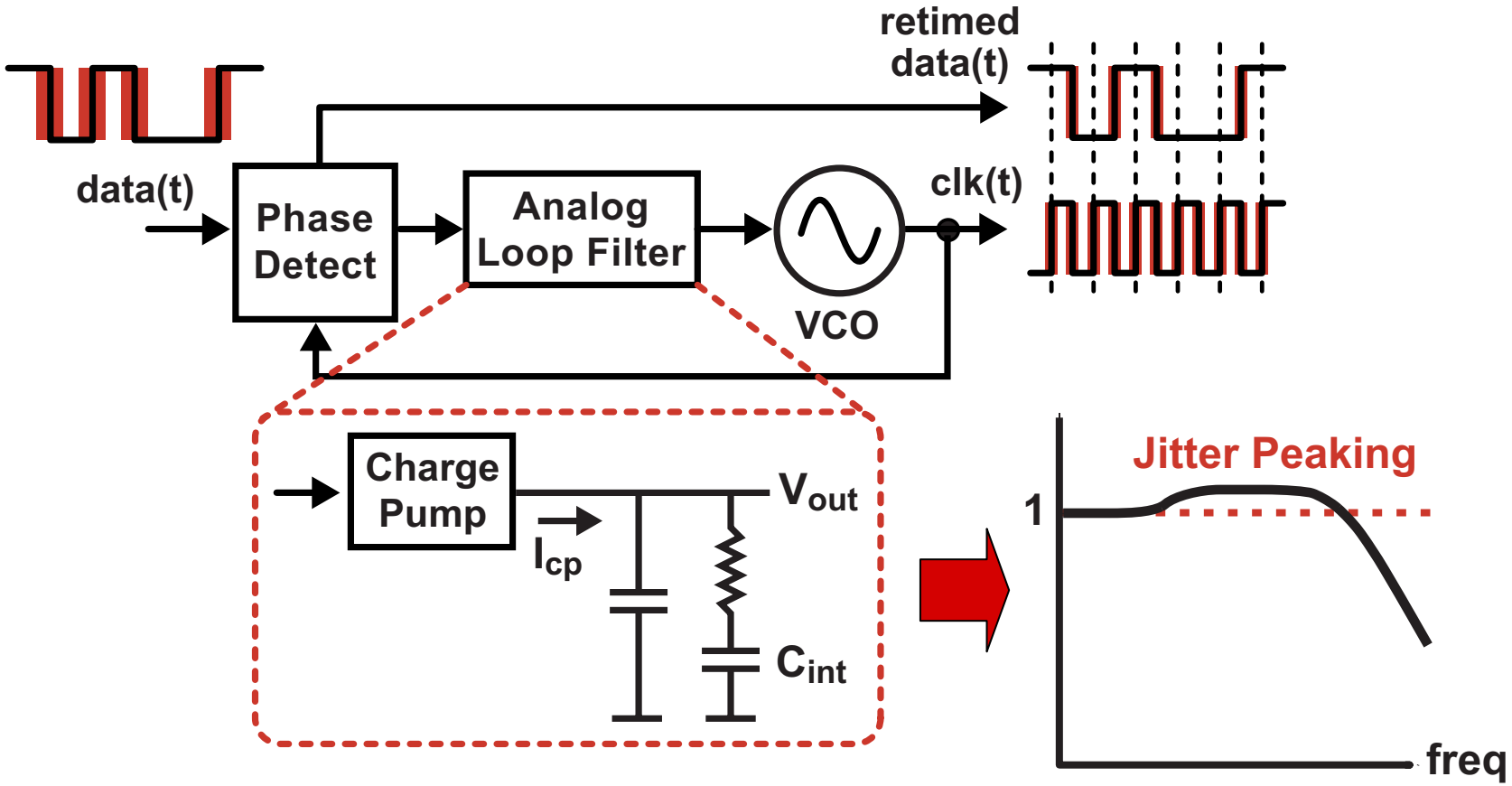
- Function: recover clock from input NRZ data stream
  - Want to support multi-rates: 2.5 Gb/s, GbE, 622 Mb/s, 155 Mb/s
- Structure: phase-locked loop with an appropriate phase detector
- Focus: analog, digital, or hybrid (i.e., mixed-signal) implementation?

Key Jitter Performance Metrics for SONET



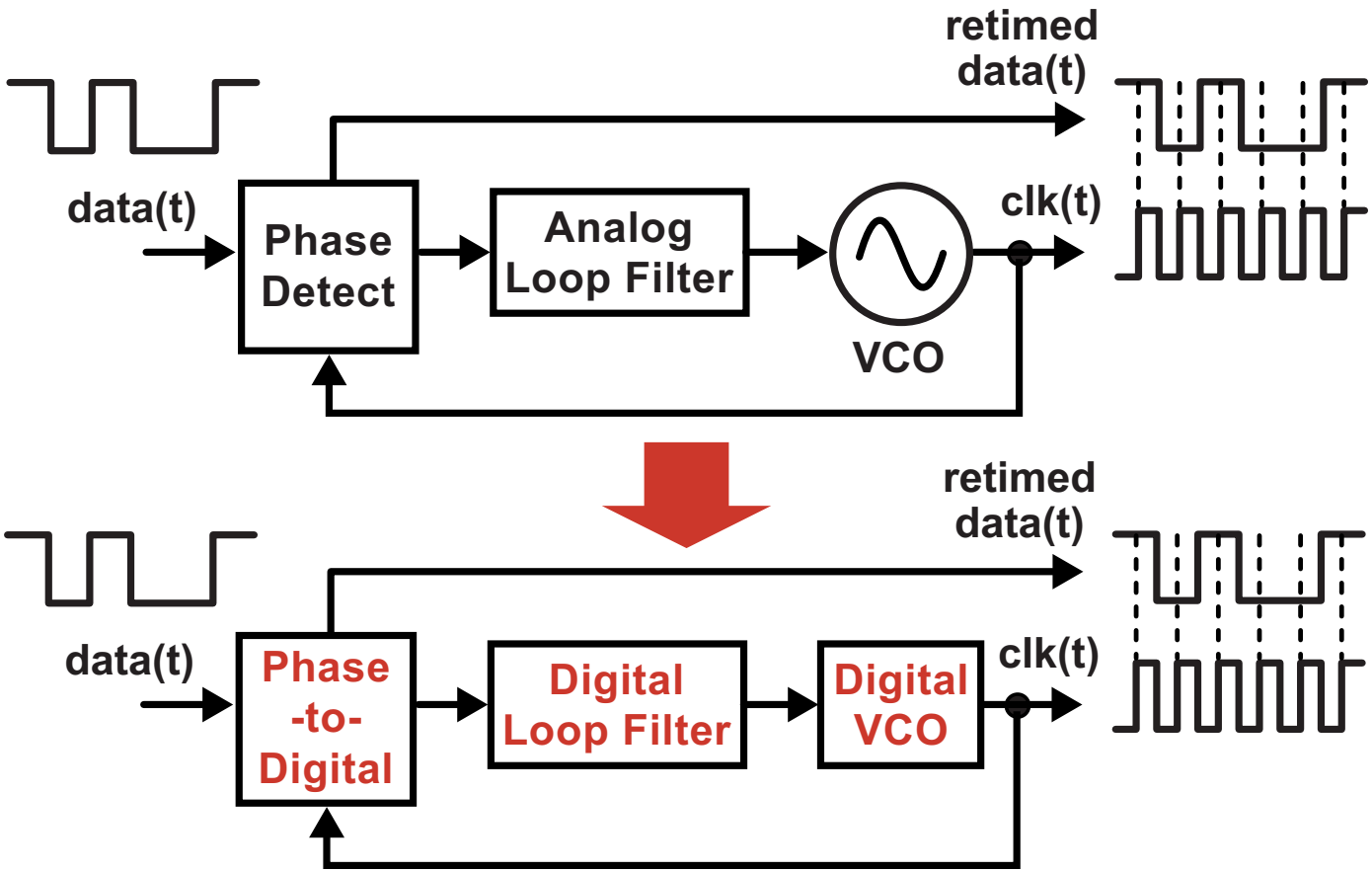
- Jitter generation: amount of jitter produced by PLL
  - Achieved by designing low noise PLL
- Jitter tolerance: amount of input jitter tolerated by PLL
  - Achieved through appropriate design of phase detector
- Jitter transfer: required filtering of input jitter
  - Achieved by properly designing transfer function of PLL
  - Key challenge: need < 0.1 dB peaking in transfer function

The Woes of an Analog PLL Implementation



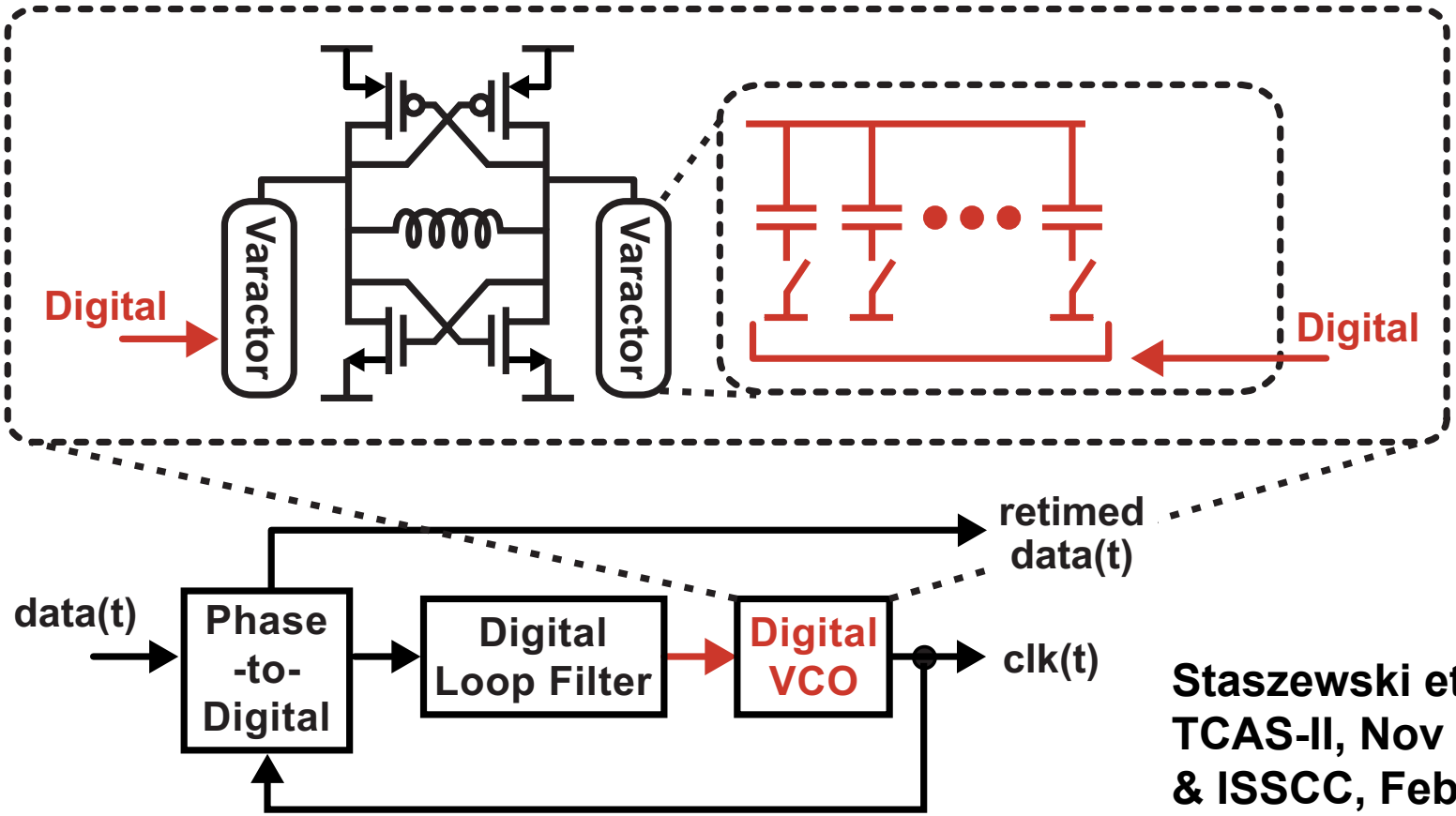
- Goal: integrated loop filter
- Issue: required cap value too large (100 uA charge pump):
  - 2.5 Gb/s (OC-48): 4 nF
  - 155 Mb/s (OC-3): 64 nF

Consider A Digital CDR …



- Digital loop filter allows:
  - Easy integration of loop filter
  - Easy configurability for multi-rate operation

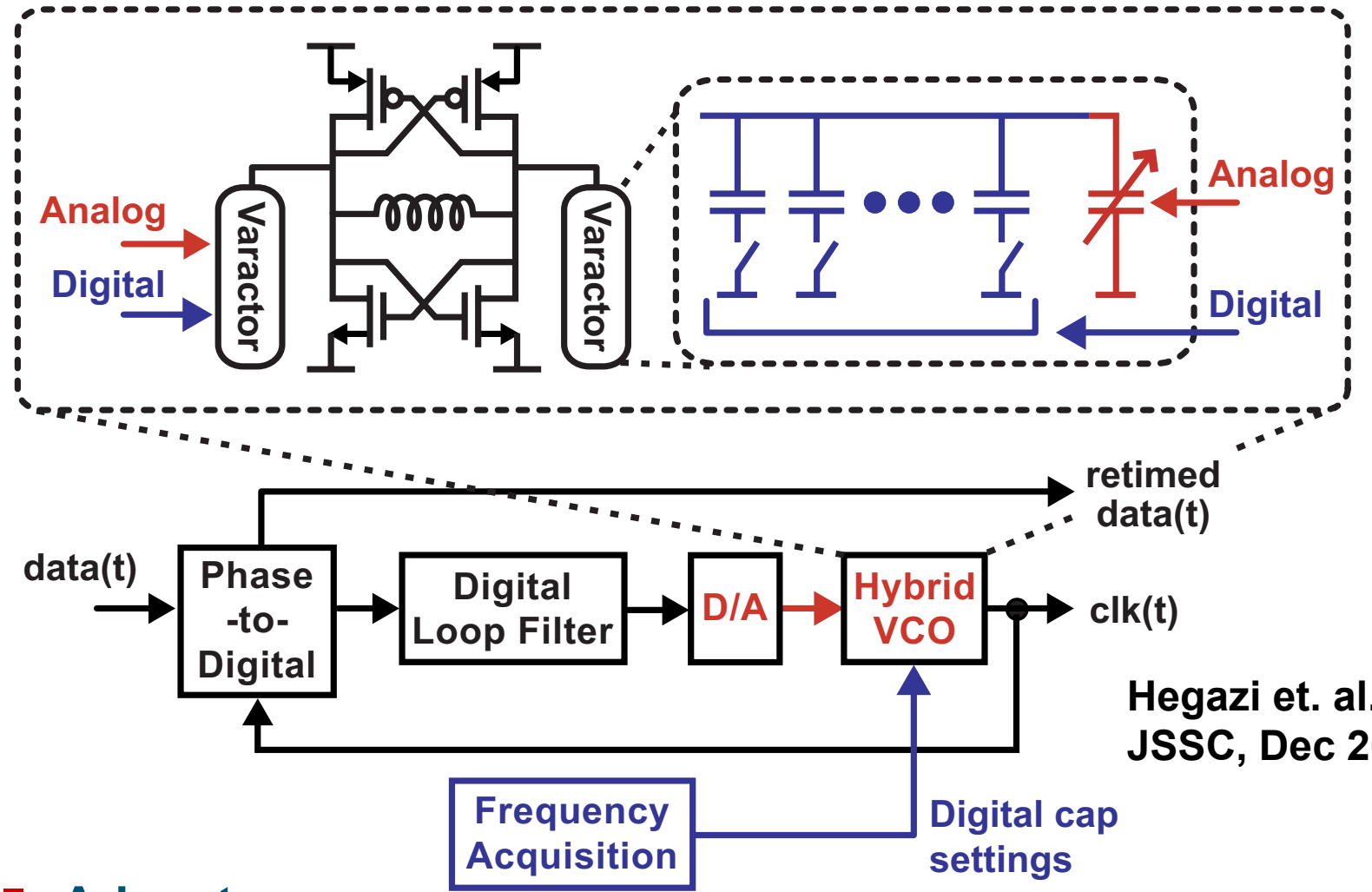
Digital VCO Implementation



Staszewski et. al.,
TCAS-II, Nov 2003
& ISSCC, Feb 2004

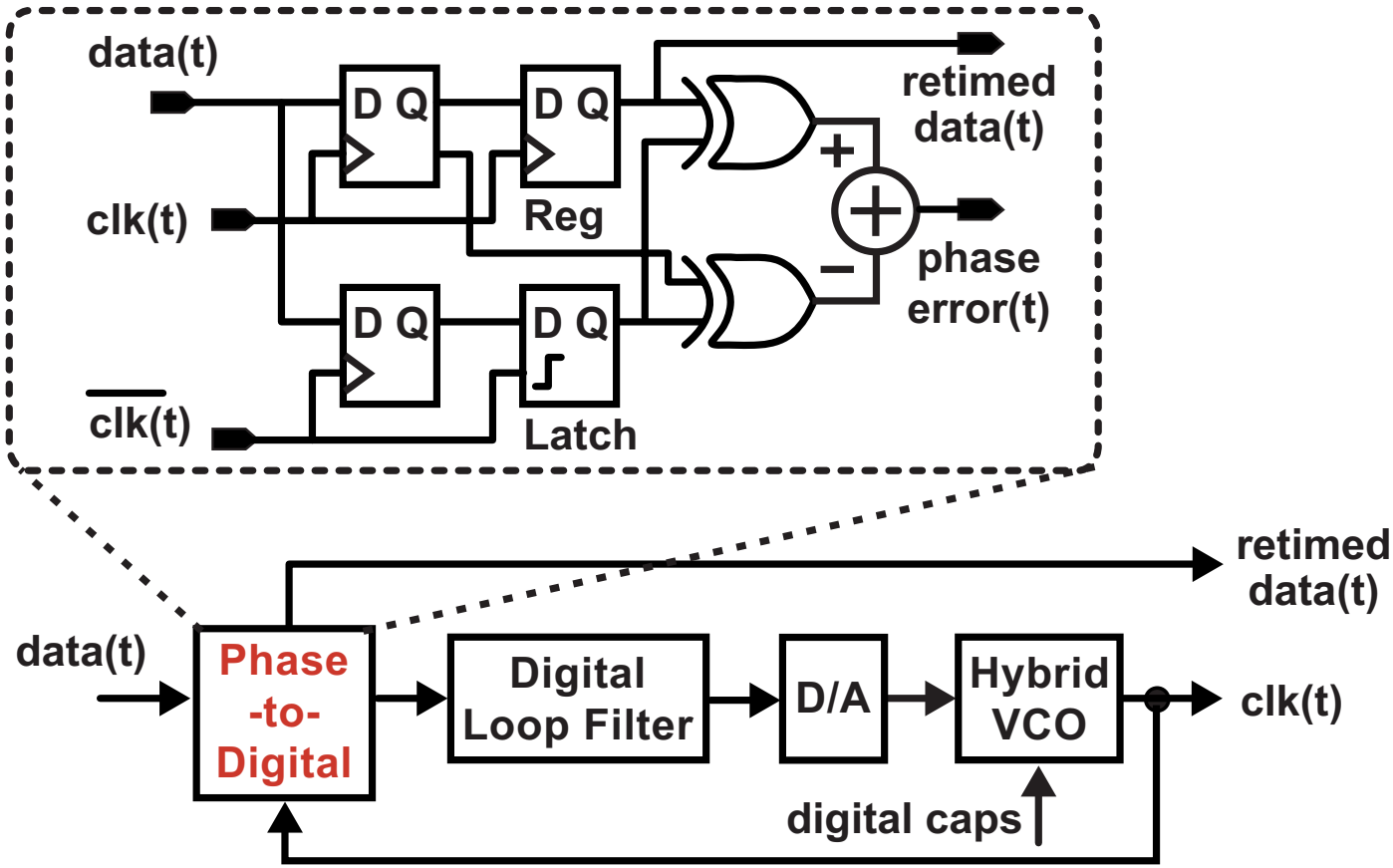
- Other researchers have demonstrated a "digital" LC VCO using a switched capacitor bank
- Issue: better suited for 0.09u rather than 0.25u CMOS

Hybrid VCO Implementation



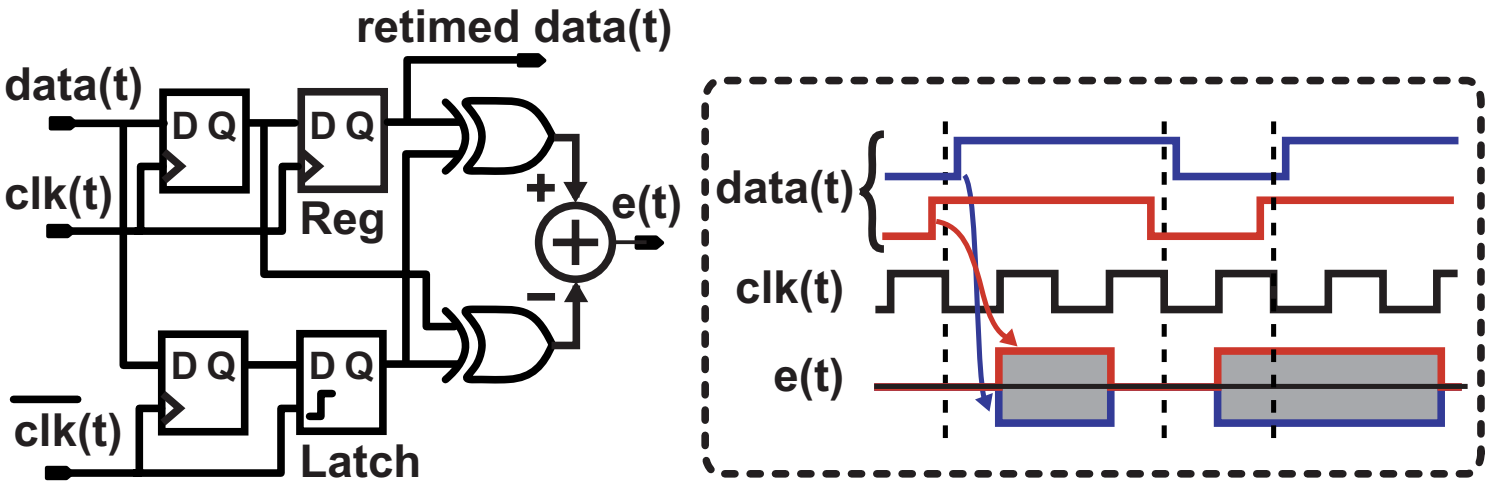
- **Advantages**
  - Low phase noise, easy implementation in 0.25u CMOS

Bang-Bang Structure as Digital Phase Detector?



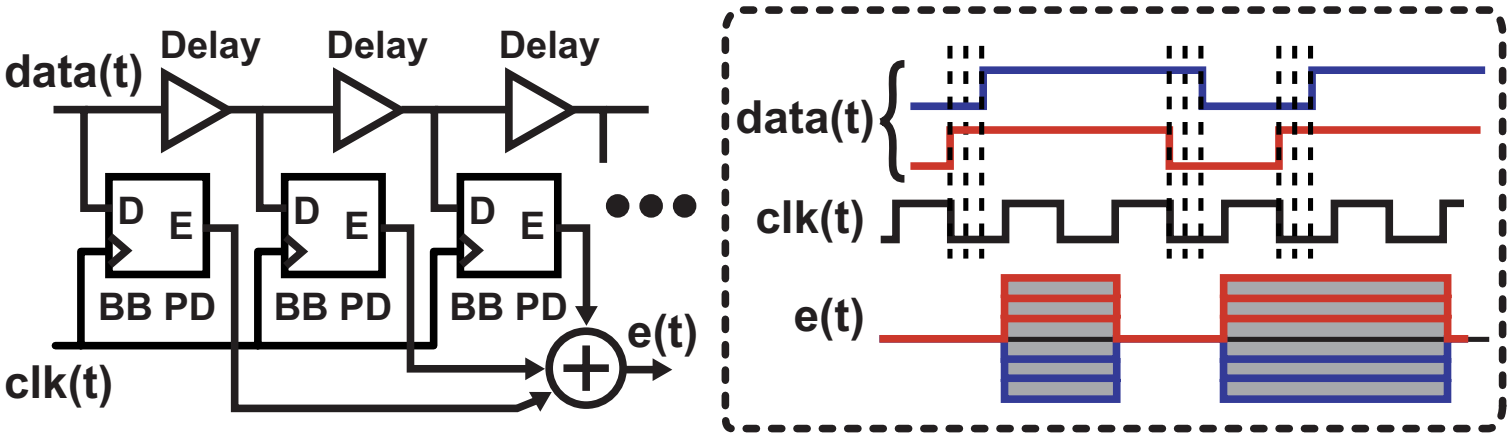
- Advantages: purely digital implementation with low complexity and low clock loading
- Issue: leads to nonlinear CDR behavior

A Closer Look at the Bang-Bang Detector



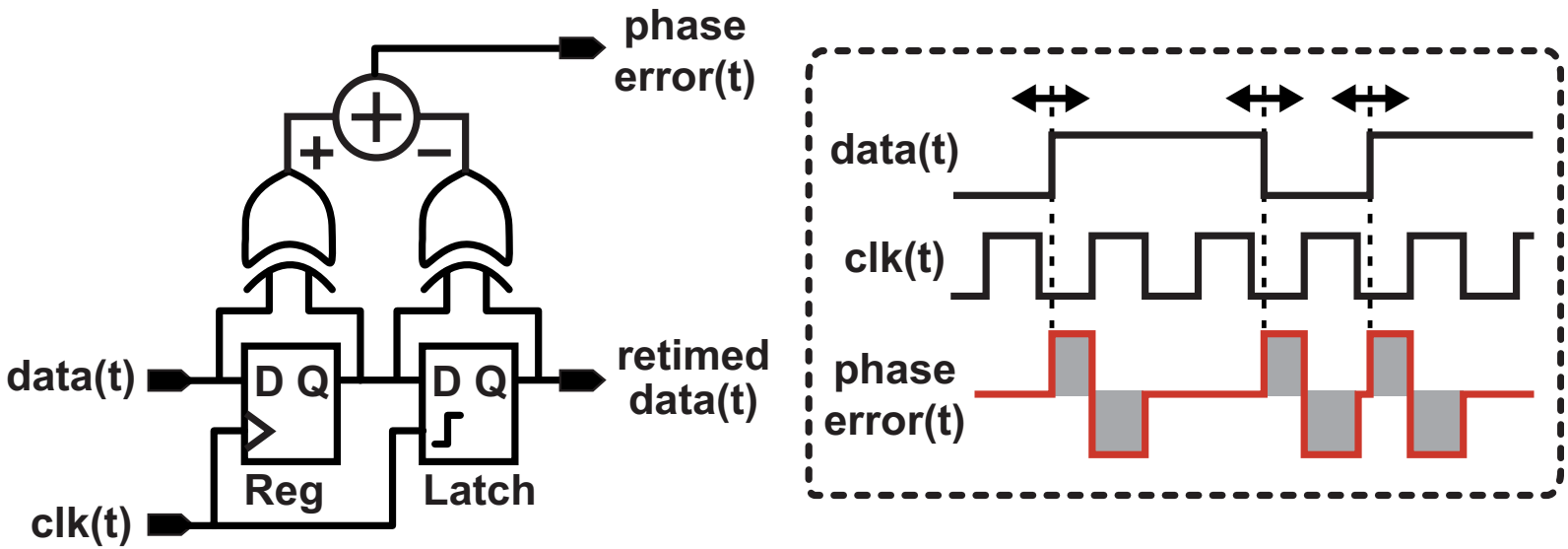
- Phase error output consists of pulses of *fixed* area that are either positive or negative
  - Nonlinear phase detection!
- Issue: PLL dynamics become nonlinear
  - Difficult to meet SONET Jitter Transfer Specification
  - Prone to limit cycle issues

A Flash Phase-to-Digital Converter?



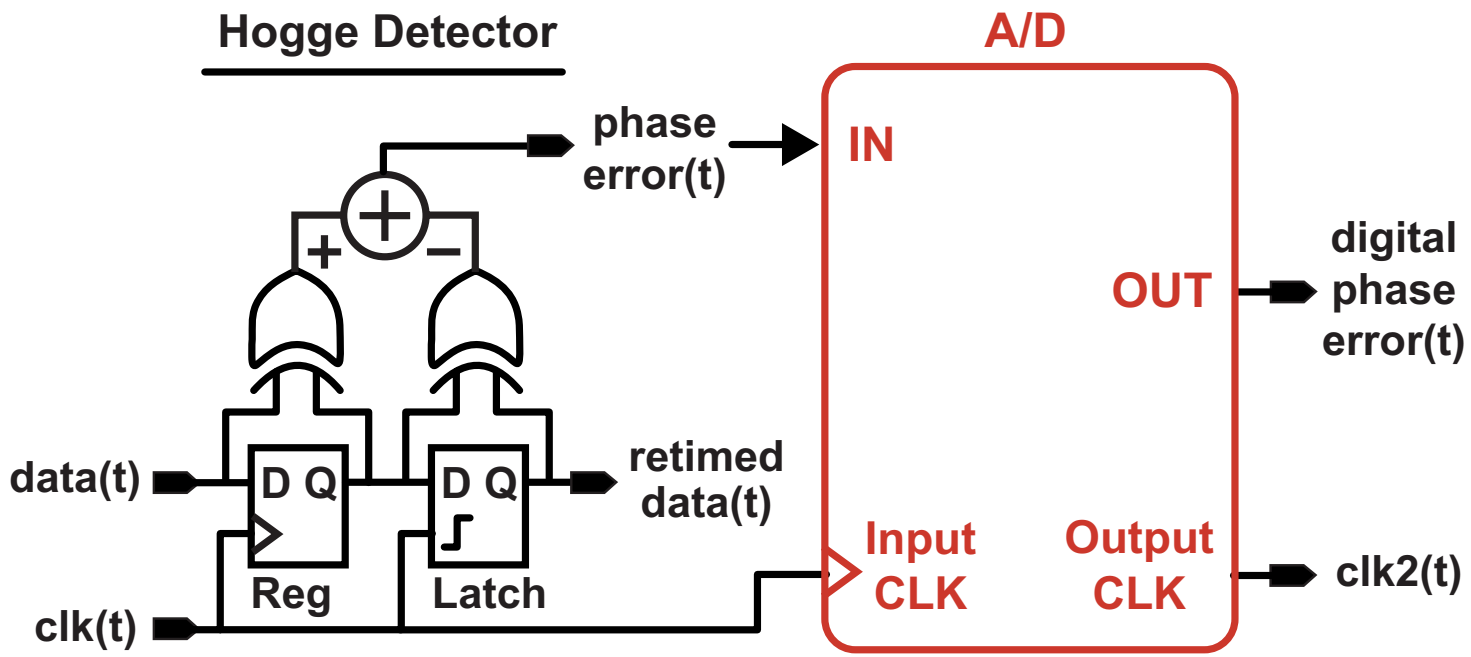
- Chain several bang-bang detectors through delays
  - Allows multi-level phase detection with digital structure
  - Similar to time-to-digital converters of other researchers
    - Staszewski et. al., **TCAS-II, Nov 2003** & ISSCC, Feb 2004
- Issues:
  - High power consumption (multi-GHz operation required)
  - High clock loading (complicates VCO buffer design)
  - Prone to limit cycle issues

An Analog Phase Detector?



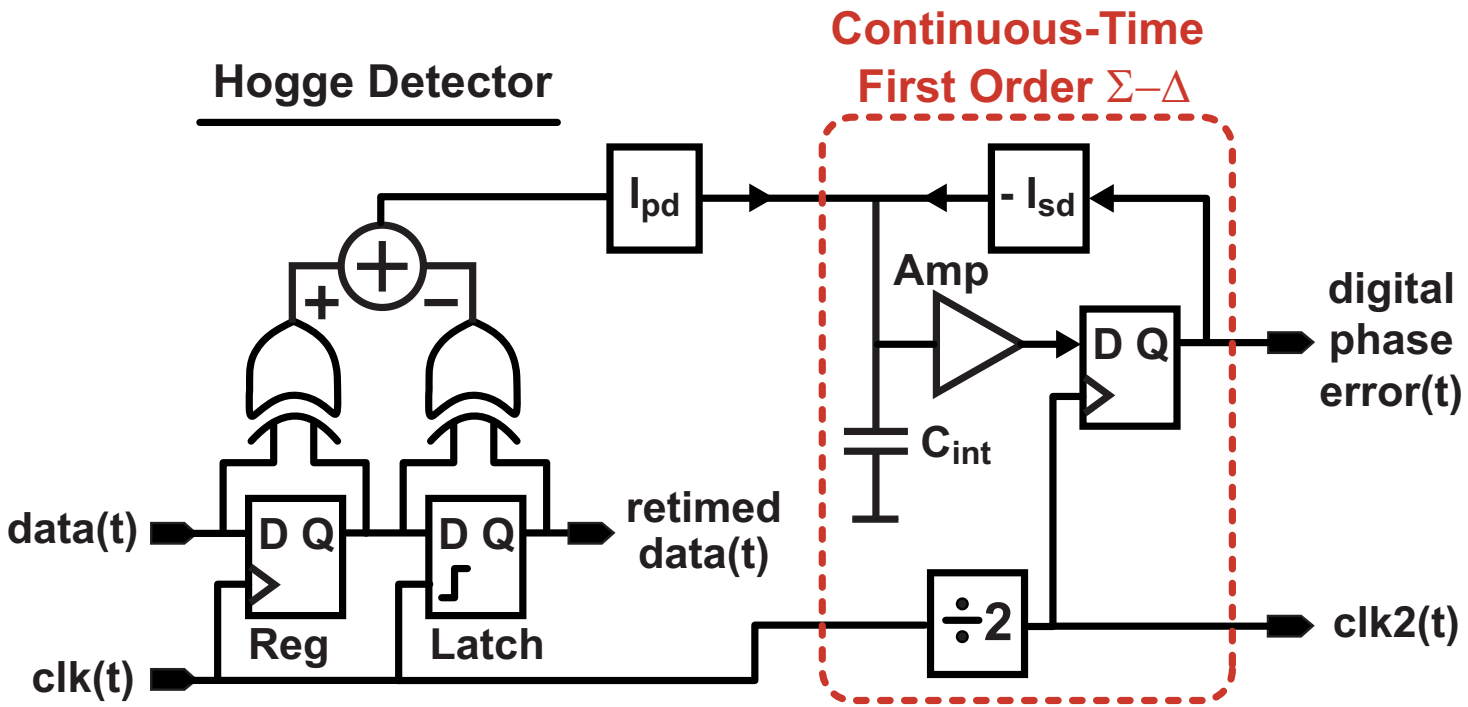
- Hogge detector popular in analog CDR designs
- Advantages
  - Low complexity, power consumption, and clock loading
  - Leads to linear PLL dynamics
- Issue
  - We need a digital output!

Proposed Phase-to-Digital Converter



- Combine Hogge Detector with a high speed A/D
- Issues:
  - Want high resolution (i.e., to achieve high linearity)
  - Want low power, low clock loading, and compact area

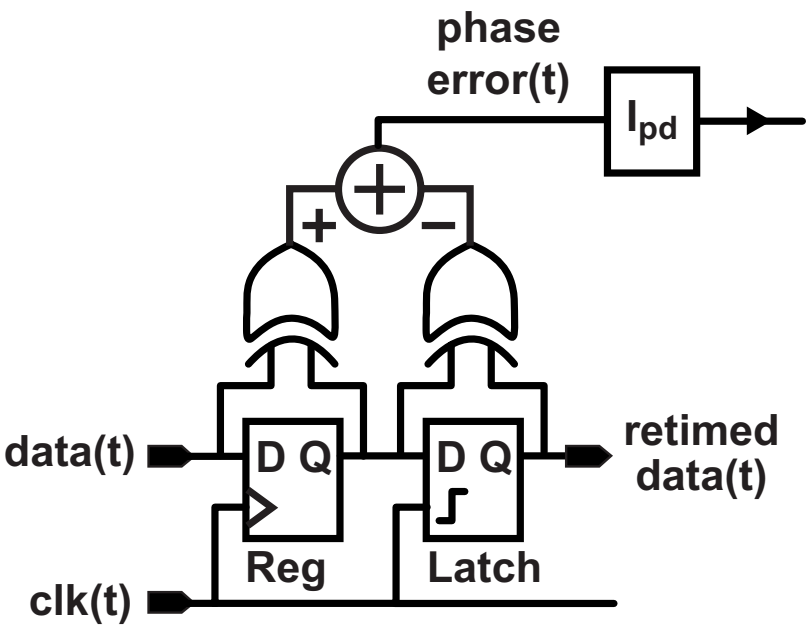
Proposed A/D Approach

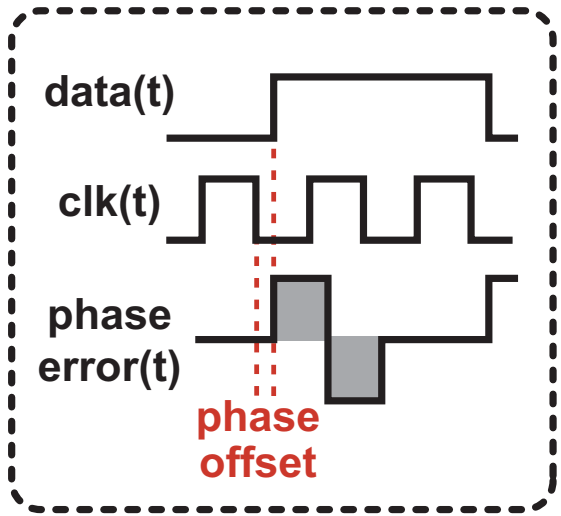


- A first order continuous-time Sigma-Delta A/D
  - Achieves high resolution, low power, low clock loading, compact area
- How could this work??
  - Can easily clock at GHz speeds (i.e., high oversampling)
  - Hogge output provides random dithering source for free

Phase-to-Digital Converter Implementation Details

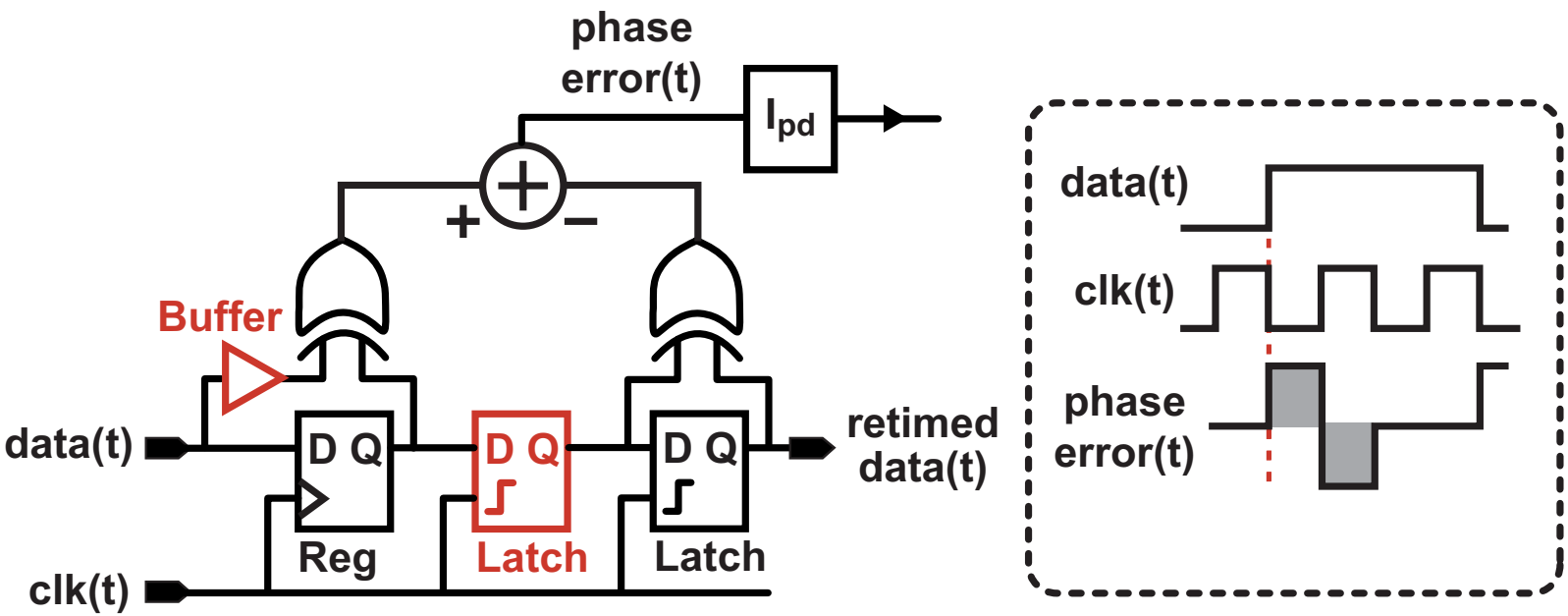
- Start with Hogge Detector/Charge Pump implementation





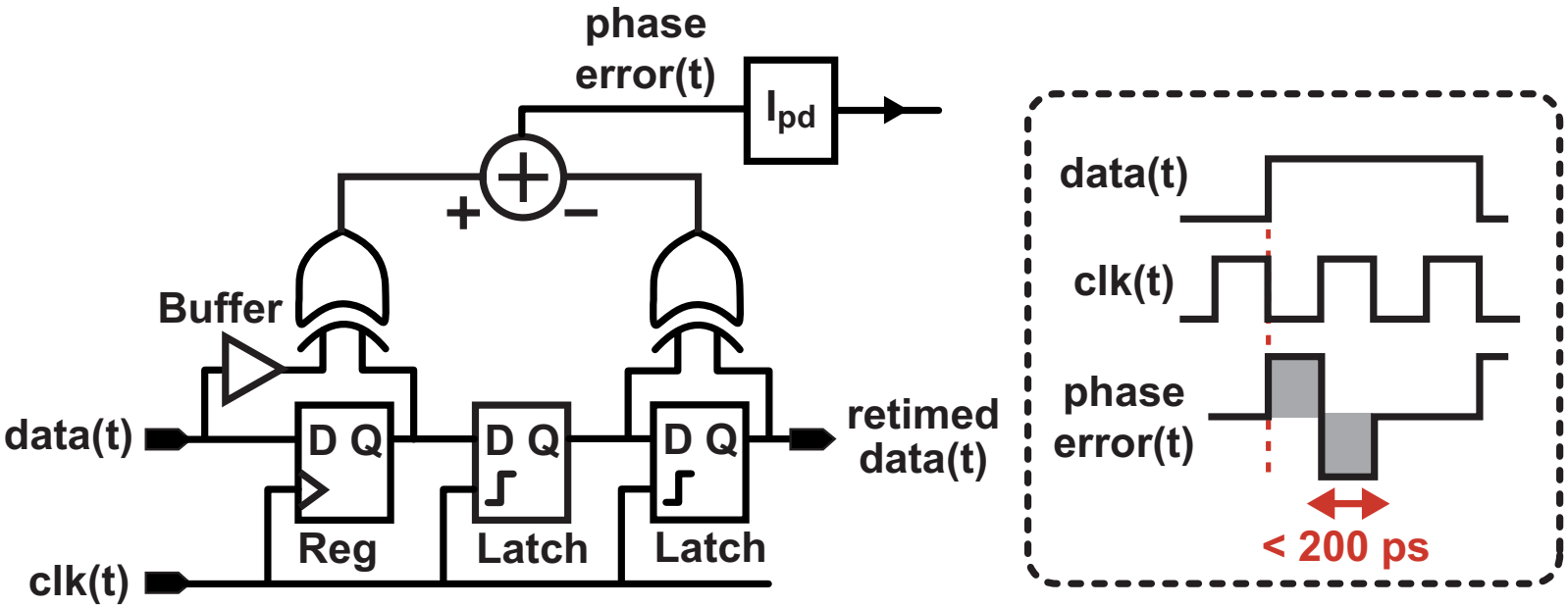
- Issue 1: Hogge detector is prone to phase offsets
  - Caused by unequal delays for XOR input signals
  - Degrades jitter tolerance performance

Improvement of Phase Offset of Hogge Detector



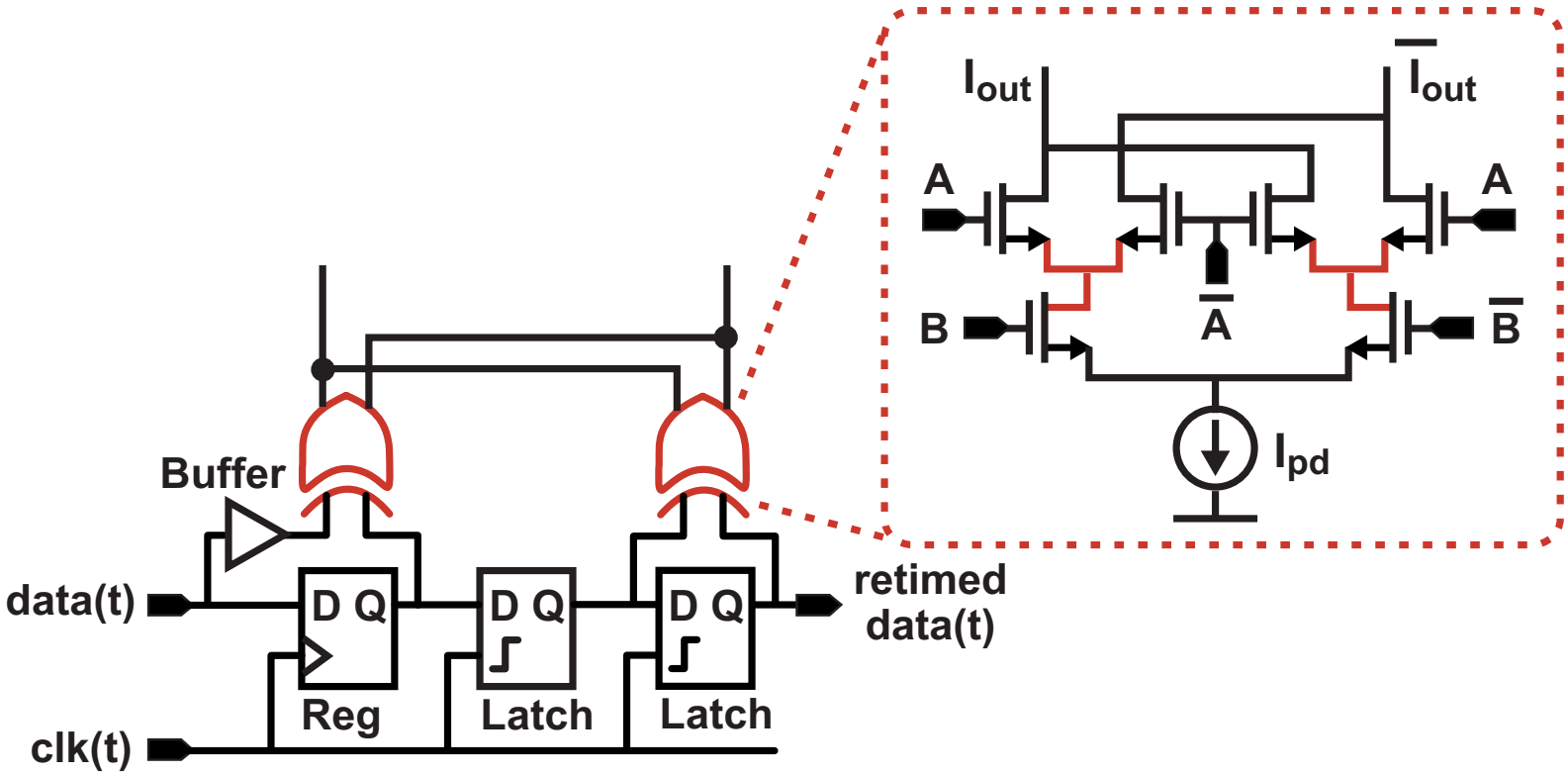
- Extra latch improves matching of loads of Reg and Latch
- Extra buffer ideally matches clk-to-Q delay of Reg

Challenge of 2.5 Gb/s Operation in 0.25u CMOS



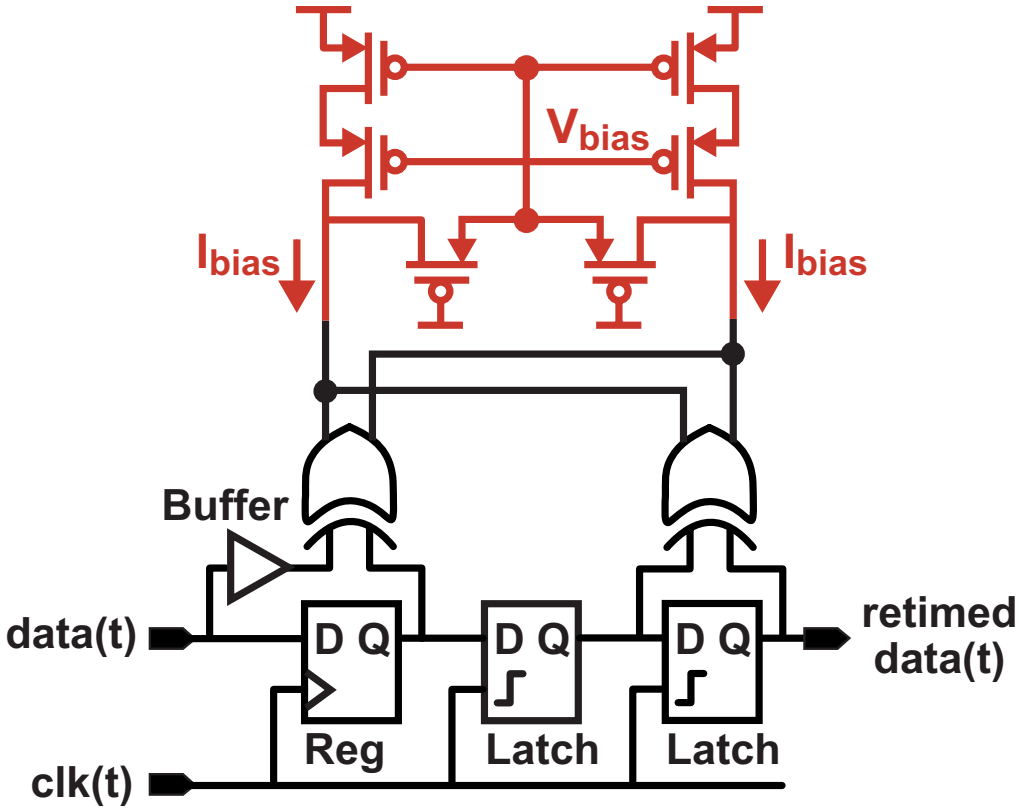
- XOR outputs have pulse widths < 200 ps at 2.5 Gb/s
  - Complicates efforts to achieve reasonable linearity and phase detector range

A Combined XOR/Charge Pump Topology



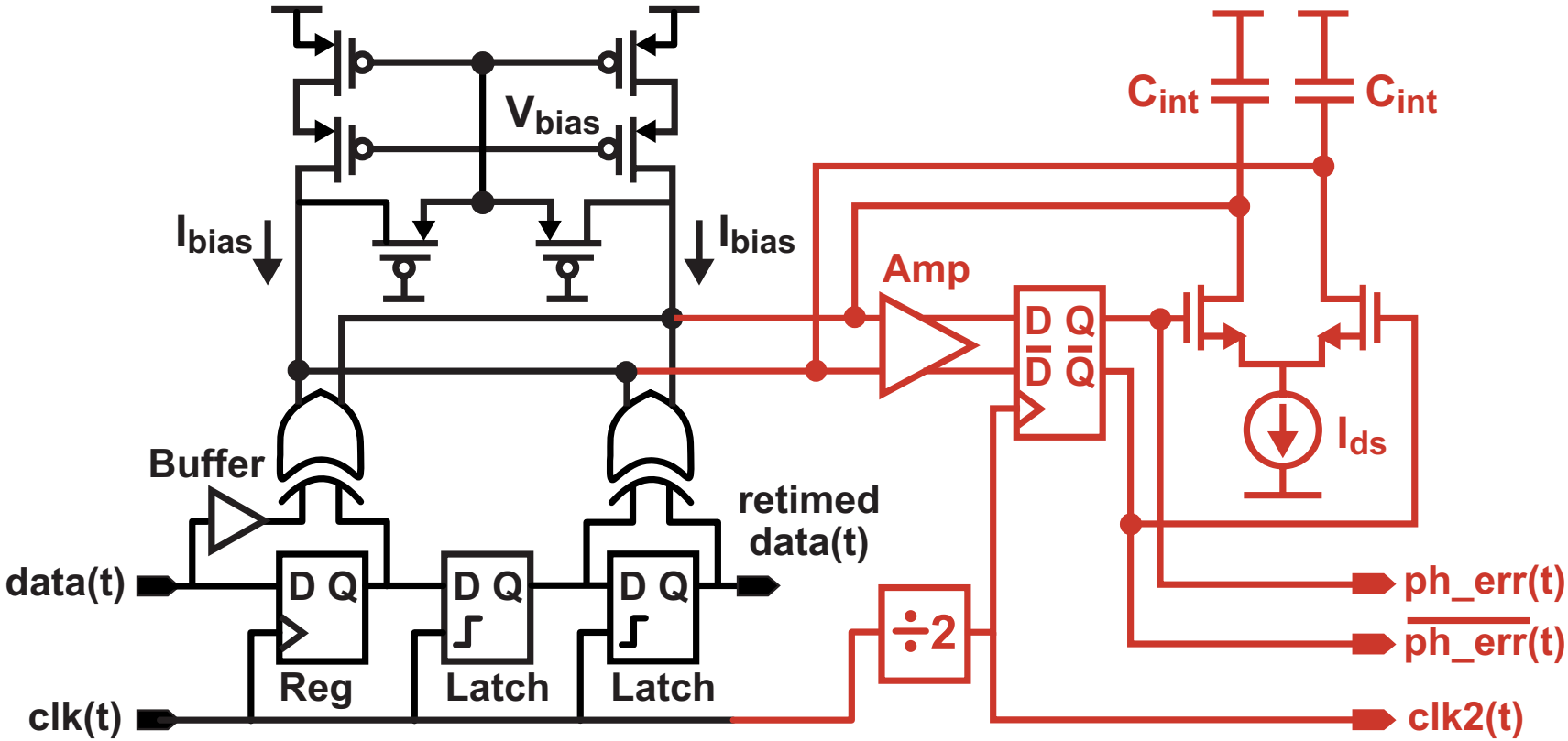
- Limits short pulse width signals to low impedance nodes
  - Fast pulses occur at source nodes of devices
  - Note: XOR outputs feed into “low impedance” capacitor
- Combined implementation saves power and area

Bias Network with Simple Common-Mode Feedback



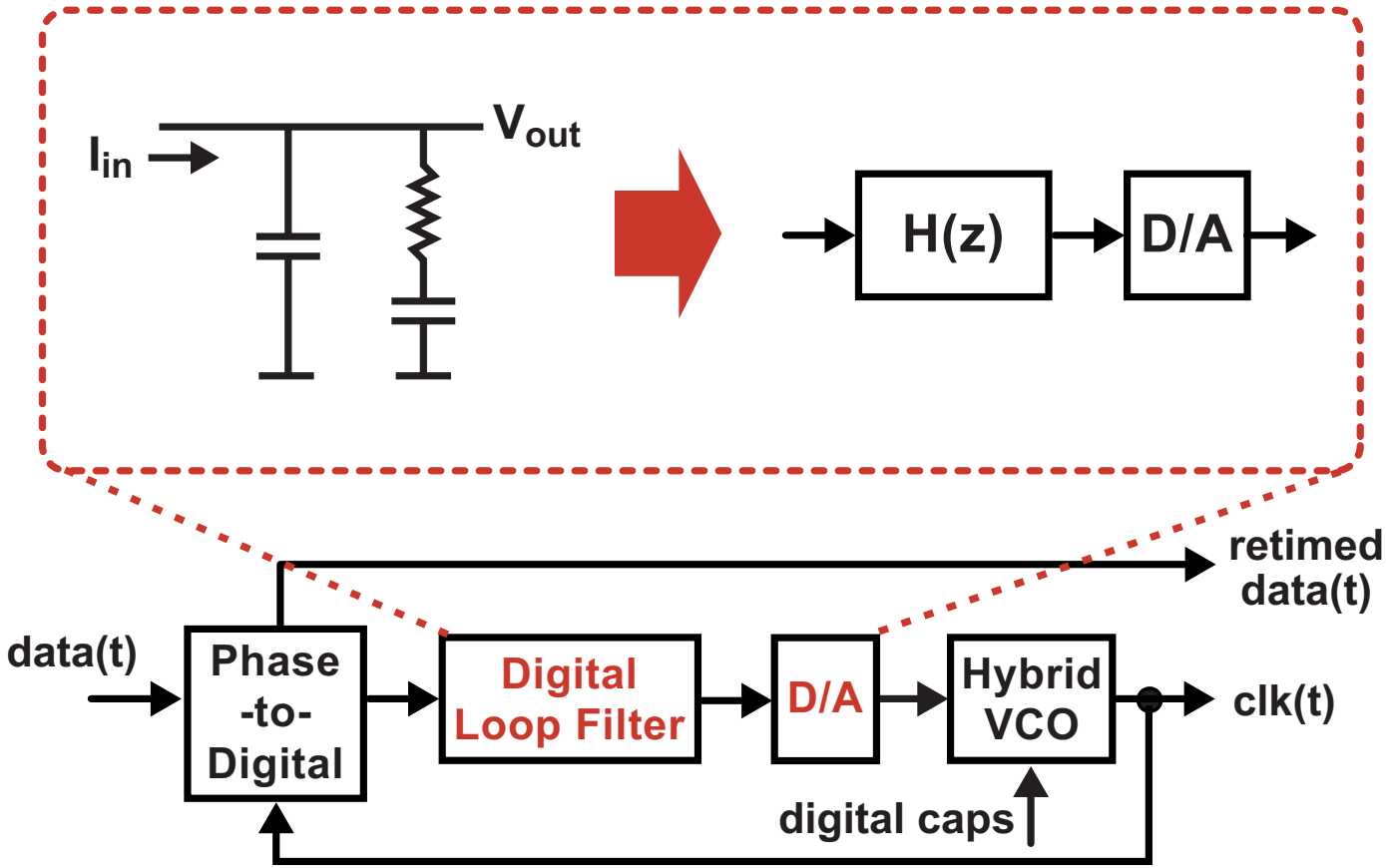
- Common-mode feedback sets voltage according to voltage of top PMOS devices
  - Size PMOS devices appropriately for desired voltage
- Achieves high impedance with compact design

First Order, CT, Sigma-Delta A/D Topology



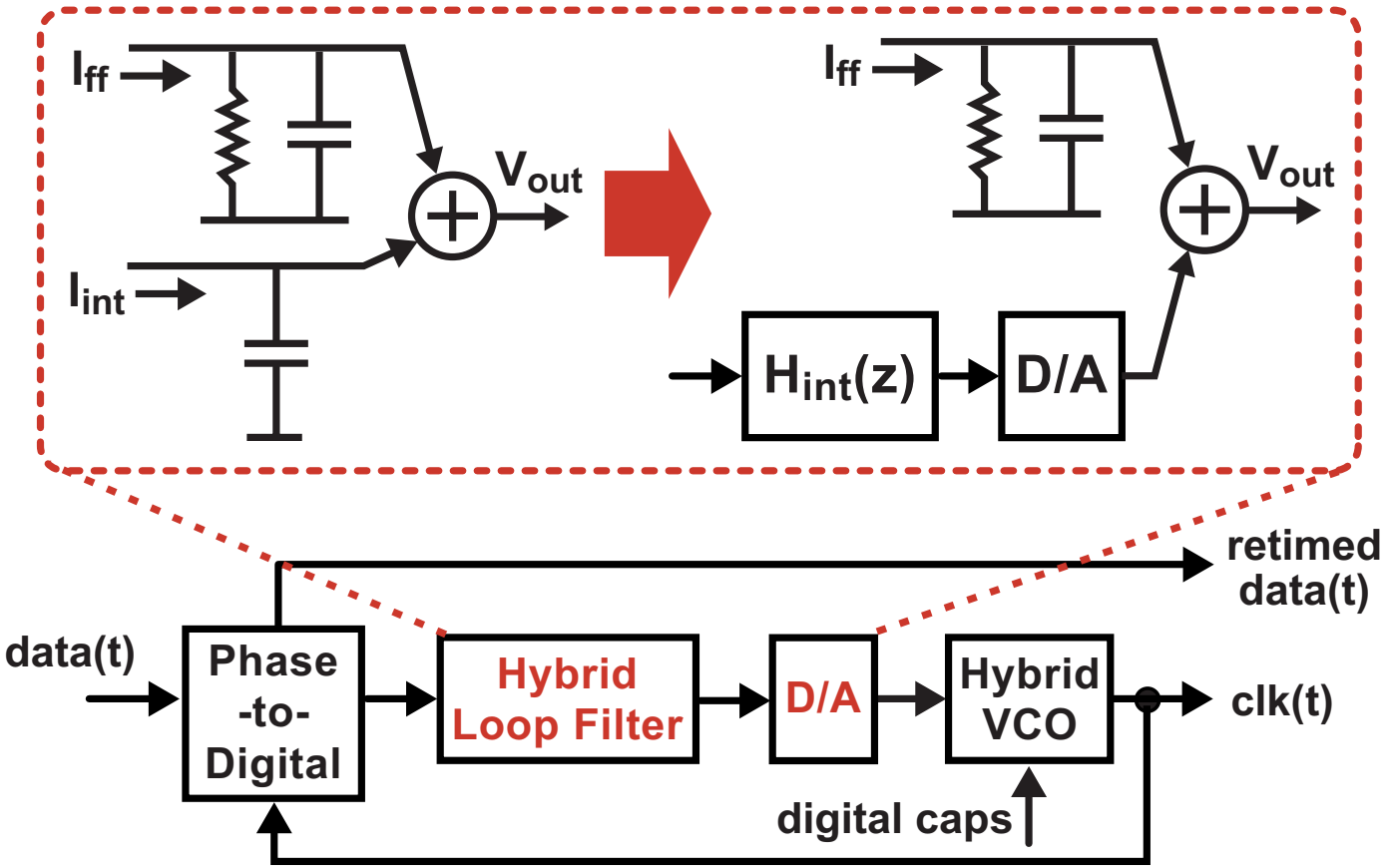
- Simple design allows high speed clocking
- Metastability behavior improved with:
  - Inclusion of Amp
  - Slight reduction of clock frequency (i.e., 1.25 GHz)

Digital Loop Filter and D/A Implementation



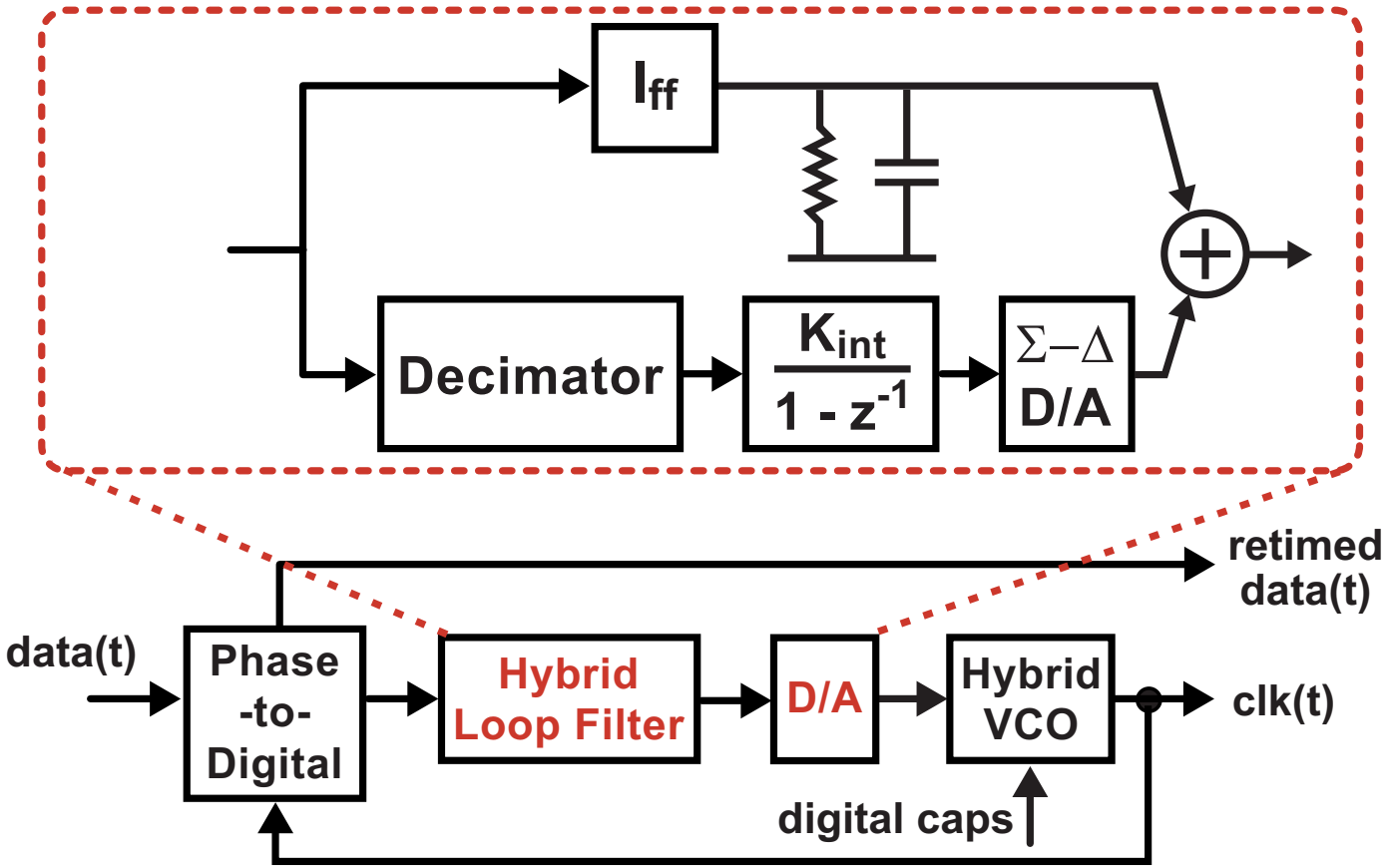
- Goal: digital implementation of analog lead/lag filter
- Issue: requires D/A with >> 1 MHz bandwidth, high resolution
  - An easier D/A implementation is preferred …

Proposed Hybrid Loop Filter Approach



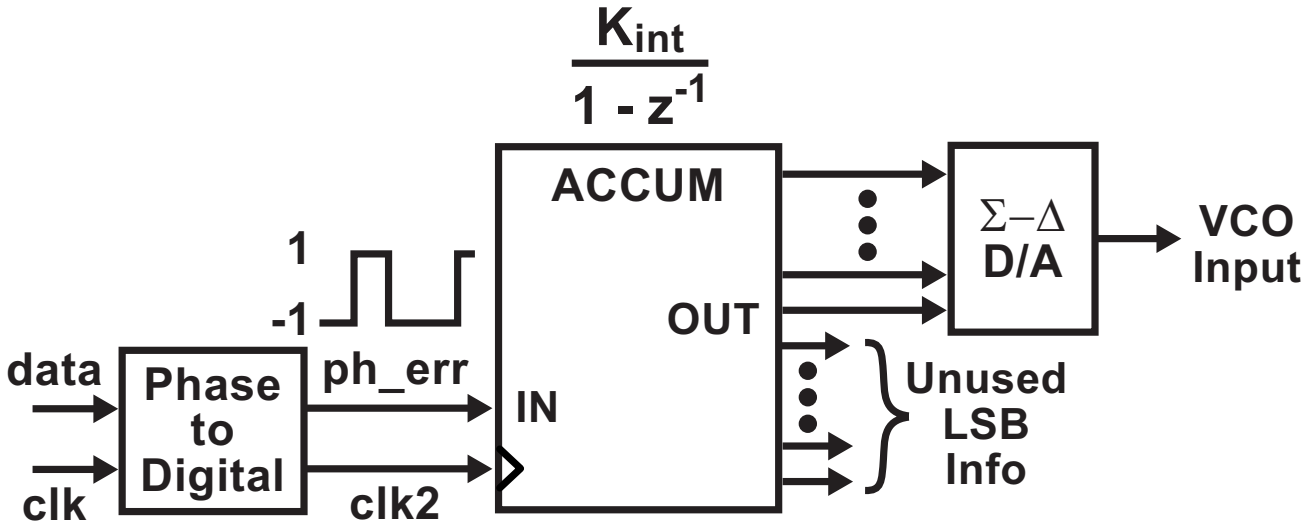
- **Lead/Lag filter can be decomposed into two paths**
  - **Feedforward path (high bandwidth, easy in analog domain)**
  - **Integrating path (low bandwidth, hard in analog domain)**
    - Digital domain provides a compact implementation

Overall Hybrid Loop Filter Structure



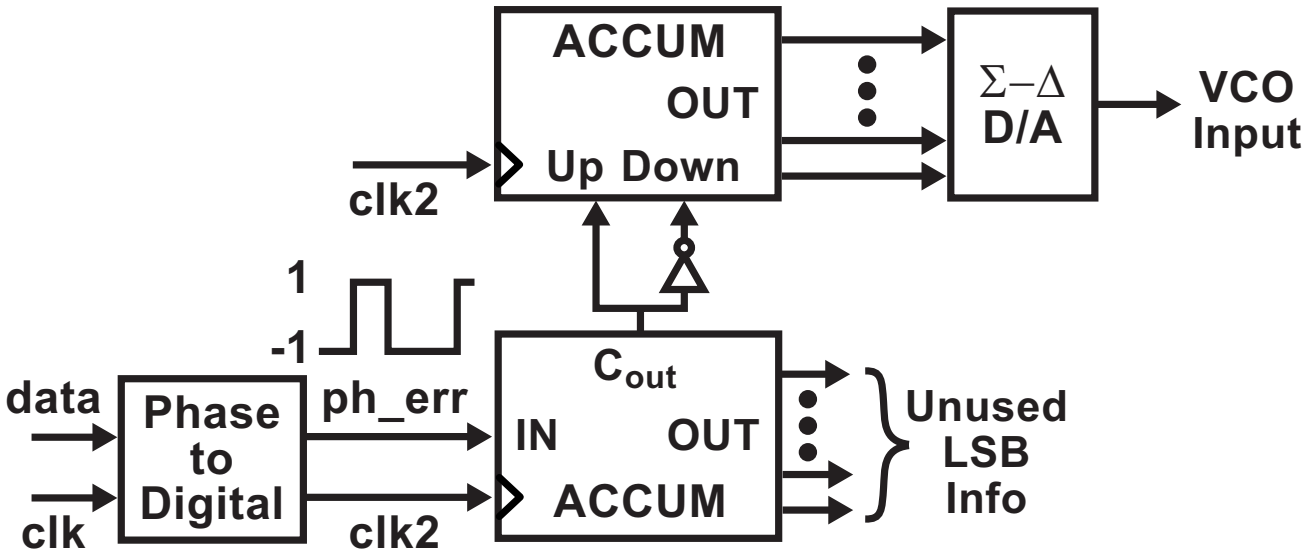
- Accumulator acts as digital integrator
- Sigma-Delta D/A allows high resolution with easy implementation
- Decimator lowers operating speed of accumulator and D/A

Walk Through of Decimator Implementation



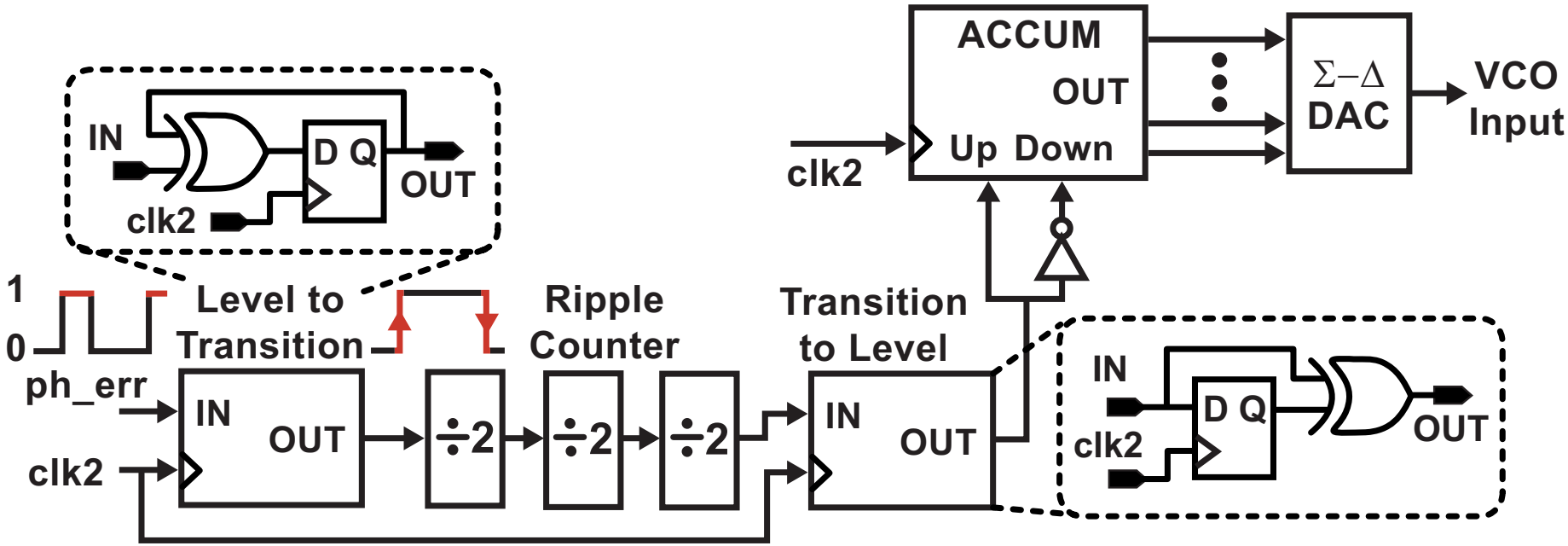
- Consider simply running accumulator at full rate
  - Would need to run at GHz speeds in 0.25u CMOS
    - High power!
- Key observations
  - Accumulator output has higher resolution than needed by VCO input
  - We do not need the LSB portion of the accumulator output

Split Accumulator into LSB and MSB Sections



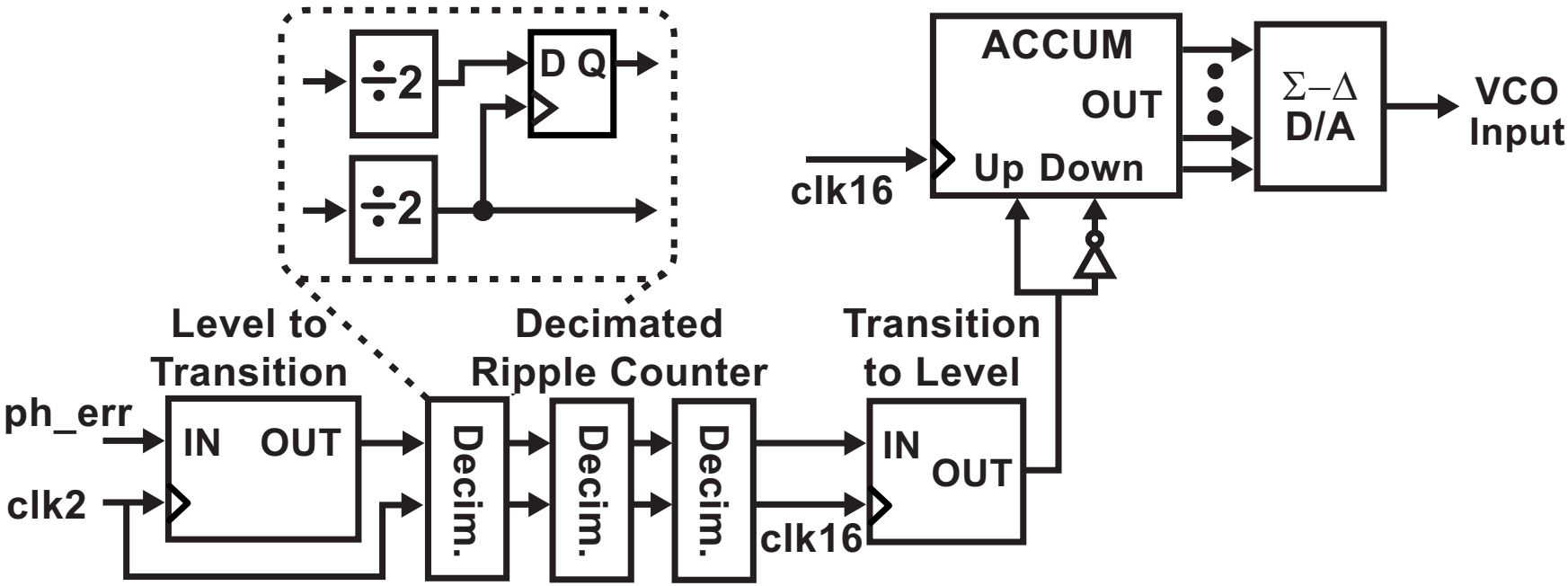
- **Key observations:**
  - We only need one line of communication between LSB and MSB sections (i.e., carry signals)
  - We only need to generate the carry out signal of the LSB section
  - We can replace the LSB section with a decimator structure and still preserve all relevant information

First Pass at Decimator Implementation



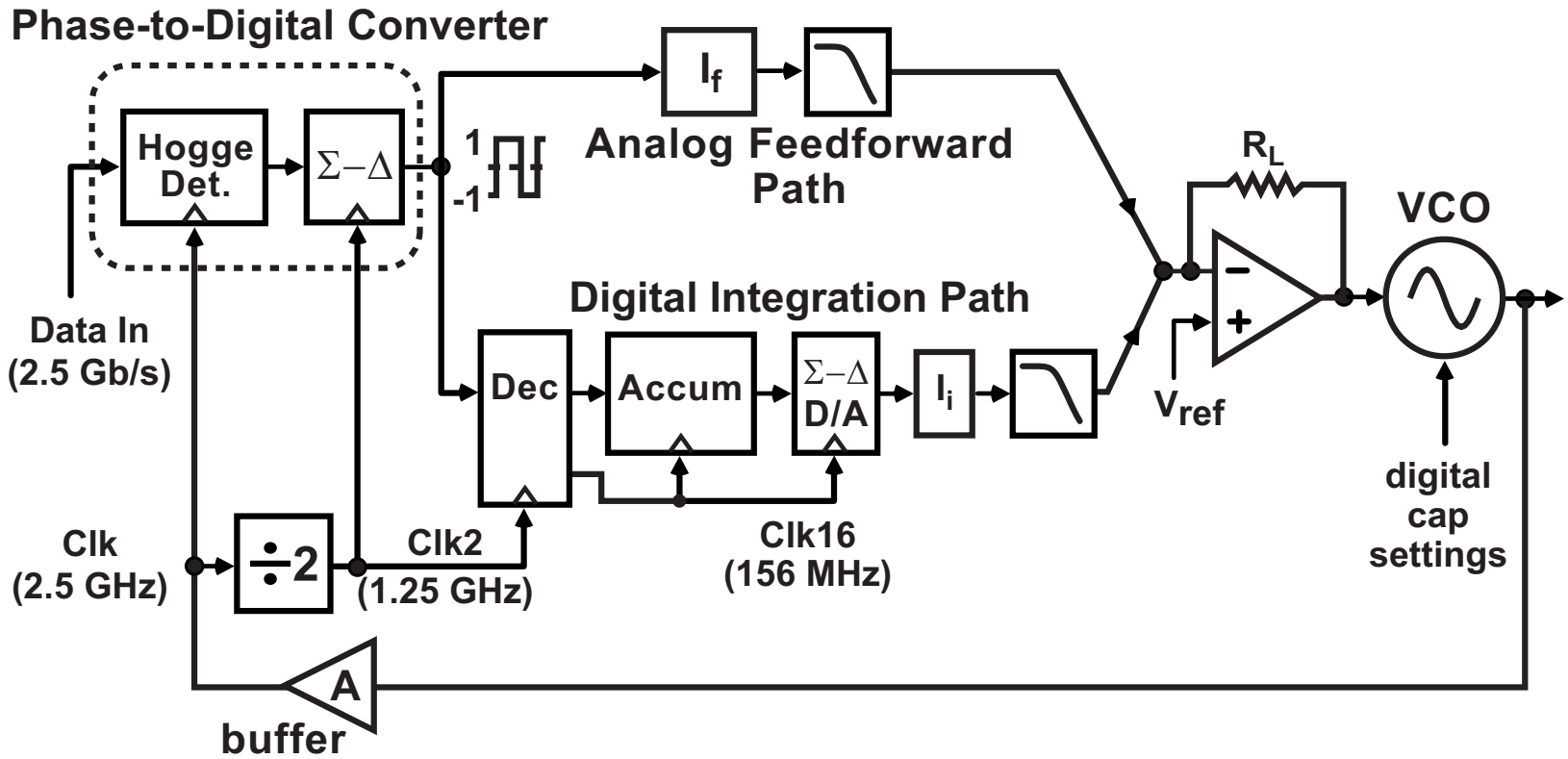
- We can implement the LSB accumulator with a ripple counter
  - Issue: ripple counter counts transitions
  - Solution: use appropriate translators to convert between voltage levels and transitions
- Next step: we have achieved an efficient LSB accumulator, but not a lower operating frequency

Final Decimator Architecture



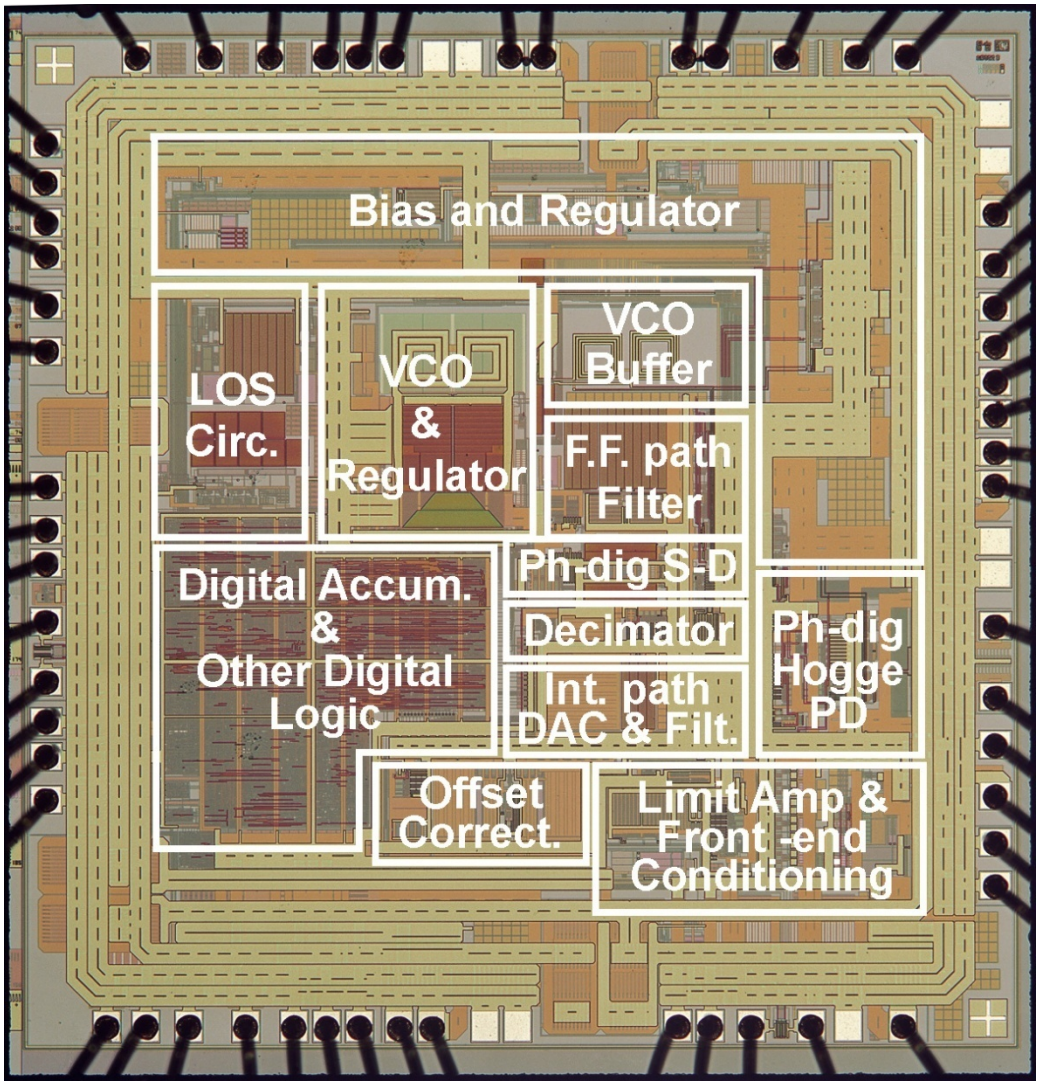
- Re-clock divide-by-2 stages of ripple counter at progressively lower clock frequencies
  - Aligns ripple counter transitions to lower frequency clock boundaries
- MSB Accumulator now runs at 1/16 of the original frequency in the above example

Overall CDR Architecture



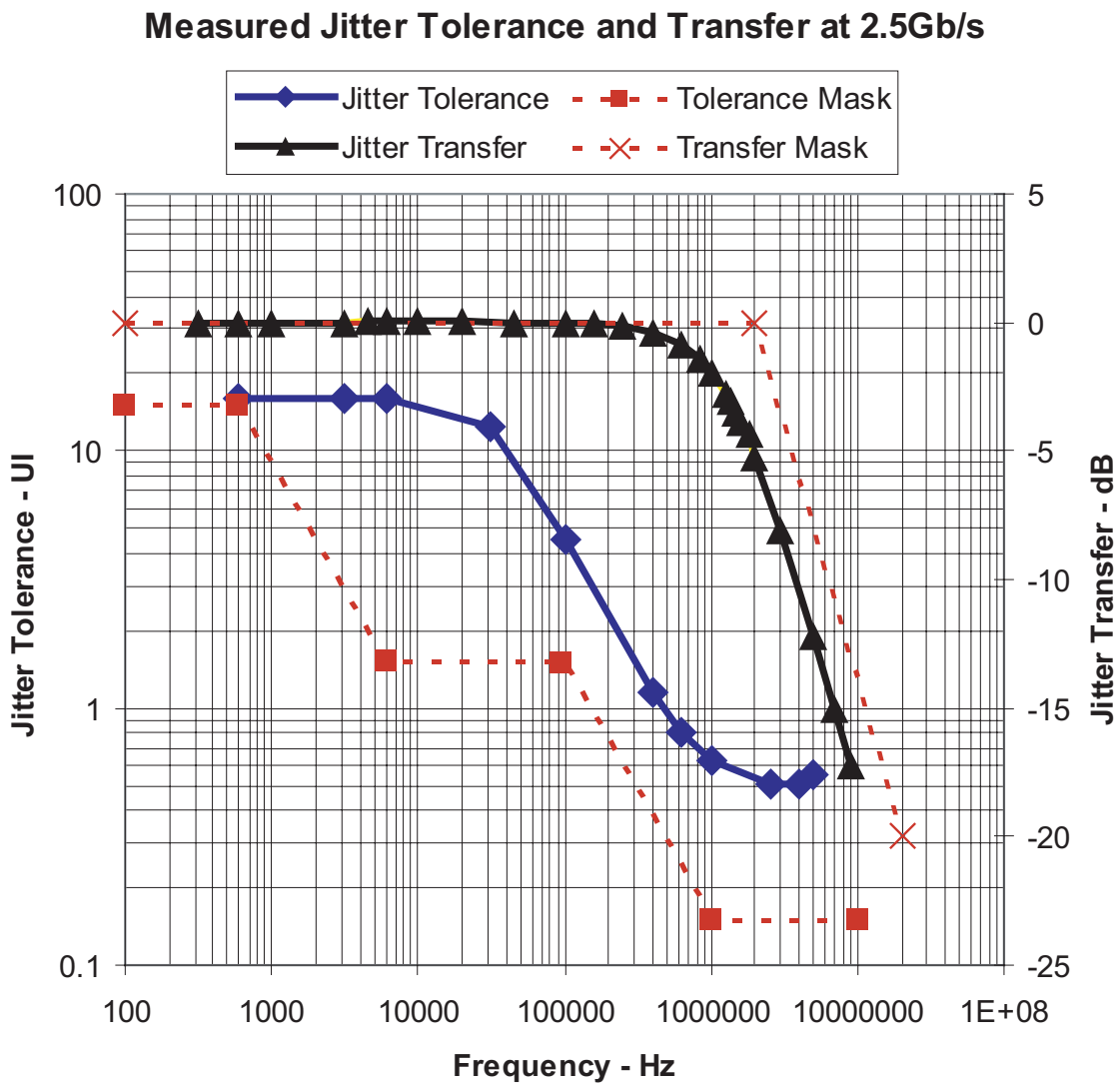
- We have achieved:
  - A low power, compact, highly linear phase-to-digital structure
  - A low power, compact, highly configurable hybrid loop filter
  - Compatible with existing hybrid VCO structures achieving excellent phase noise in 0.25u CMOS

Die Photo



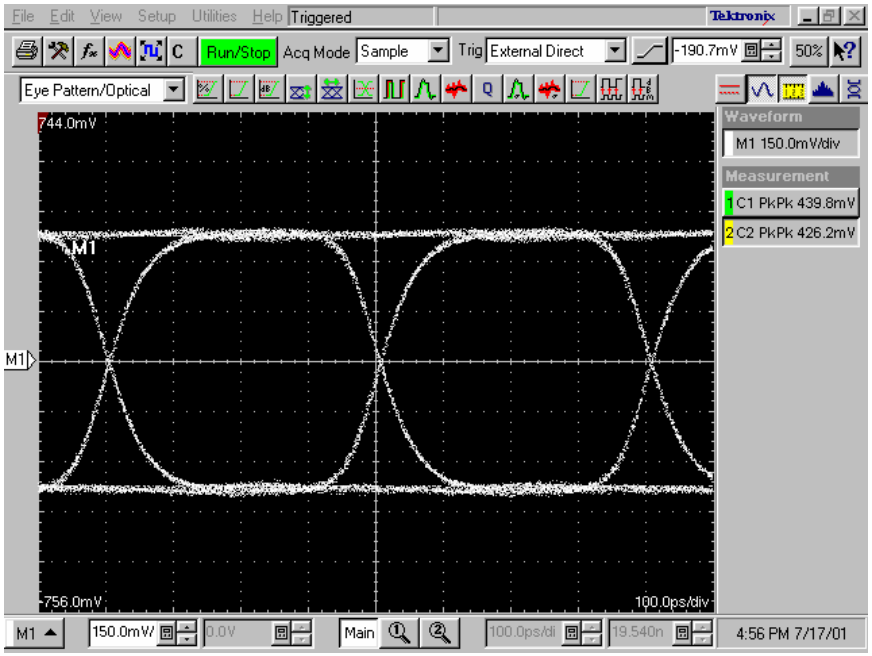
- Supply Voltage
  - 2.5 V or 3.3 V
- Typical current
  - 170 mA (2.5 Gb/s)
- Supported data rates
  - 2.7 Gb/s (FEC)
  - 2.5 Gb/s (OC-48)
  - Gigabit Ethernet
  - 622 Mb/s (OC-12)
  - 155 Mb/s (OC-3)
- Minimum input
  - 10 mV (differential)
- Package size
  - 5mm X 5mm

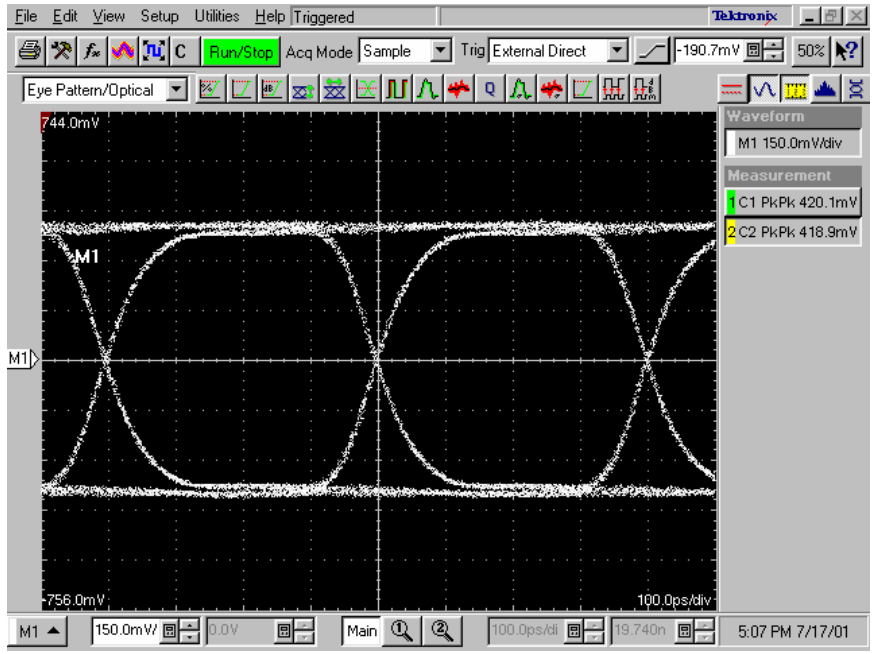
Measured Jitter Tolerance and Transfer at 2.5 Gb/s



- SONET performance specifications met at all data rates:
- Jitter transfer (typ.)
  - Peaking < 0.03 dB
- Jitter tolerance (min)
  - > 0.3 UI_{pp} (> 1 MHz)
- Jitter generation
  - 3 mUI rms (typ.)
  - 25 mUI pp (typ.)

Measured Eye Diagrams at 2.5 Gb/s



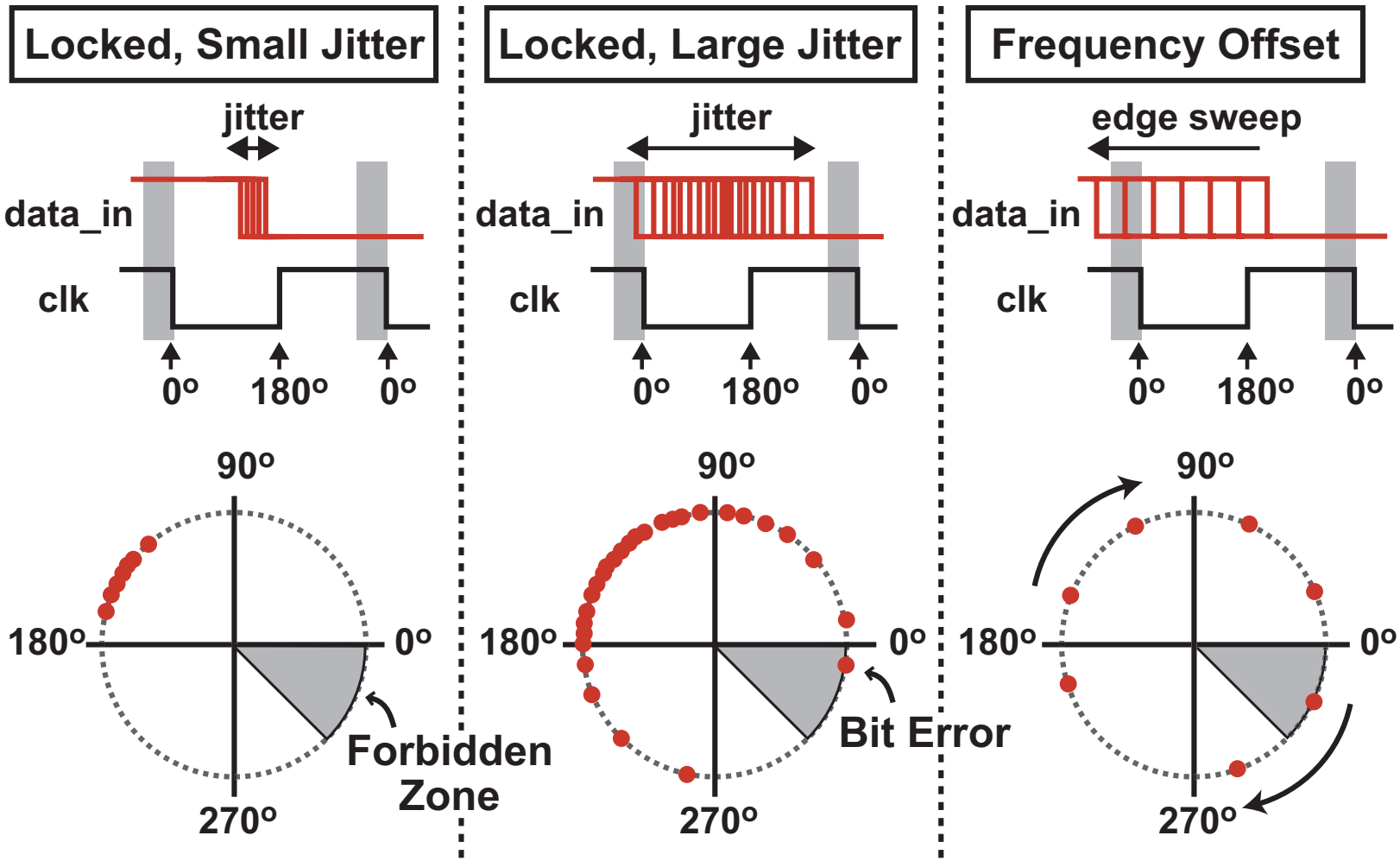


- **Best Case Conditions**
  - Input data: 2 Vp-p diff.
  - Pattern: PRBS 2^7-1
  - Temperature: 25° C
  - Jitter: 1.2 ps RMS
- **Worst Case Conditions**
  - Input data: 10 mVppd
  - Pattern: PRBS 2^{31}-1
  - Temperature: 100° C
  - Jitter: 1.4 ps RMS

What about the digital cap settings?

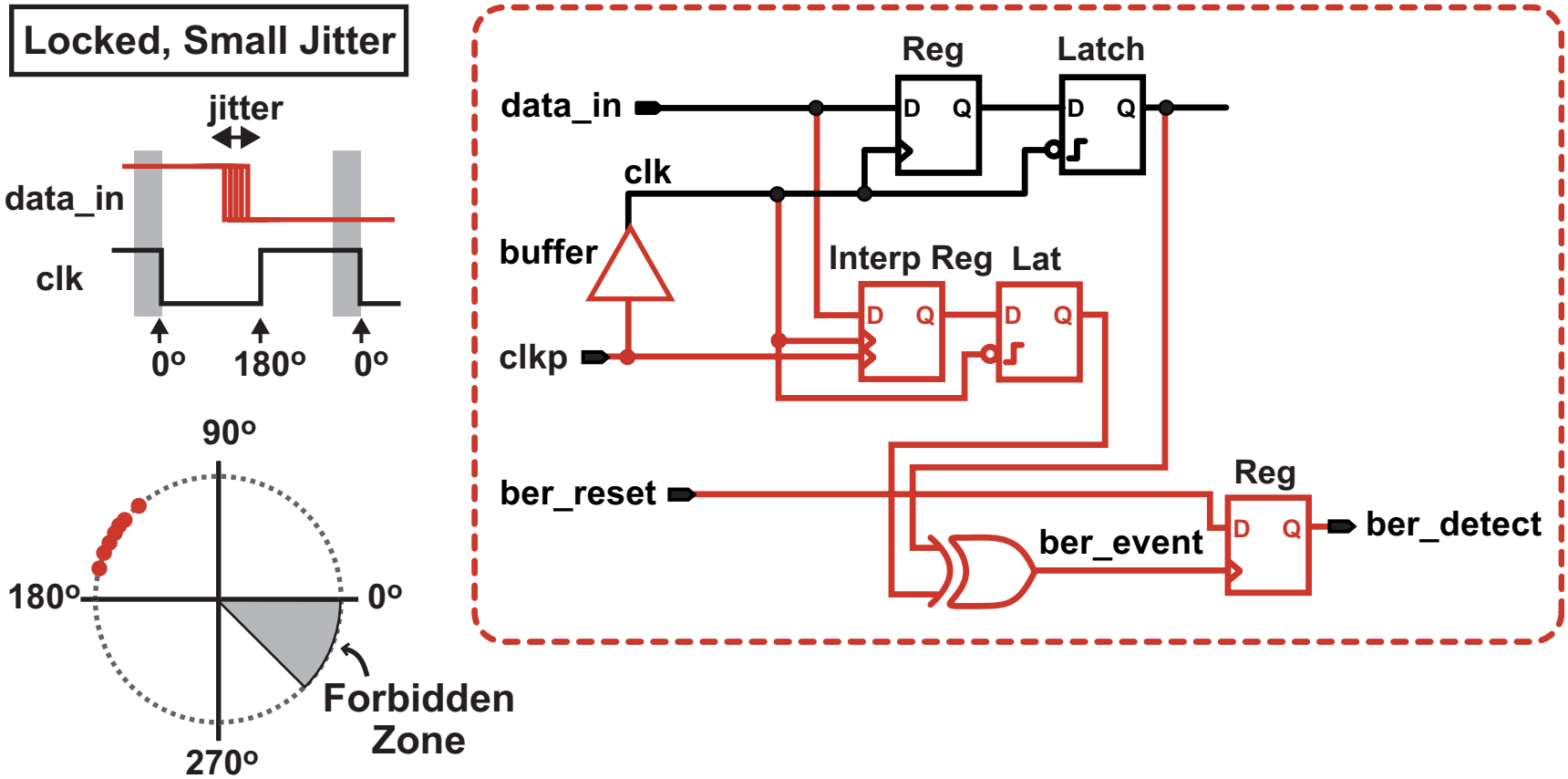
--- Digital frequency acquisition example ---

Referenceless Frequency Acquisition



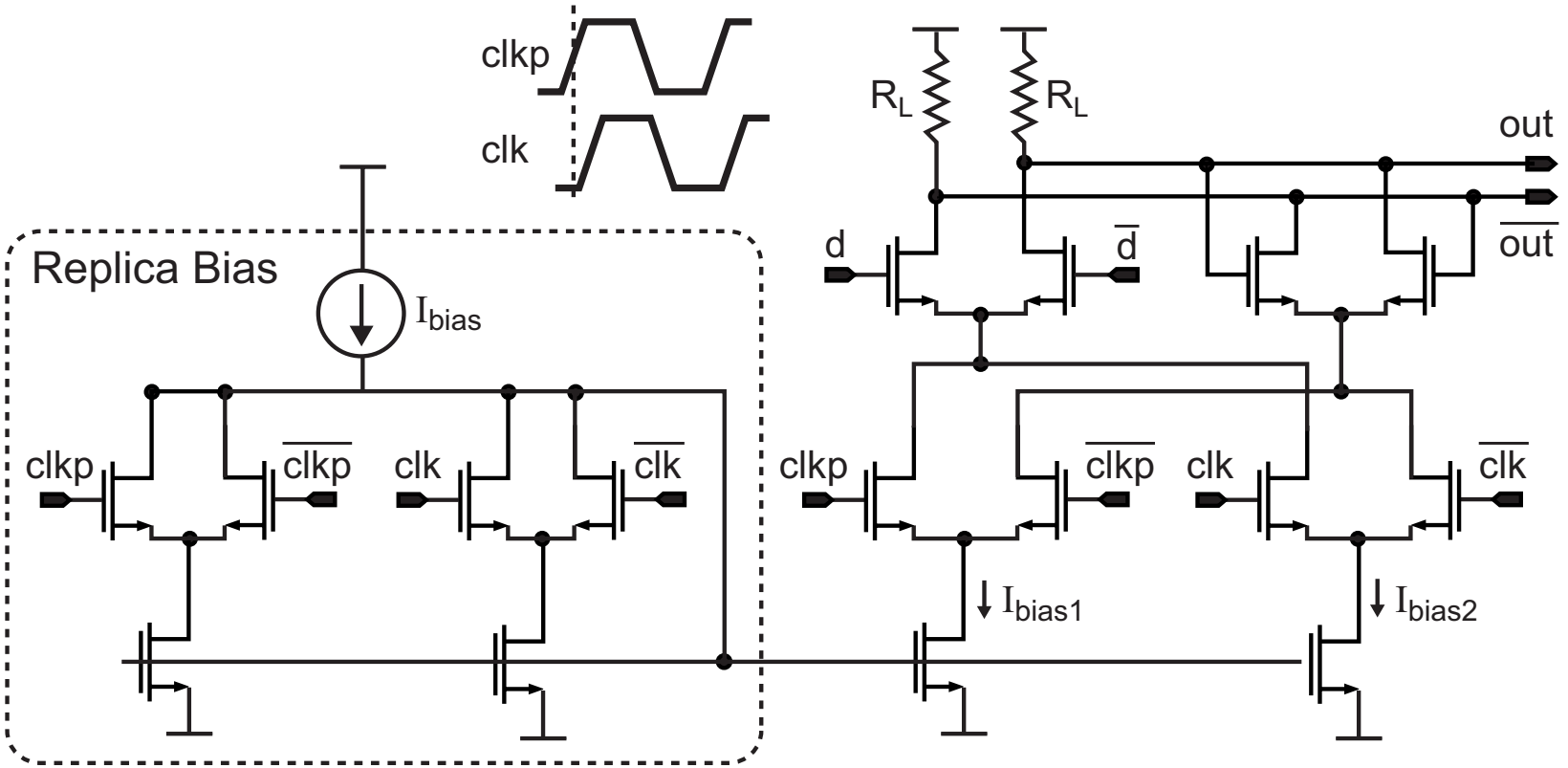
- Utilize a "Forbidden Zone" to infer frequency lock
  - Use this information to determine digital cap settings

A Bit Error Detector Based on Forbidden Zone



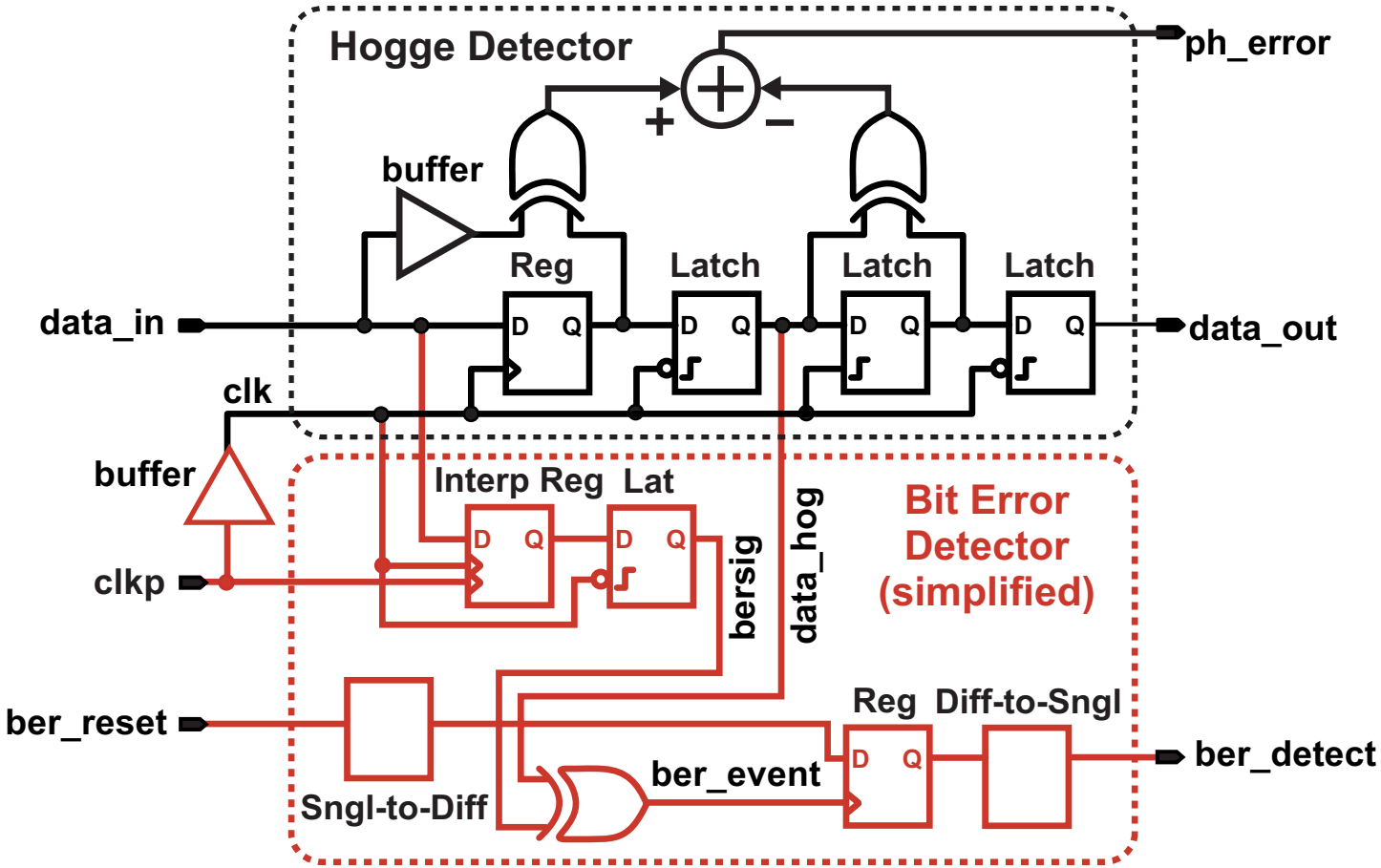
- Key idea: sample input data at two different times
  - Change *ber_detect* value if the two results are different
- Implementation: achieve delayed clock with less than one buffer delay by using interpolative register

Interpolative Latch



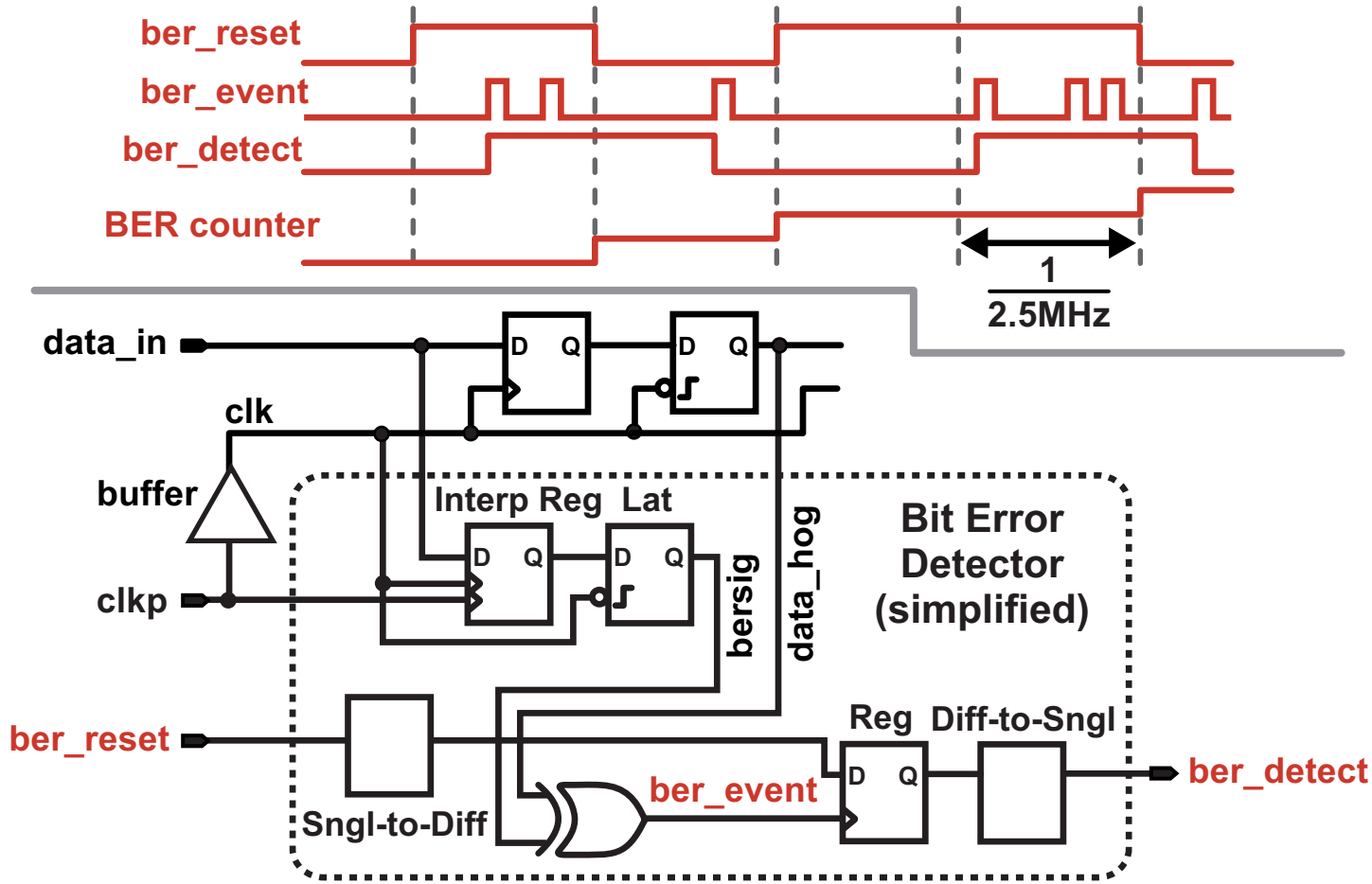
- **Effective latch time occurs *between* rising edges of input clocks (i.e., *clk* and *clkp*)**
  - **Adjustment of I_{bias1}/I_{bias2} allows adjustment of latch time**
    - Choose $I_{bias1} = I_{bias2}$ in this application

Combined Hogge Detector and Bit Error Detector



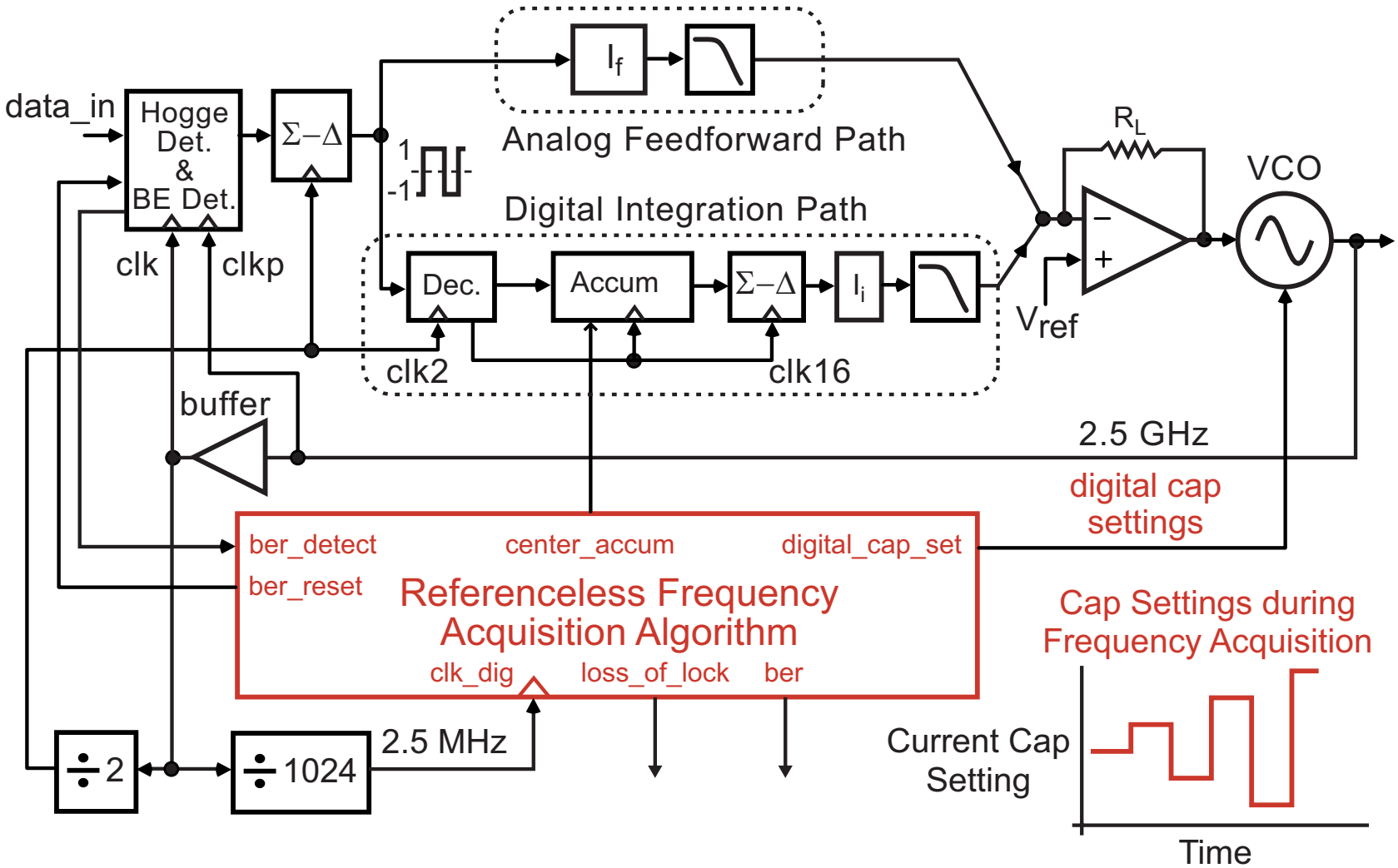
- Sensing of bit errors adds minimal overhead to Hogge Det.
  - Note: Diff-to-Sngl and Sngl-to-Diff converters interface to lower speed signals (*ber_reset* and *ber_detect*)

Sensing Bit Errors



- For robust operation, only detect whether *at least one* bit error occurs within period of 2.5 MHz clock
  - BER Counter increases by one if the above occurs

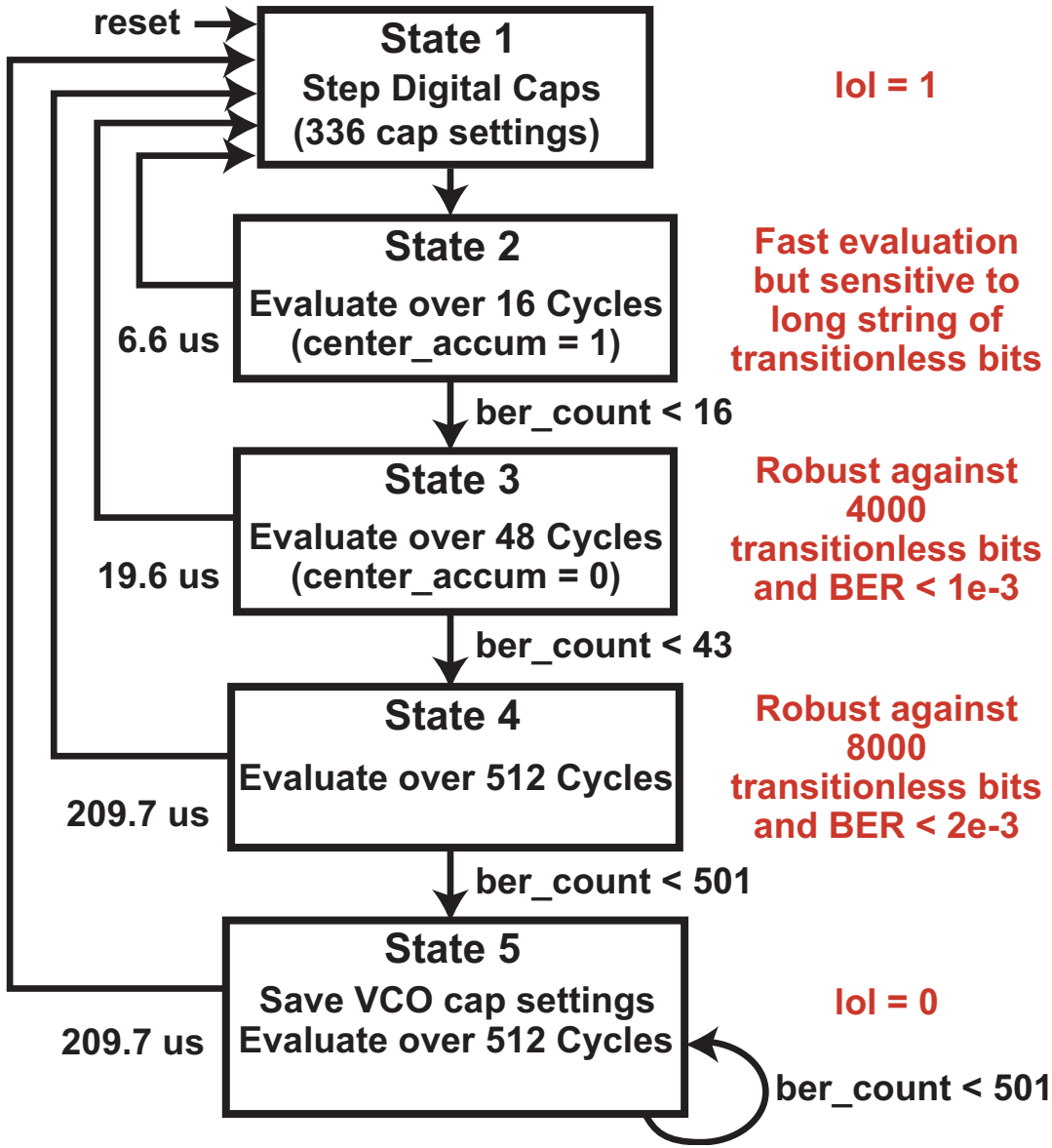
Overall System with Referenceless Frequency Acq.



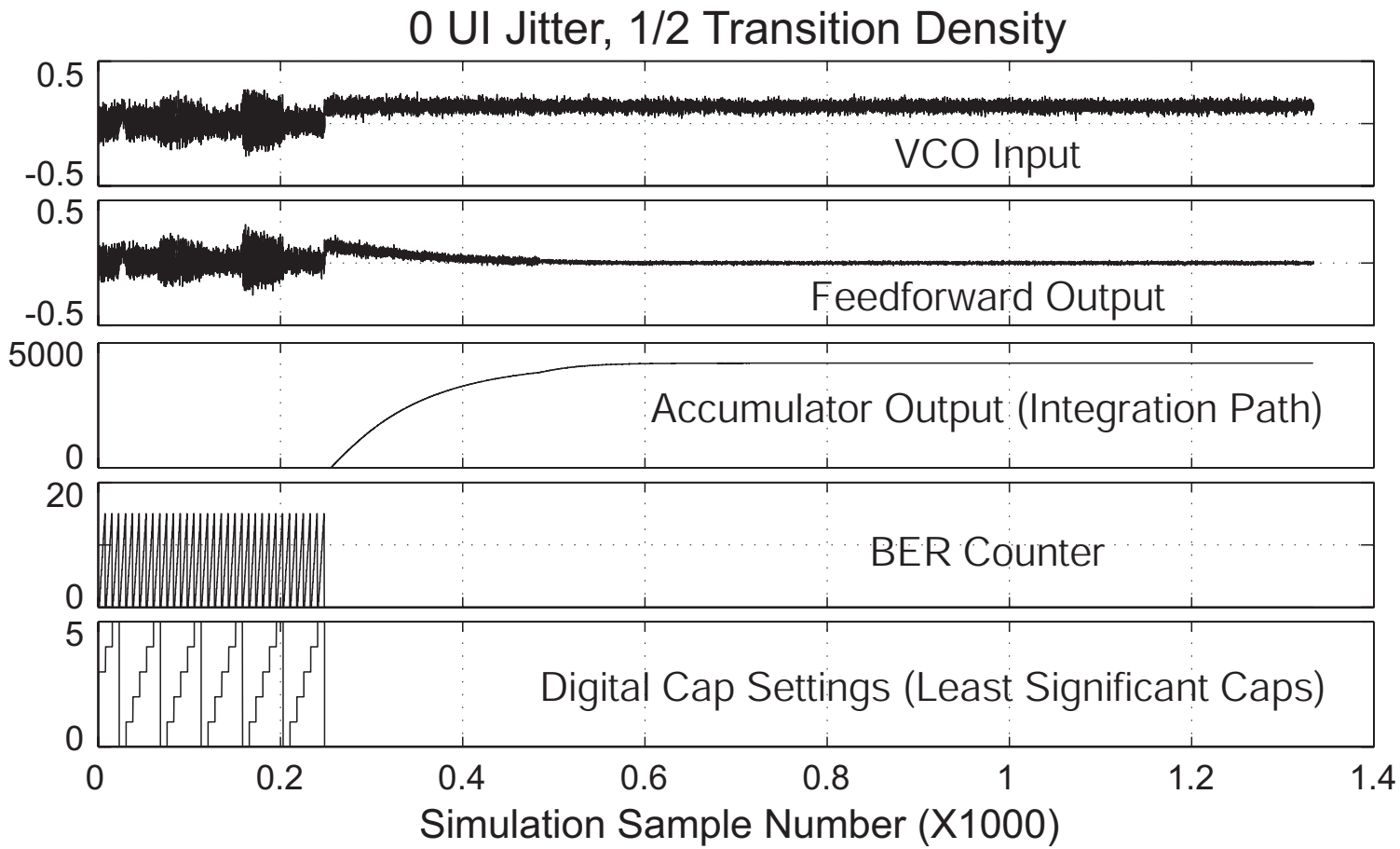
- **Digital cap settings are updated as shown when bit error counts exceed a threshold value**

State Diagram for Referenceless Frequency Acq.

- Fast initial check of cap setting
  - Allows speedy visitation of all cap settings
  - Assumes a wrong cap setting will usually yield a high BER count
- Progressively slower checks of cap setting
  - Protects against false selection of a cap setting

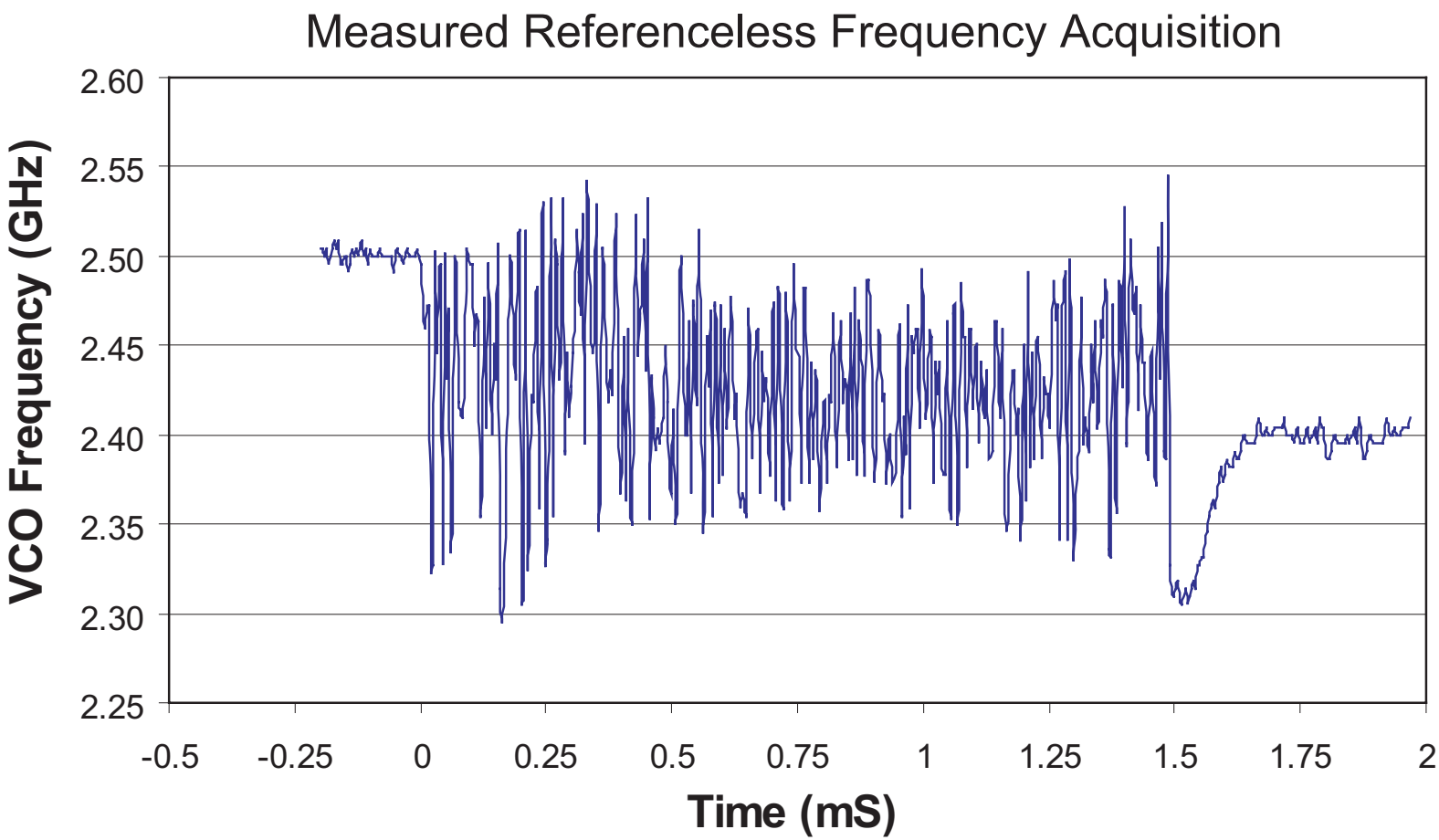


Example: No Jitter, High Transition Density



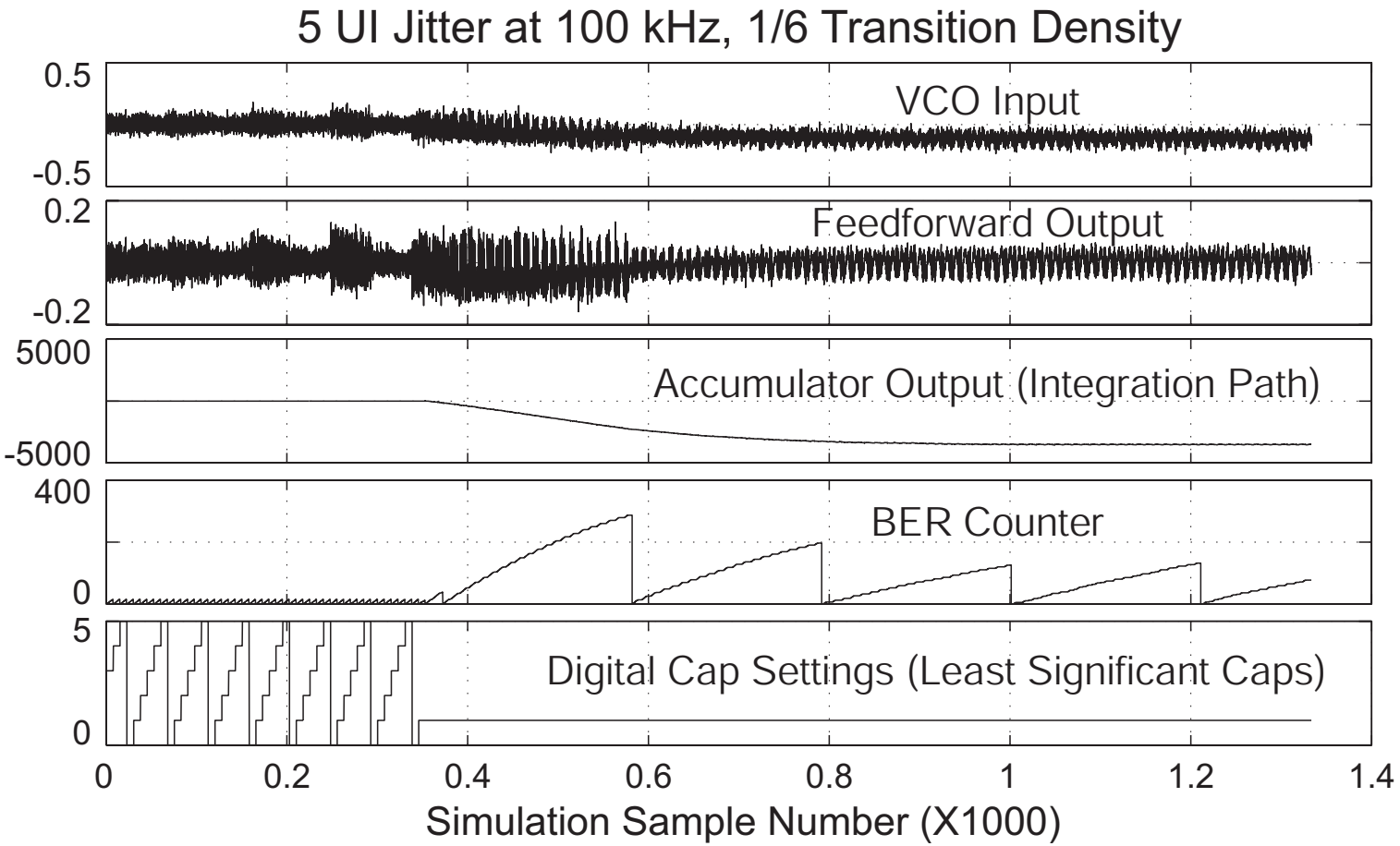
- **BER counter goes to zero when correct digital cap setting is achieved**

Measured Referenceless Frequency Acquisition



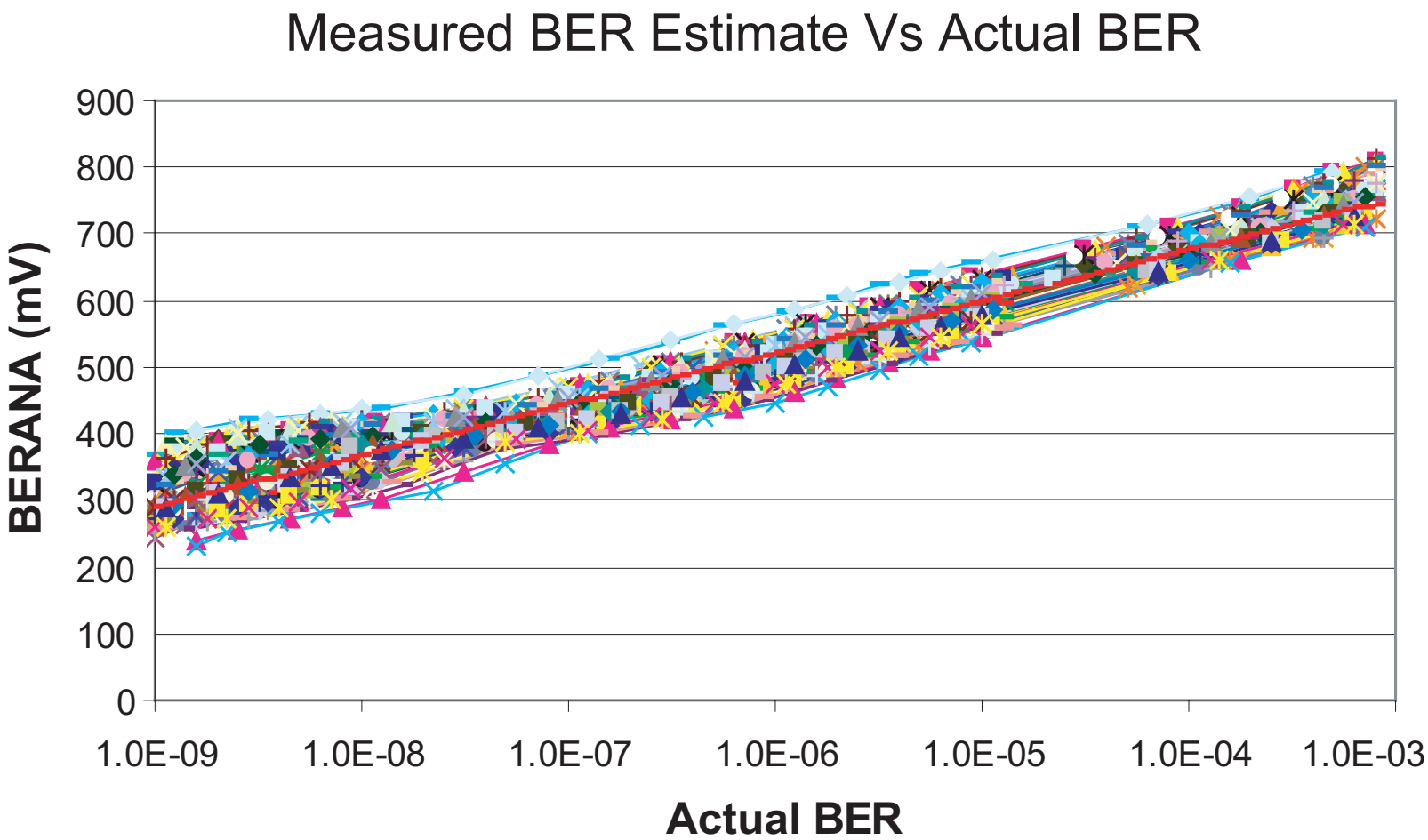
- Change data input from 2.5 Gbit/s to 2.4 Gbit/s
  - In this case, frequency acquisition completes in < 2 ms

Example: High Jitter, Low Transition Density



- **BER Counter continues to have non-zero values even after correct digital cap setting is achieved**
  - **This information can be used to estimate BER of CDR**

Measured BER Estimation versus Actual BER



- **Above measured results occur across:**
  - **Worst case split lot corners**
  - **Temp: -40 to 85 degrees C, Voltage supply: 1.62 to 3.63 V**

Conclusion

- **Mixed-signal techniques allow high performance to be achieved with low power and compact area**
  - **Phase-to-digital converter: combined Hogge PD and First Order Sigma-Delta A/D**
  - **Hybrid Loop Filter**
  - **All-digital frequency acquisition with minimal overhead**
- **Measured results confirm high performance**
  - **All SONET specifications met with 1.2 ps typical rms jitter**
  - **Referenceless frequency detection with BER monitor**

Mixed-signal design philosophy:
Leverage *both* analog and digital circuits such that their relative strengths are fully utilized