Short Course On
Phase-Locked Loops and Their Applications
Day 5, PM Lecture

Advanced PLL Examples (Part II)

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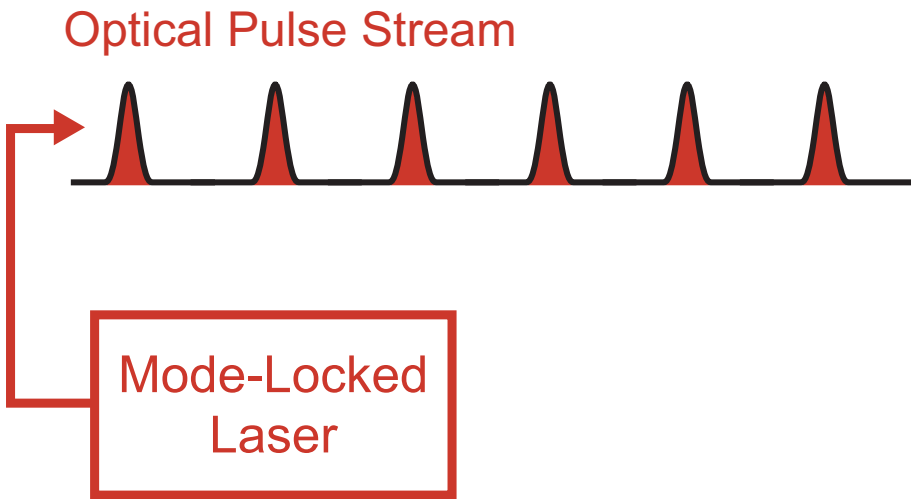
August 15, 2008

Outline

- **Optical/Electrical Phase-Locked Loops**
- **High Speed CDR Techniques**
- **VCO-based A/D Conversion**
- **MEMS-based clocking**

Optical/Electrical Phase Locking

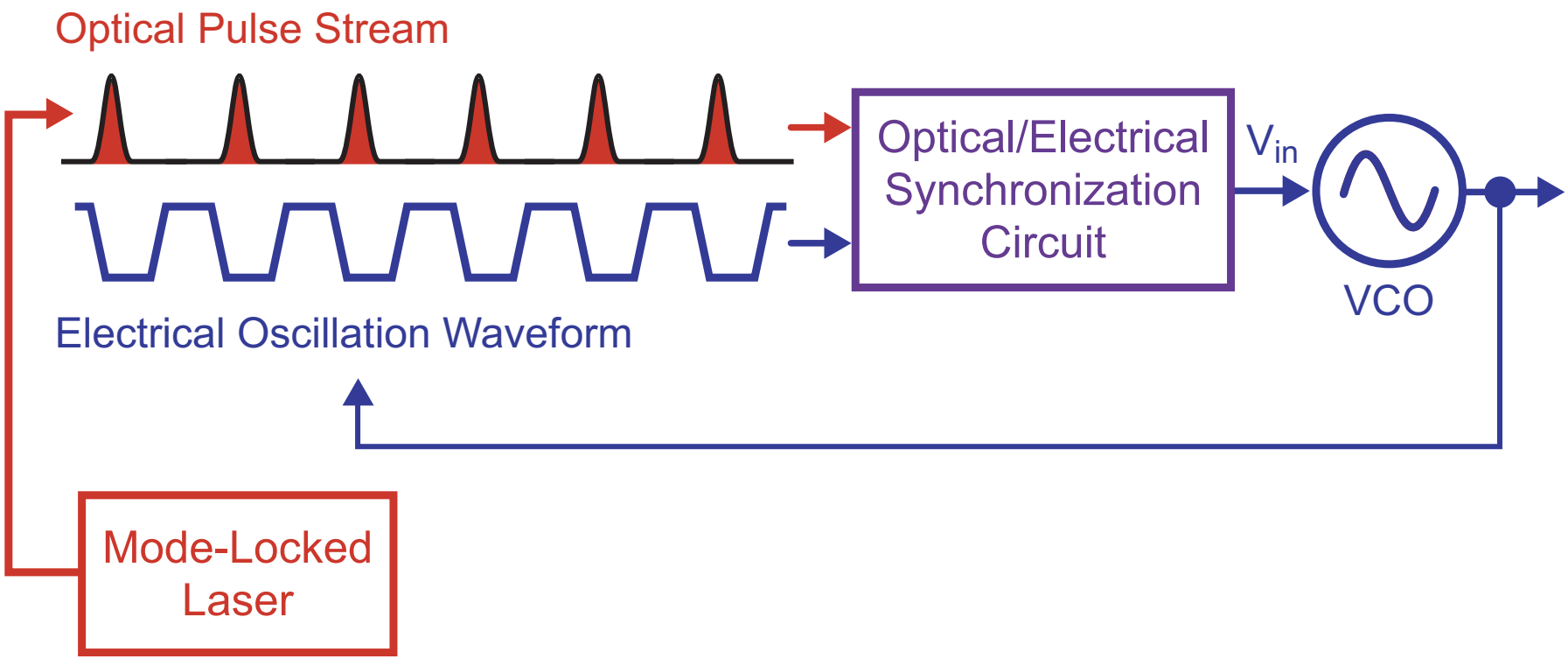


- **Mode-locked lasers provide optical clock streams with excellent jitter characteristics**
  - **14 fs jitter (10 Hz to 375 MHz) has been achieved**

    J.B. Schlager et. al, Opt. Lett. 28, 2411-2413 (2003)

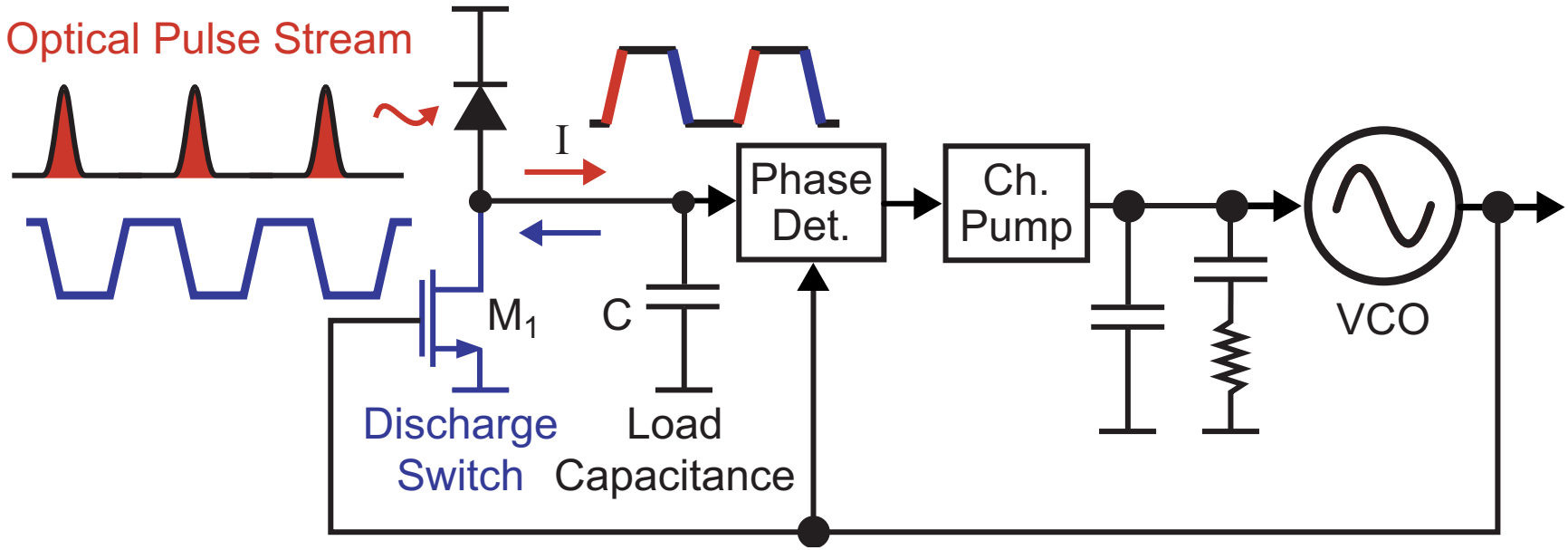
Can we lock an electrical clock to the optical pulse stream AND maintain low jitter?

Optical/Electrical Phase Locked Loops



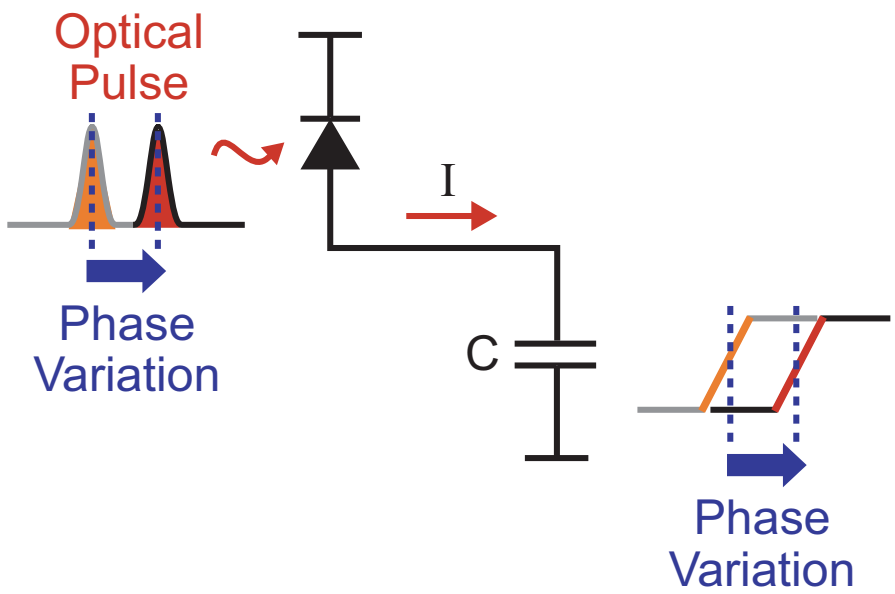
- **Generate a frequency tunable electronic clock source by using a voltage controlled oscillator (VCO)**
- **Lock VCO output to pulse stream using an optical/electrical synchronization circuit**

Method 1 of Implementing the Synchronization Circuit



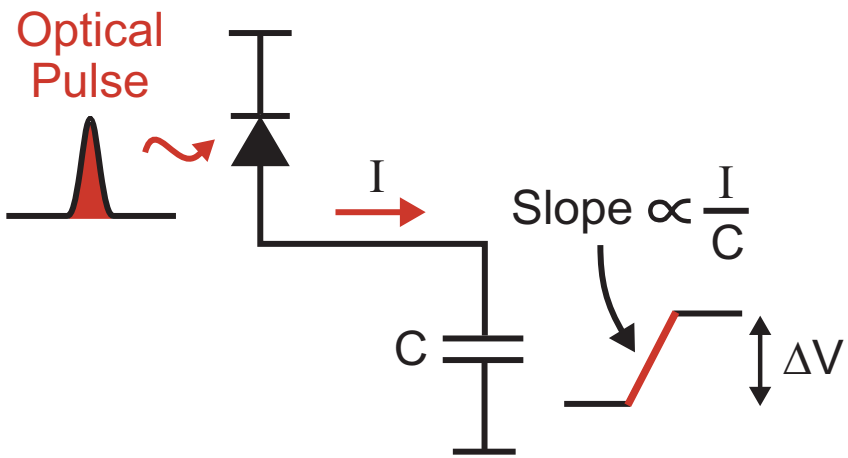
- Create an electrical square wave reference signal by using a photodiode and discharge switch
- Lock the VCO output to the electrical reference signal by using a conventional electronic phase locked loop

Key Idea of Method 1: Measure Phase Based on Edges



- **Relative phase positions of optical pulses are captured by the edge locations of the electrical reference waveform**

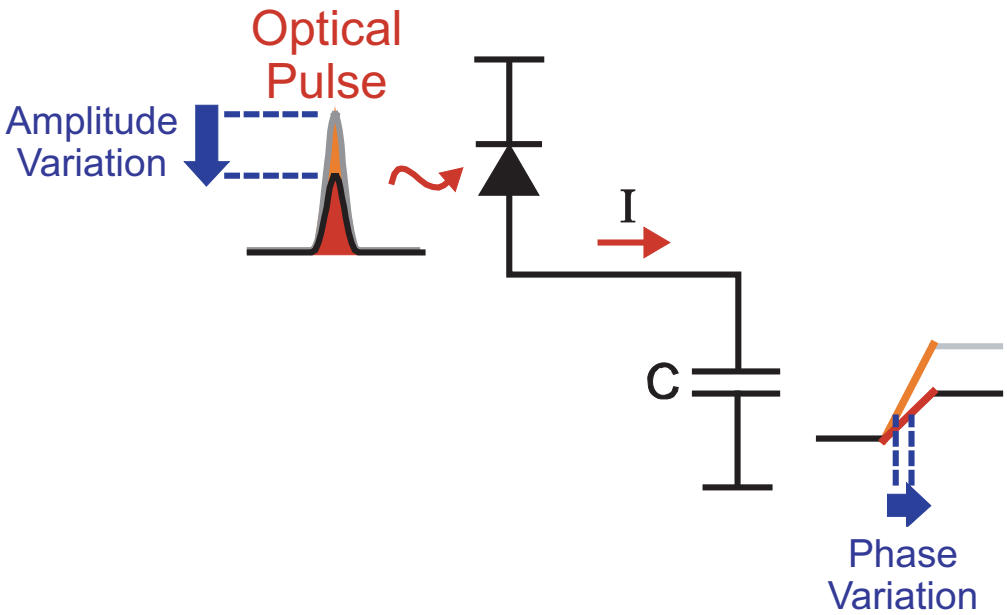
Issue 1: Noise



- The slope of the transition edges is limited by the current/capacitance ratio at the photodetector output
- Higher edge slopes are desirable to achieve low noise
  - Voltage noise present in the reference waveform translates to timing jitter according to the edge slope

Achievable noise performance is limited by the I/C ratio of the electronics (i.e., photodiode and the capacitive load it drives)

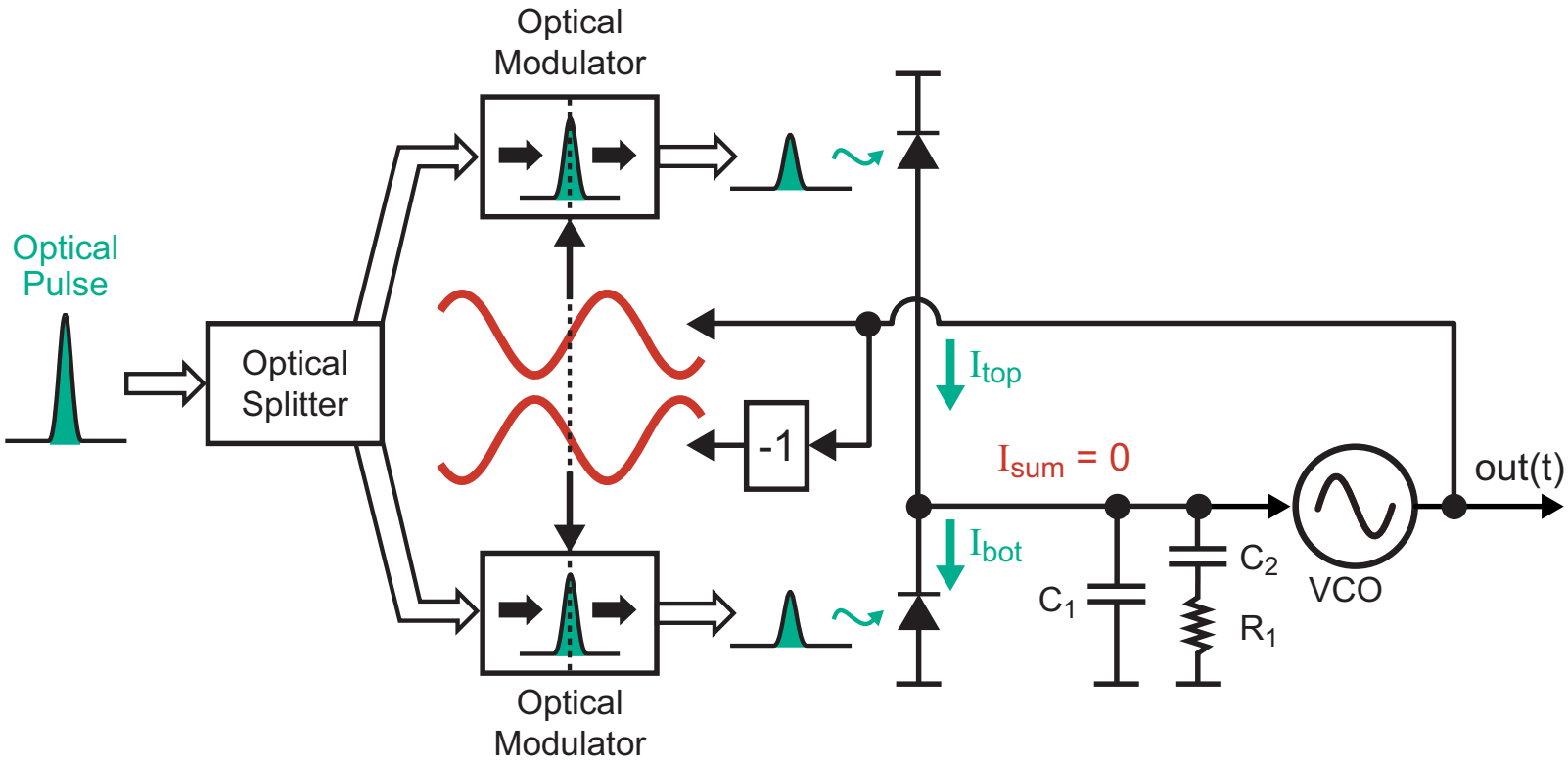
Issue 2: Sensitivity to Amplitude Variation



- **Practical pulse streams from mode-locked lasers exhibit undesired amplitude variation**
- **Phase detection based on the edge-based approach above translate pulse amplitude variation into phase variation**

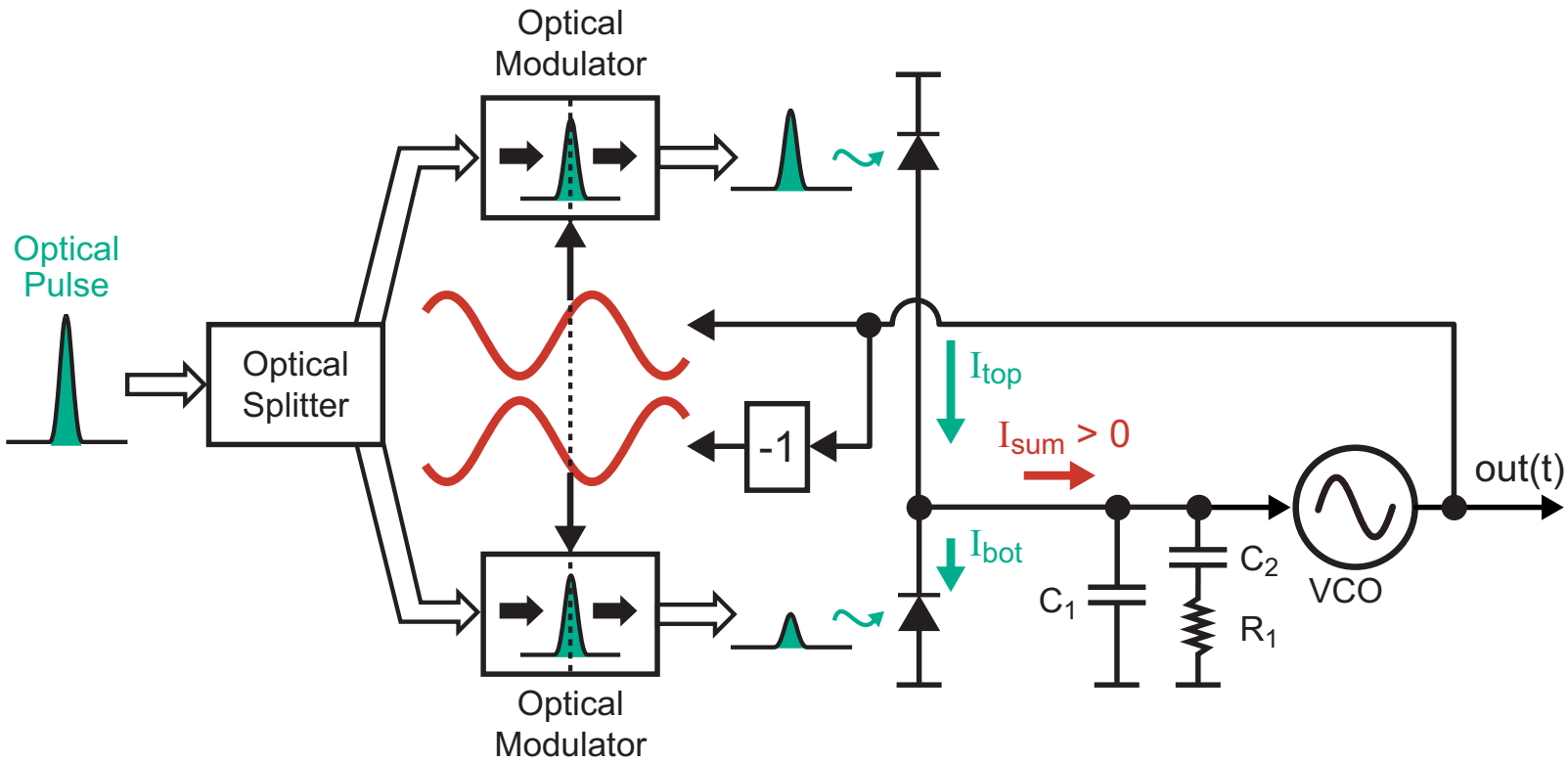
Can We Do Better?

Proposed Approach



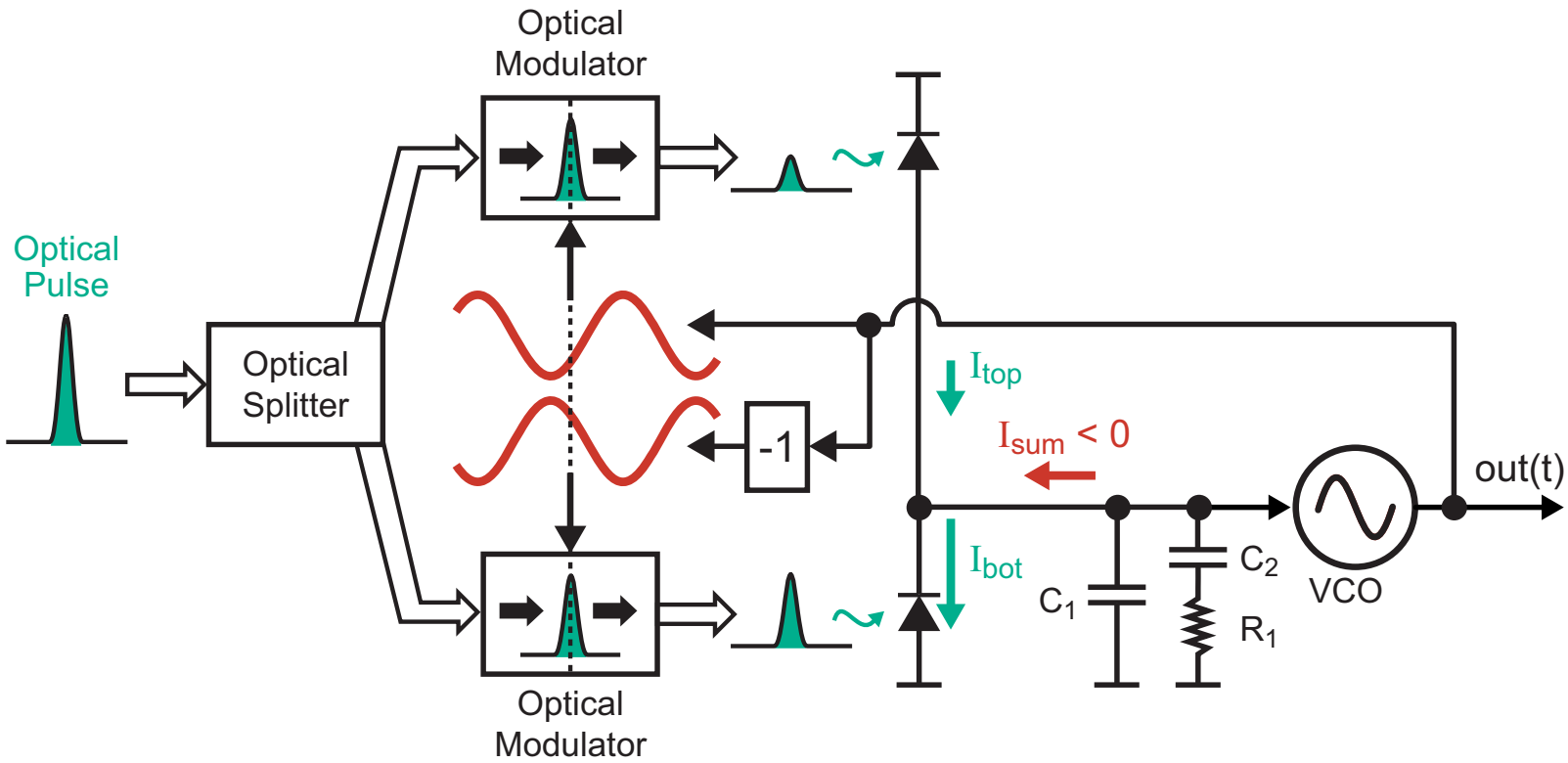
- **Move phase comparison into the optical domain**
  - **Passing an optical pulse through an optical modulator effectively samples its input value at the time**
- **Use photodetectors to detect the average *power* of the modulator outputs**

Impact of VCO Output Phase Being Too Early



- An imbalance of modulator output power levels causes a difference in current between the top and bottom photodetectors
  - The resulting current causes the VCO input voltage to rise

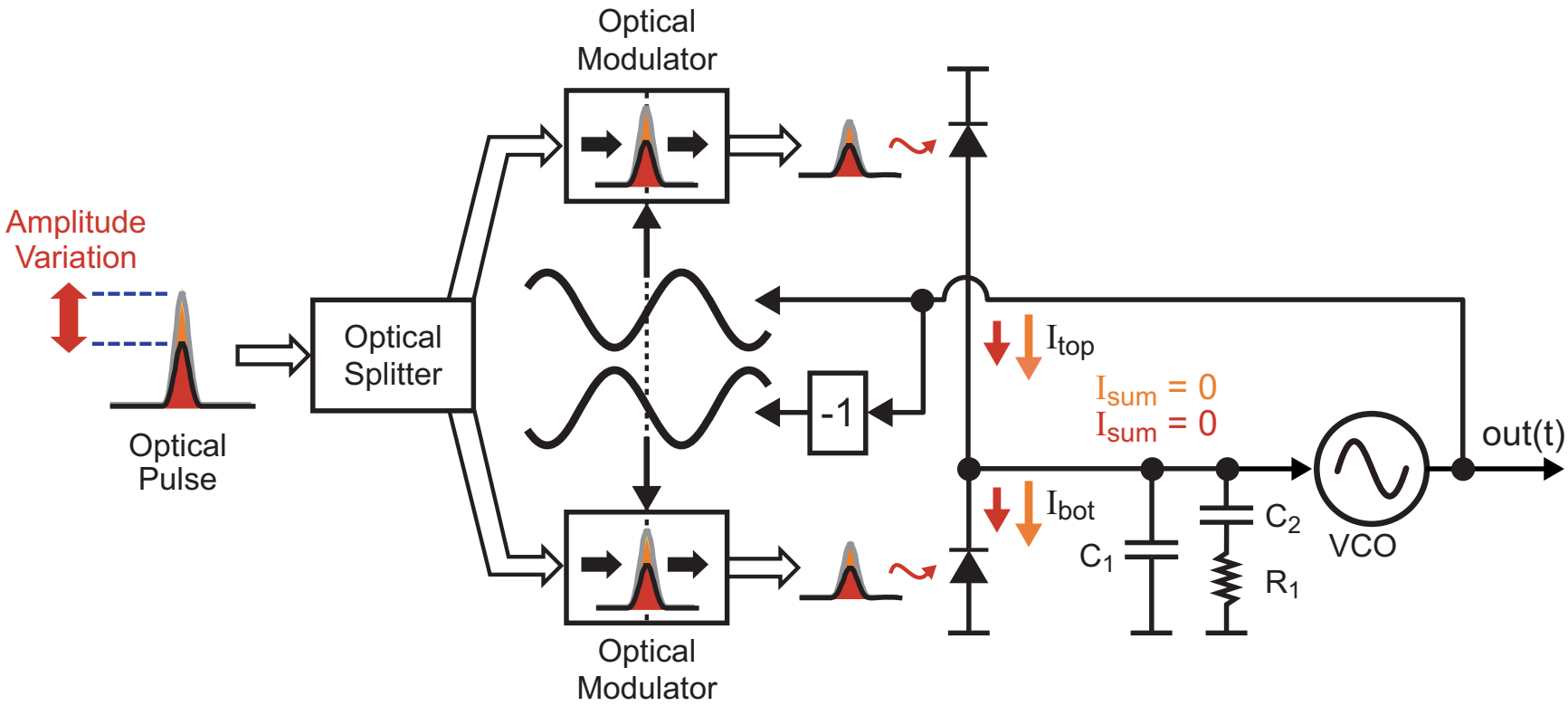
Impact of VCO Output Phase Being Too Late



- **Current imbalance shifts the opposite way, so that the VCO control voltage now starts to fall**

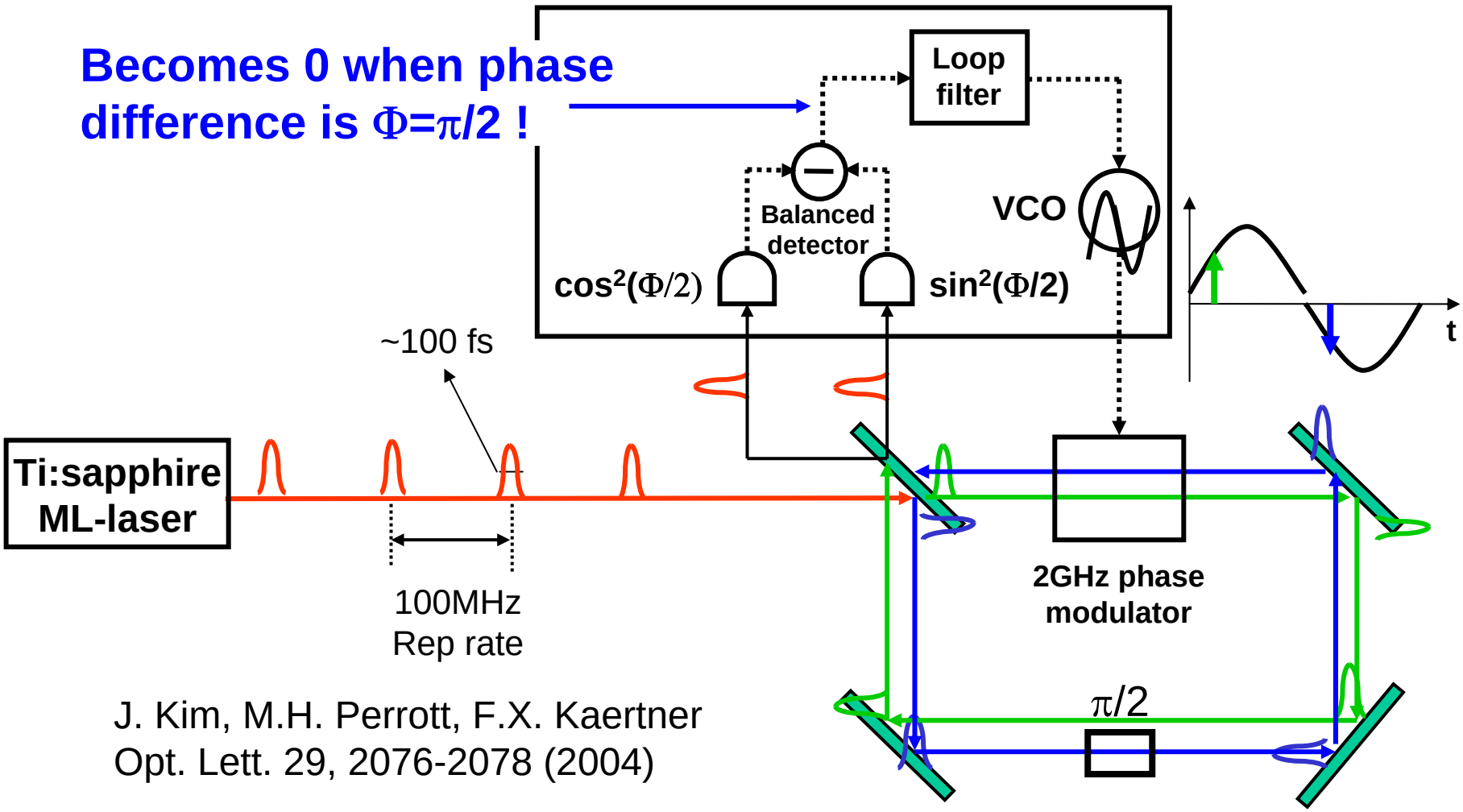
Accurate measurement of phase error is achieved

Approach is Insensitive to Amplitude Variations



- **Amplitude fluctuations impact the top and bottom currents equally (at least to first order)**
  - **The VCO control voltage remains undisturbed**

Actual Implementation (Jung-Won Kim)

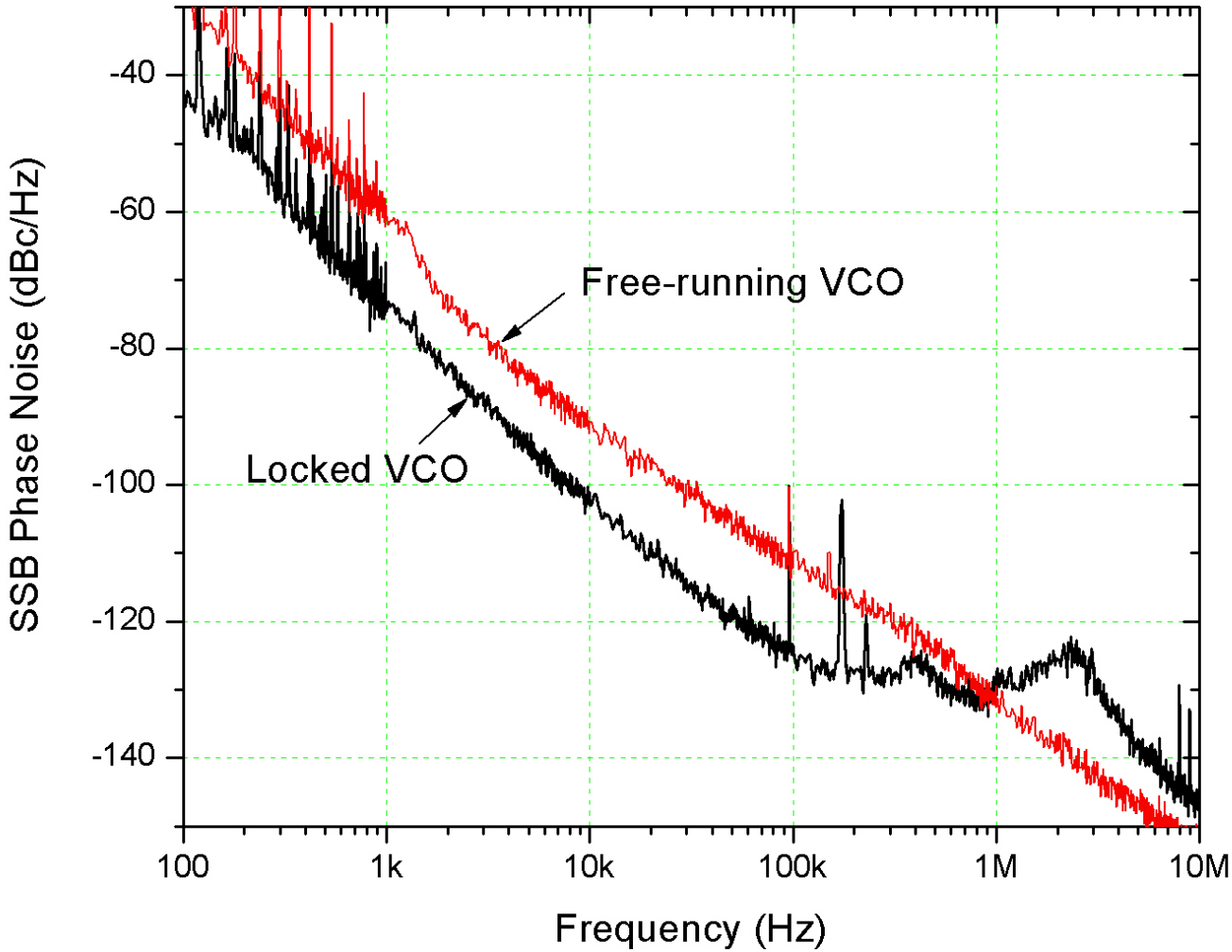


J. Kim, M.H. Perrott, F.X. Kaertner
Opt. Lett. 29, 2076-2078 (2004)

- **Use Mach-Zehnder interferometer within Sagnac-loop**
  - **Robust against temperature fluctuations**

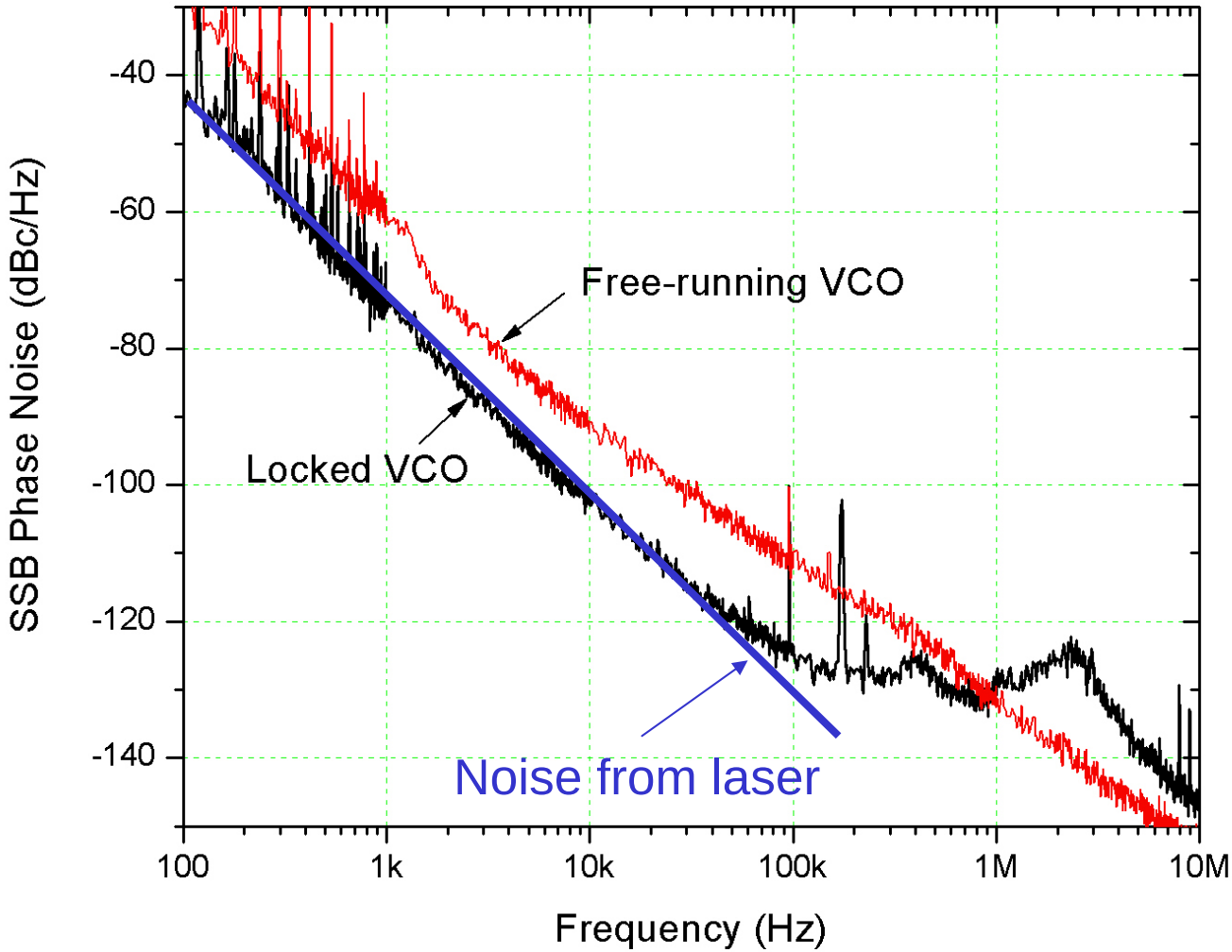
Measured Results

- **Locking is achieved with > 1 MHz bandwidth**



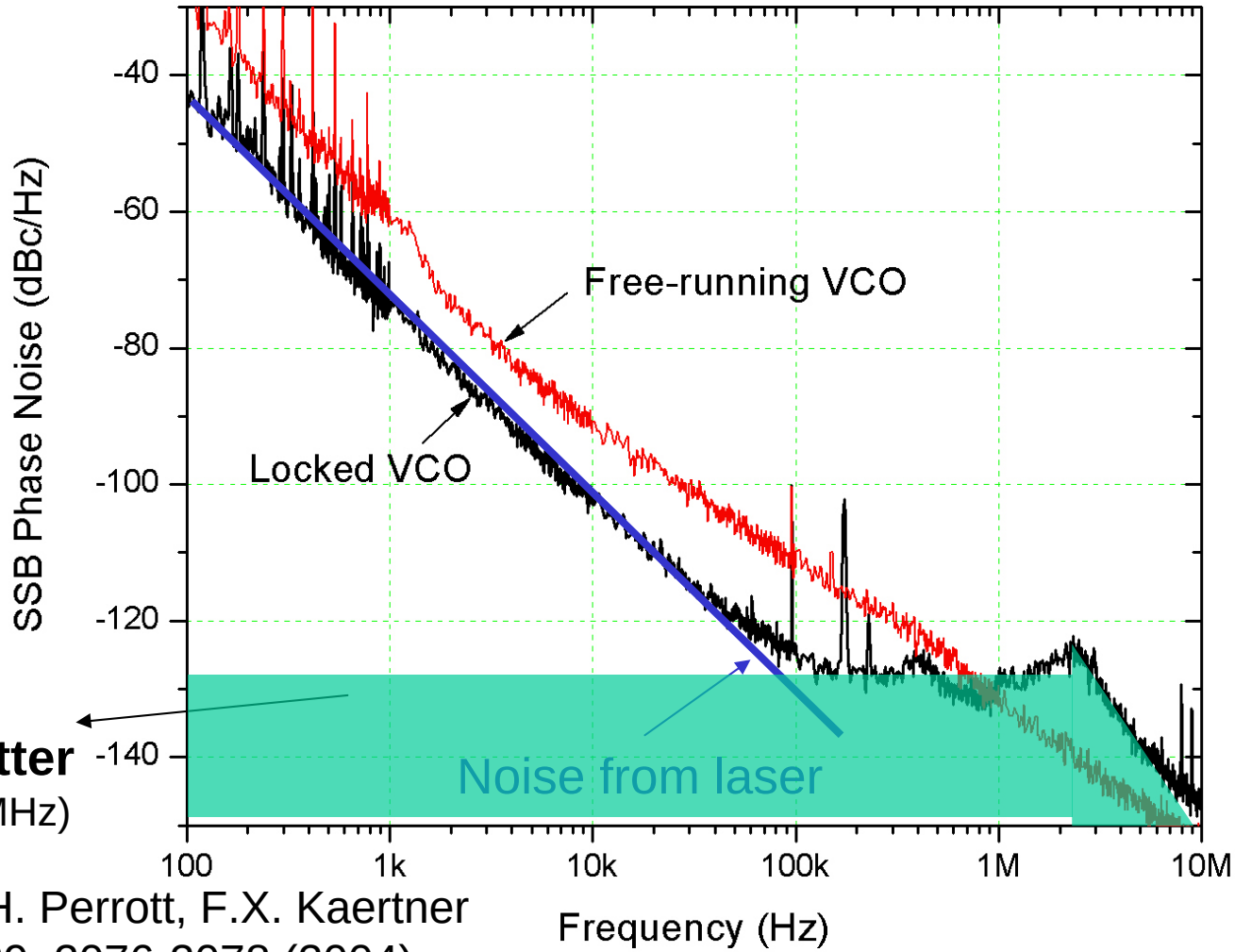
Limitation in Achieving Low Absolute Jitter

- **Noise of laser noise dominates at low frequencies**



Estimate of Relative Noise Between VCO and Laser

- **A separate experiment led to the estimate below**



<60 fs
Timing jitter
(100Hz-10MHz)

J. Kim, M.H. Perrott, F.X. Kaertner
Opt. Lett. 29, 2076-2078 (2004)

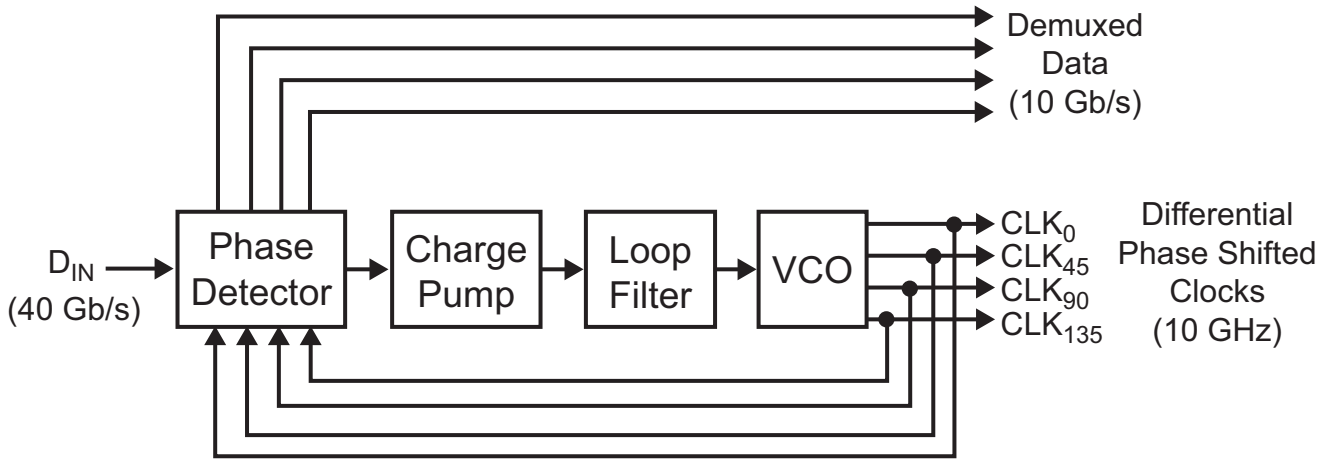
Conclusions

- **Optical components have the following benefits for phase-locked loops:**
  - **Mode-locked lasers provide extremely low jitter pulse sequences**
  - **Optical channels provide extremely high bandwidth**
  - **Optical components allow extremely fast memoryless processing of signals (such as multiplication)**
- **We demonstrated a low jitter phase-locked loop leveraging optical pulses as input and optical/electronic phase detection**

Many more exciting opportunities will arise as we obtain higher integration levels for optical components

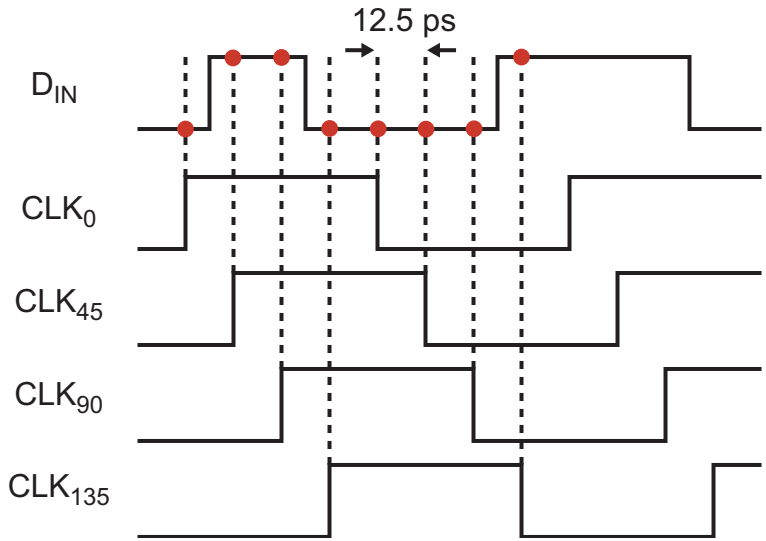
High Speed Clock and Data Recovery Circuit Techniques

A 40 Gb/s CDR in 0.18u CMOS! (Lee and Razavi)



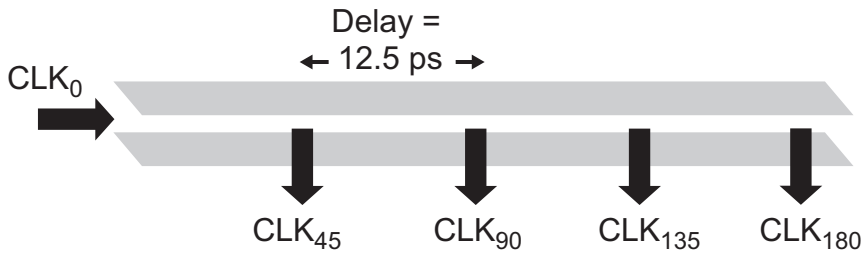
- **Achieves high speed operation using interleaving**
  - **4 parallel 10 Gb/s detectors are fed by an 8-phase VCO**
    - 4 phases used for sampling registers
    - 4 phases used for bang-bang phase detection registers
- **Key challenges**
  - **Low jitter and low mismatch between clock phases**
    - We will look at this issue in detail here
  - **Achievement of 10 Gb/s sampling/bang-bang detection**

The Need for Low Mismatch Between Clock Phases



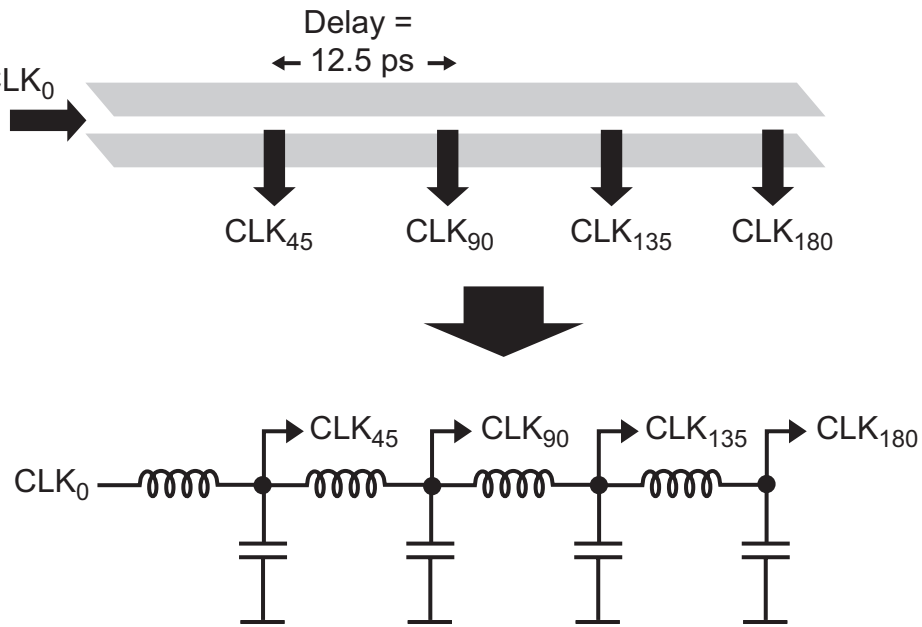
- 8-phases generated by 4 VCO clock signals and their complements
- Desired spacing between clock signals is only 12.5 ps!
  - Must meet setup and hold times of each 10 Gb/s sampler and phase detector register (limited by 0.18u technology)
  - Mismatch and jitter on clock phases quickly eats into any margin left over after meeting setup/hold times
    - Unacceptable bit error rates can easily result

A Method to Generate Clock Phases



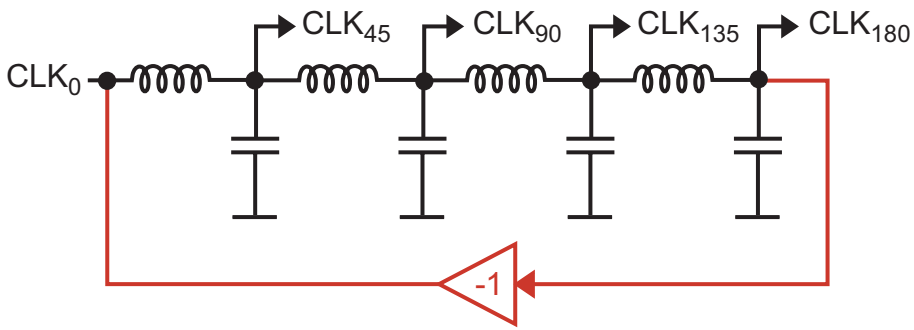
- Use transmission delay lines to generate each phase
- Advantage over using buffers as delay elements
  - Wide bandwidth and lower noise
  - Mismatch only a function of geometry variation
    - Buffer mismatch a function of both geometry and device variation (i.e., doping variation, etc.)
- Issue: transmission line is big
  - Loss (and finite bandwidth) due to finite resistance of metal
  - Long distance between clock phase outputs undesirable

Realize a Lumped Parameter Version of Trans. Line



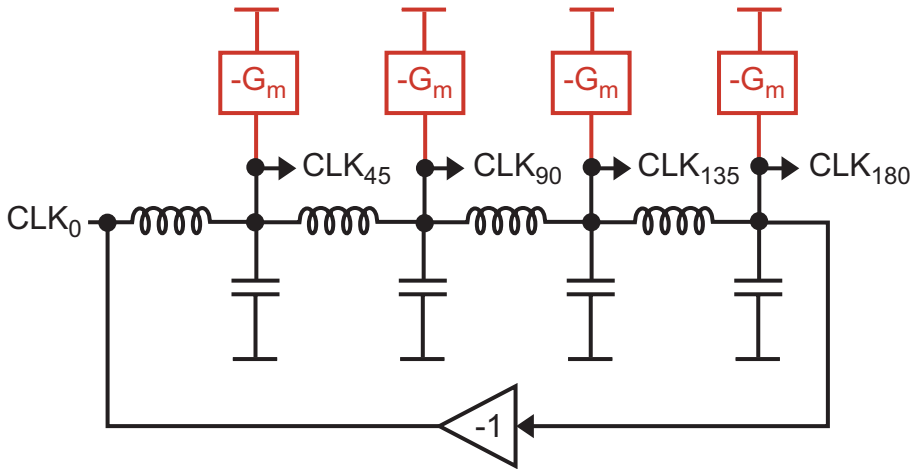
- Approximate transmission line as an LC ladder network
  - Allows a much more compact implementation
  - Offers the same advantage of having mismatch depend only on geometry
- Issue: now that mismatch has been dealt with, how do we achieve low jitter?

Combine VCO and Phase Generator



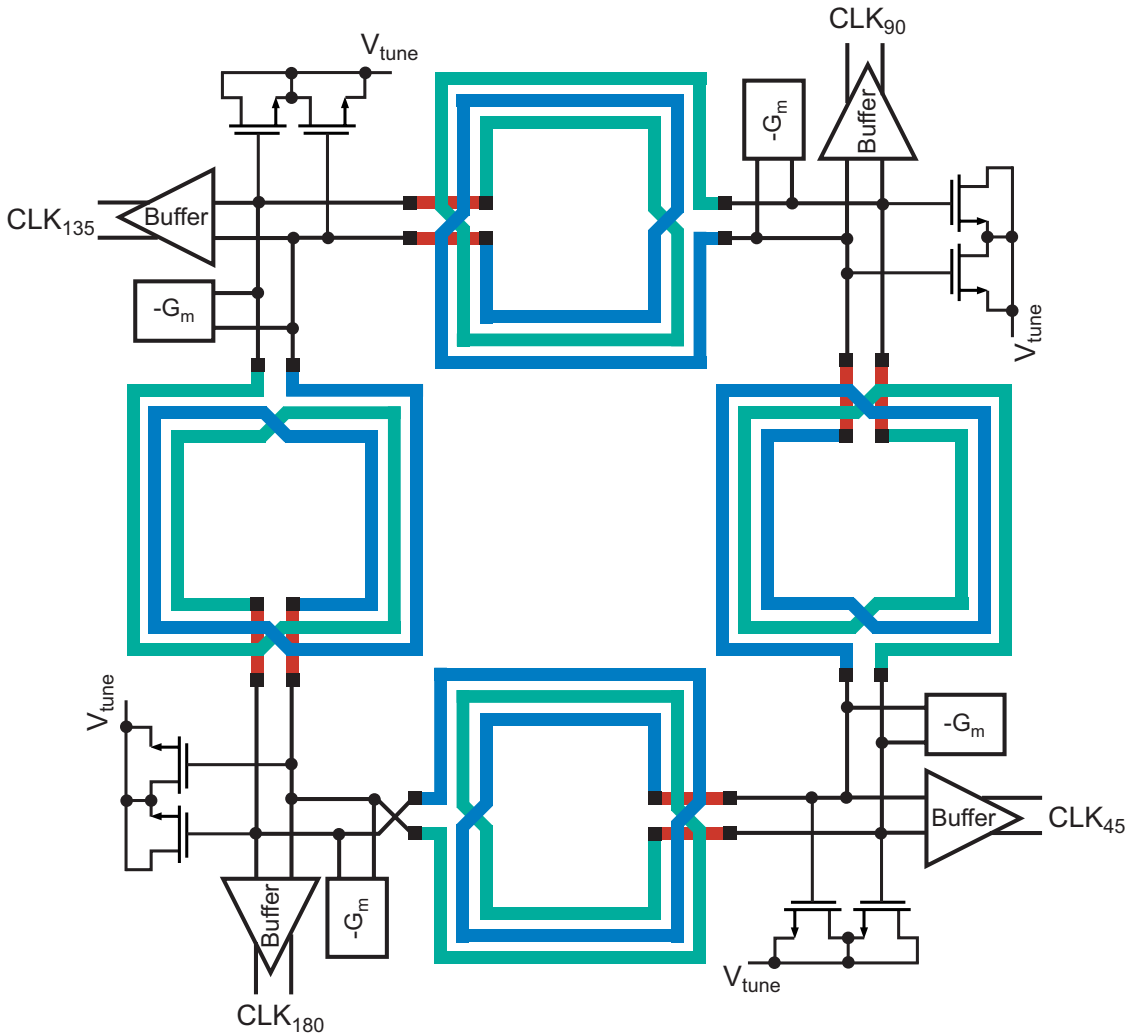
- Can satisfy Barkhausen criterion by inverting output of line and feeding back to the input
  - Looks a bit like a ring oscillator, but much better phase noise performance

Sustain Oscillation by Including Negative Resistance



- Place negative resistance at each phase to keep amplitudes identical
  - Must be careful to minimize impact on mismatch
- Issue: how do you match feedback path from CLK_{180} to CLK_0 with other phases?

Use a Circular Geometry!



- Note use of differential inductors, etc.

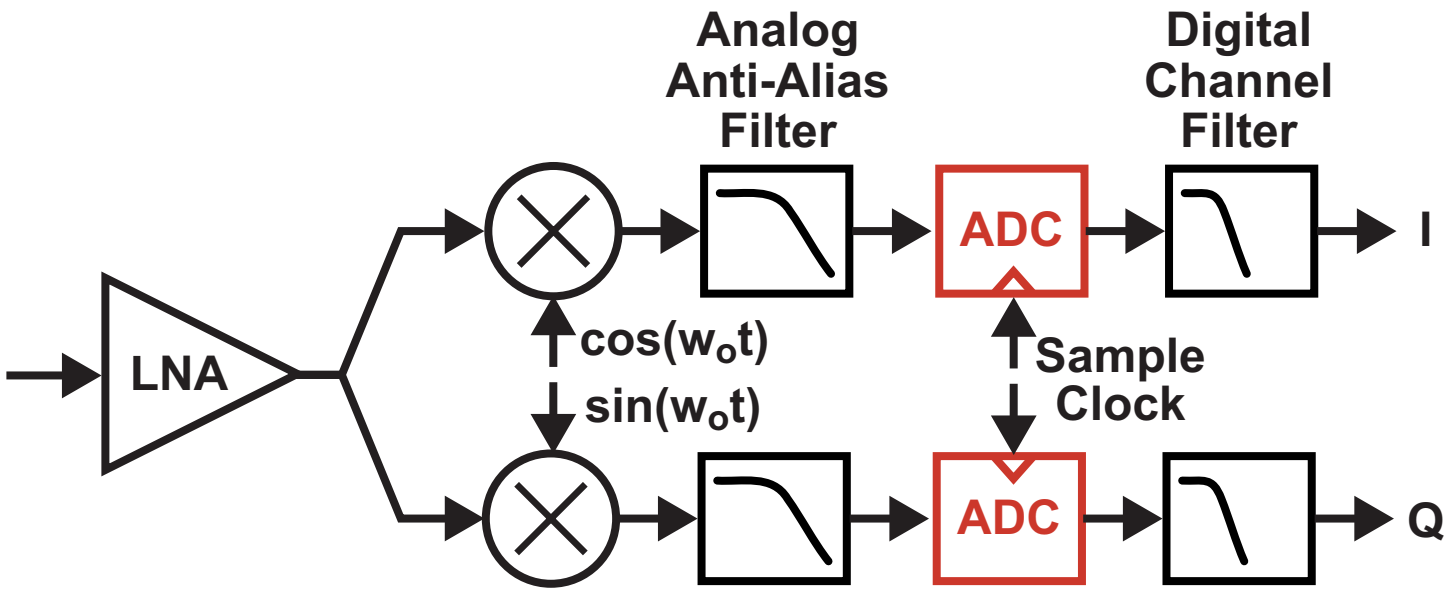
Other Nice Nuggets in the Lee and Razavi Paper

- **Phase detection using 4 bang-bang detectors**
  - **Clever combining of individual detectors to create an overall control voltage**
  - **Note: Bang-bang detection linearized by metastable behavior of registers**
- **Achievement of 10 Gb/s registers in 0.18u CMOS**
  - **Leverages a large amplitude clock signal using a tuned VCO buffer**
  - **Uses SCL registers with resistor loads – bottom current sources eliminated to leverage large amplitude clock**
- **Fast XOR gate and amplifier structures**

Take a look at the paper for more details:
"A 40-Gb/s Clock and Data Recovery Circuit in 0.18-um CMOS Technology", Jri Lee and Behzad Razavi, JSSC, Dec. 2003

Leveraging VCO-based Quantization to Achieve Low Power, Wideband A/D Conversion for Multi-Standard RF Front-ends

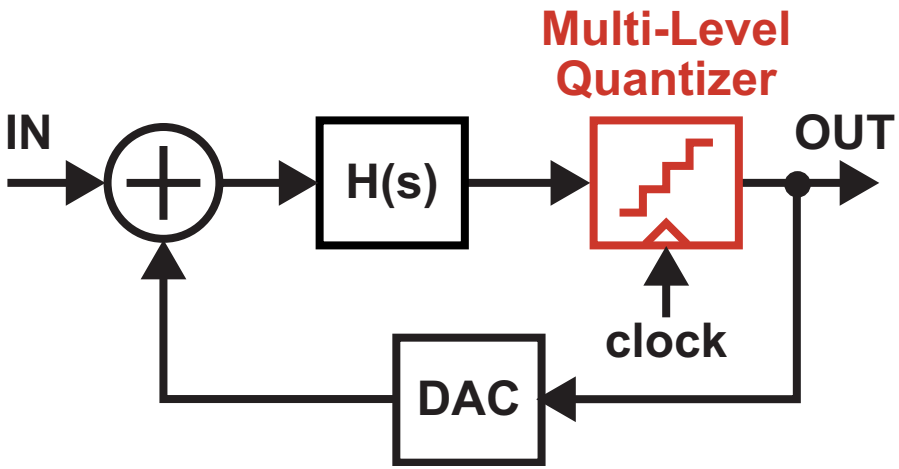
Motivation



- A highly digital receive path is very attractive for achieving multi-standard functionality
- A key issue is achieving a wide bandwidth ADC with high resolution and low power
  - Minimal anti-alias requirements are desirable for simplicity

Continuous-Time Sigma-Delta ADC structures have very attractive characteristics for this space

A Basic Continuous-Time Sigma-Delta ADC Structure



- **Key characteristics**
  - **Operation based on oversampling and feedback**
  - **Sampling occurs at the quantizer *after* filtering by *H(s)***
  - **Quantizer noise is shaped according to choice of *H(s)***
    - High open loop gain required to achieve high SNR
    - Digital filtering/decimation required for signal extraction

We will focus on achieving an efficient implementation of the multi-level quantizer by using a ring oscillator

Why are VCO-based converters interesting?

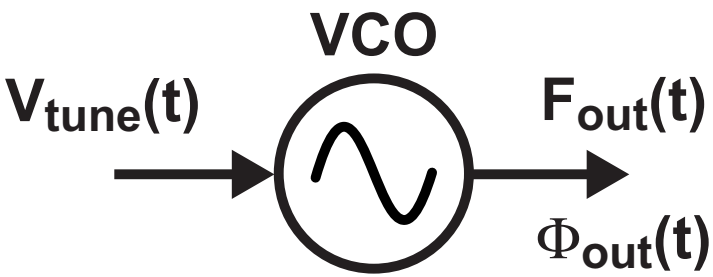
- **Converters are building blocks for mixed-signal systems**
  - **Communication systems (both wireless and wireline)**
  - **Frequency synthesizers**
- **Standard implementations are problematic**
  - **High-performance analog functionality is becoming more difficult to achieve using traditional methods**
  - **Shrinking power supply, limited intrinsic gain, etc.**
- **Voltage controlled oscillators are inherently mixed-signal**
  - **Analog input voltage**
  - **Binary (digital) output levels**
  - **Highly digital implementation**

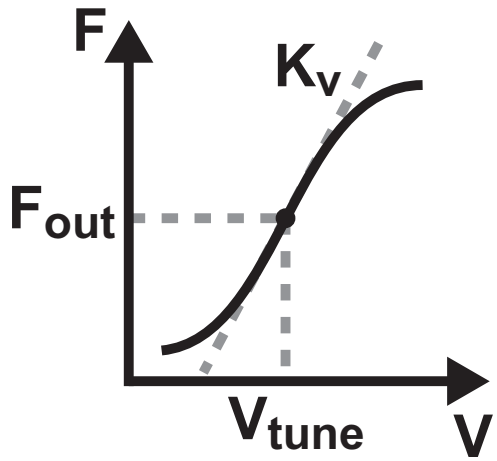
Can voltage controlled oscillators offer excellent analog performance with a highly digital implementation?

A 10-bit 20MHz 38mW 950MHz CT ΣΔ ADC with a 5-bit noise-shaping VCO-based Quantizer and DEM circuit in 0.13u CMOS

Matthew Z. Straayer, Michael H Perrott

Voltage Controlled Oscillator (VCO) fundamentals





$$F_{out}(t) = K_V \cdot V_{tune}(t)$$

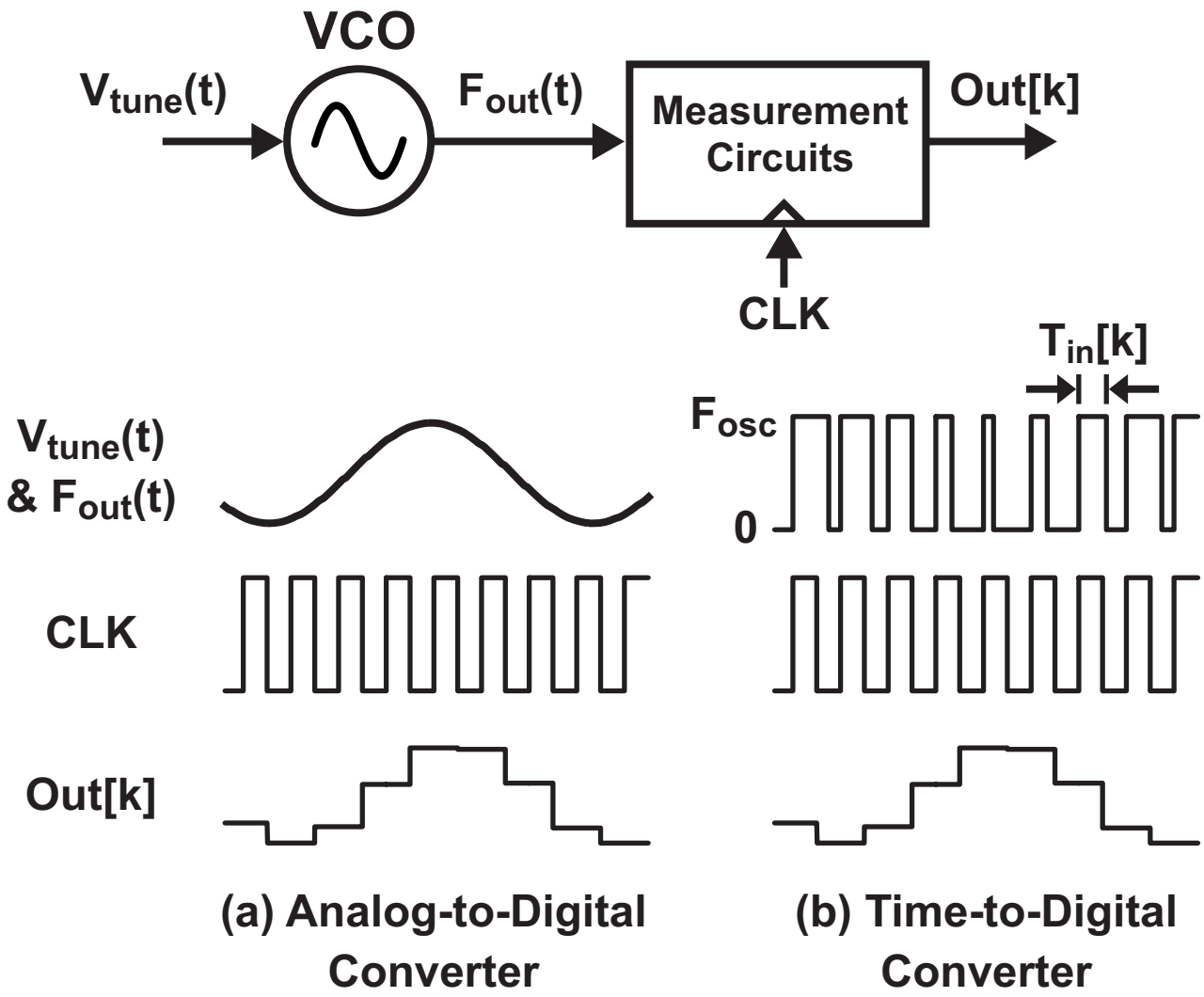
$$\Phi_{out}(t) = \int_0^t 2\pi \cdot K_V \cdot V_{tune}(\tau) \cdot d\tau$$

$$K_V = \frac{dF_{out}}{dV_{tune}}$$

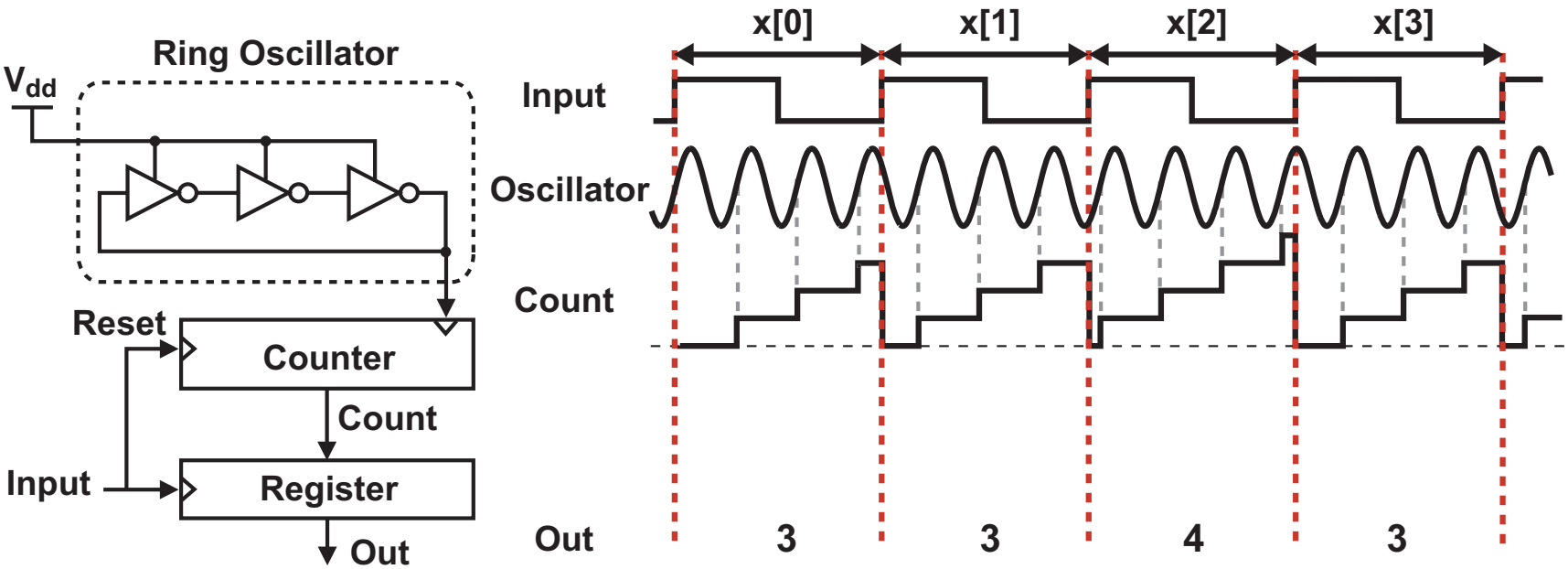
- Voltage-to-frequency is a linear relationship
- Voltage-to-phase is an integration

Can we leverage these analog signal processing functions?

Concept of VCO-based converters

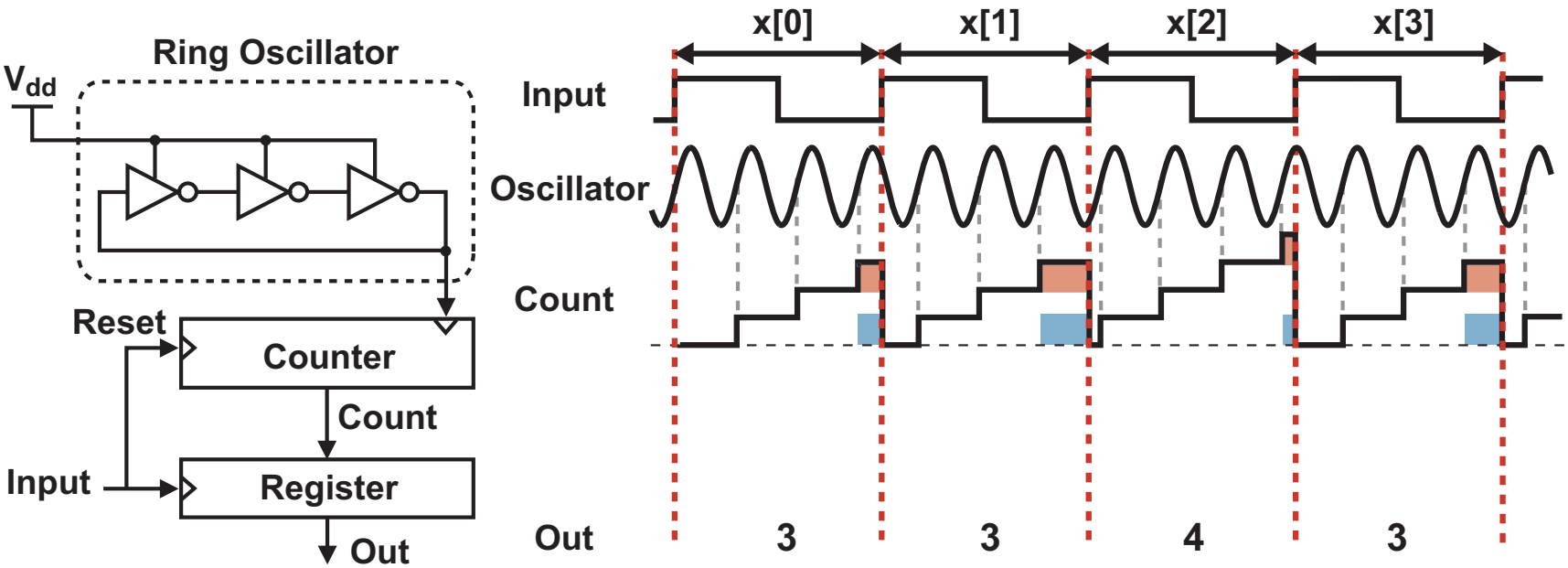


Consider Measurement of the Period of a Signal



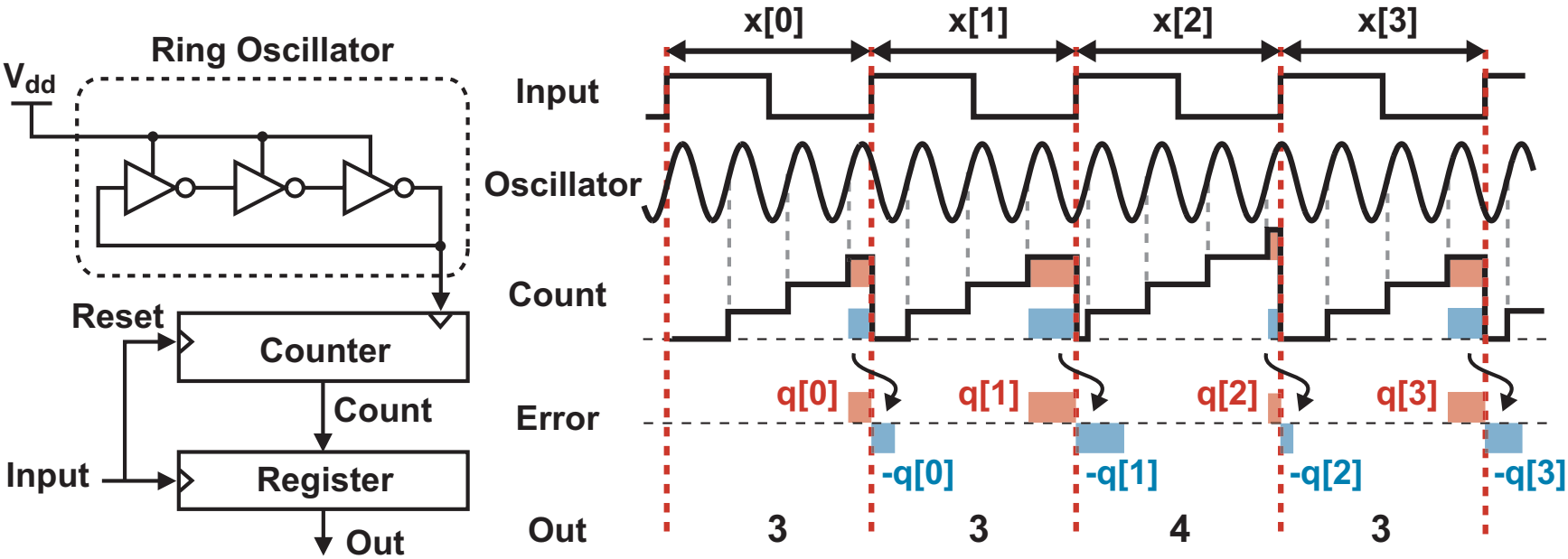
- Use digital logic to count number of oscillator cycles during each input period
  - Assume that oscillator period is much smaller than that of the input
- Note: output count per period is not consistent
  - Depends on starting phase of oscillator within a given measurement period

Examine Quantization Error in Measurements



- Quantization error varies according to starting phase of the oscillator within a given measurement period
  - Leads to *scrambling* of the quantization noise
- But there is something rather special about the scrambling action …

A Closer Examination of Quantization Noise



- **Calculate impact of quantization noise in time:**

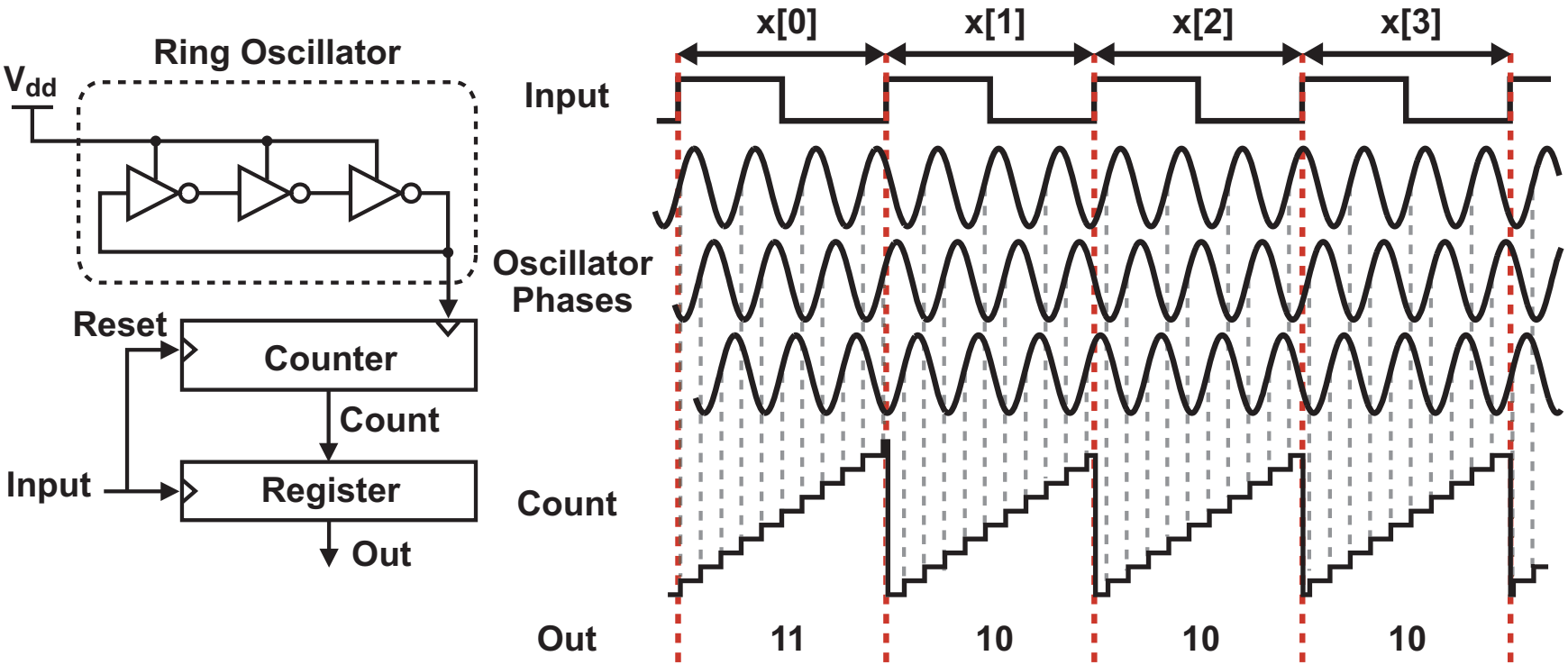
$$\begin{aligned} out[k] &= x[k] + error[k] \\ &= x[k] + q[k] - q[k-1] \end{aligned}$$

- **Take Z-transform:**

$$Out(z) = X(z) + (1 - z^{-1})Q(z)$$

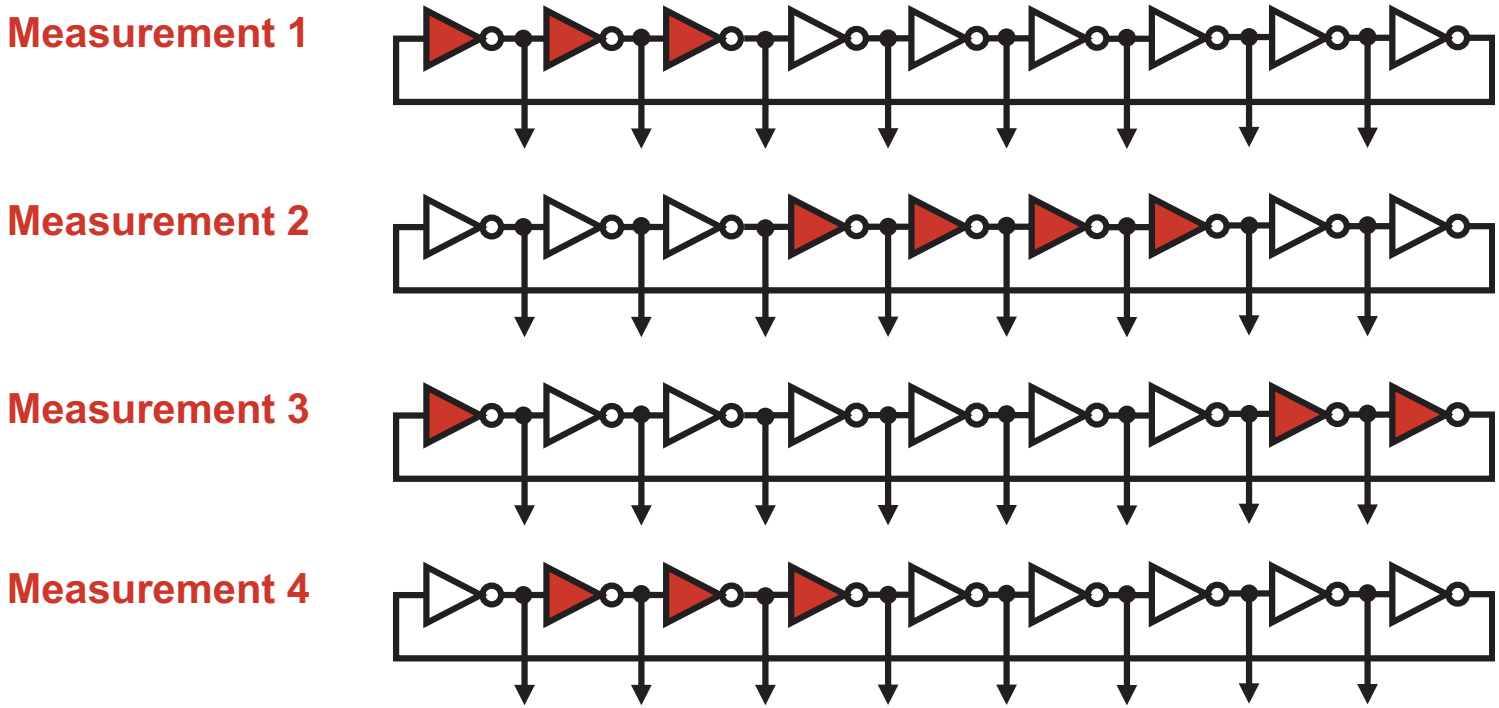
Quantization noise is first order noise shaped!

Improve Resolution By Using All Oscillator Phases



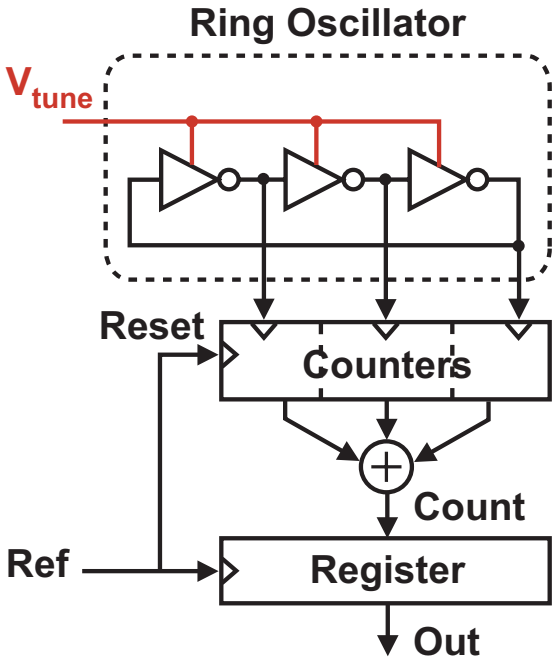
- Step size in time is reduced to one inverter delay
  - Quantization noise is still scrambled and first order noise shaped
  - Mismatch between delay elements is *barrel-shifted*

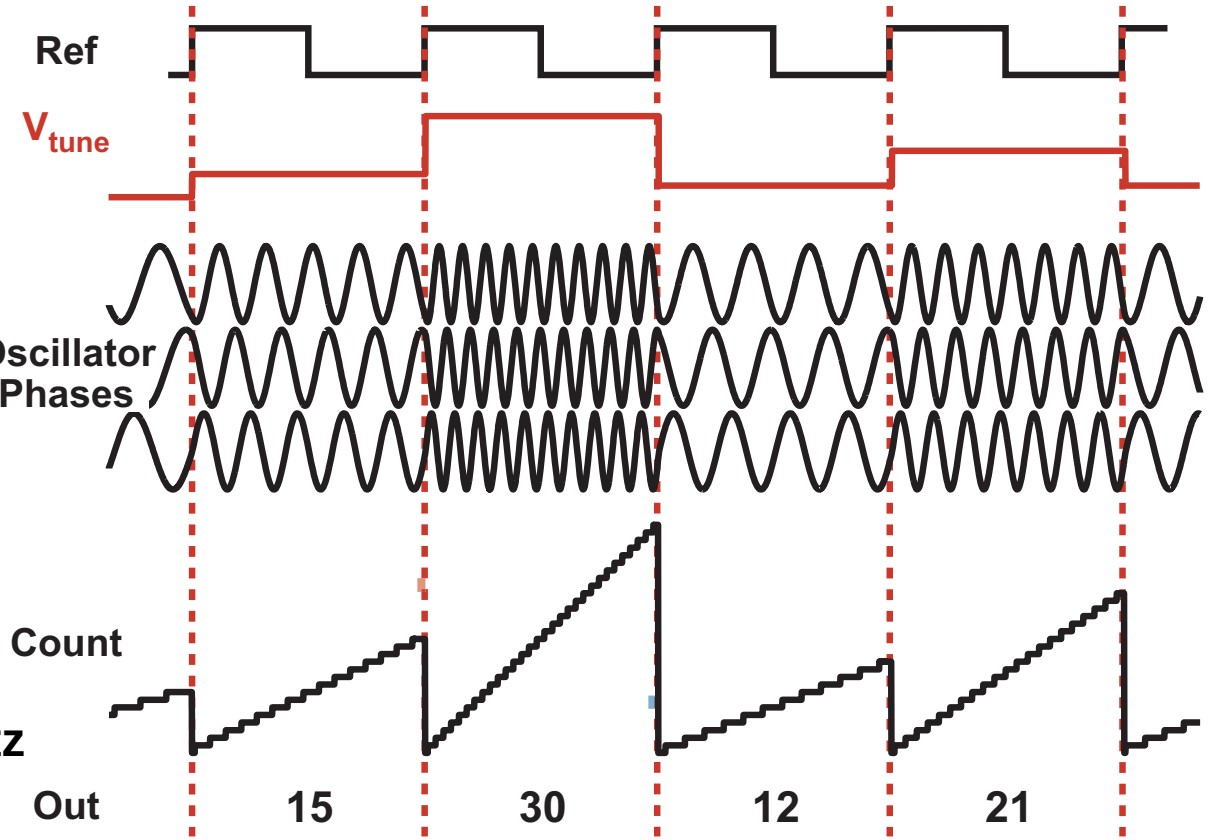
A Closer Look at Barrel Shifting Property



- Barrel shifting is seen as steady progression through delay elements across measurements
  - Mismatch between delay elements is first order shaped!

Application of Ring Oscillator as an ADC Quantizer



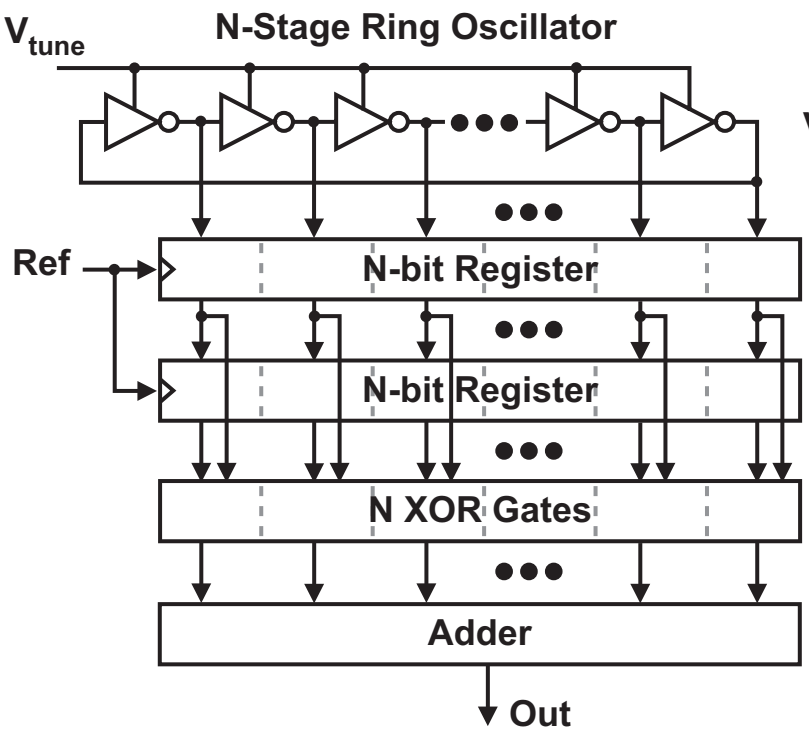


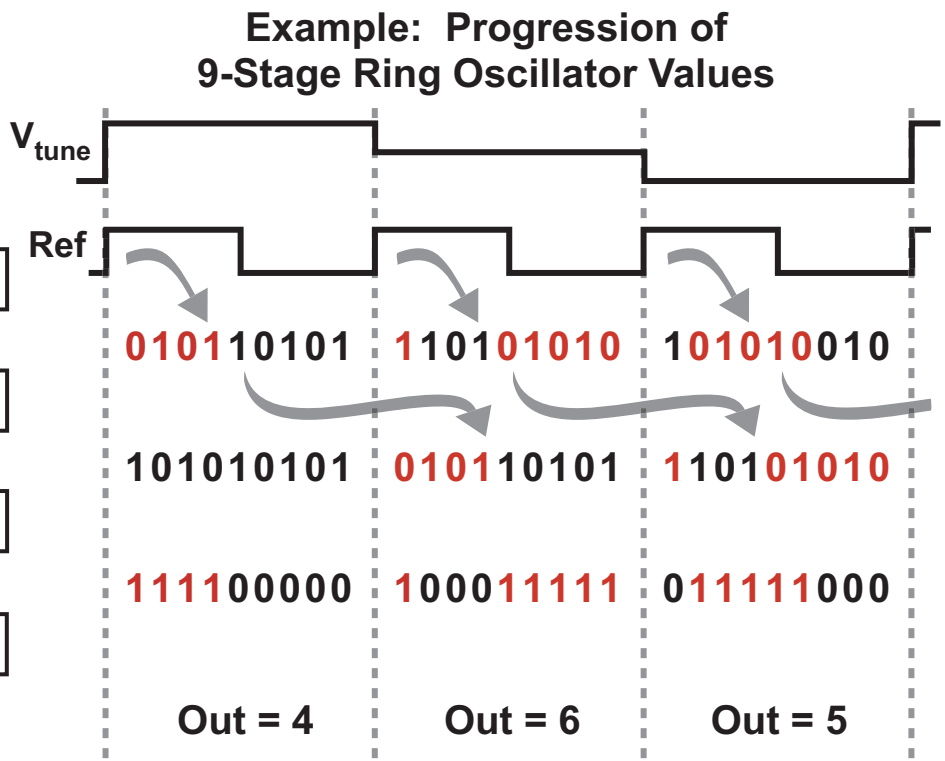
Similar approaches:
Alon, Stojanovic, Horowitz JSSC 2005
Kim, Cho, ISCAS 2006

- **Input: analog tuning of ring oscillator frequency**
- **Output: count of oscillator cycles per Ref clock period**

Quantization noise is first order noise shaped!

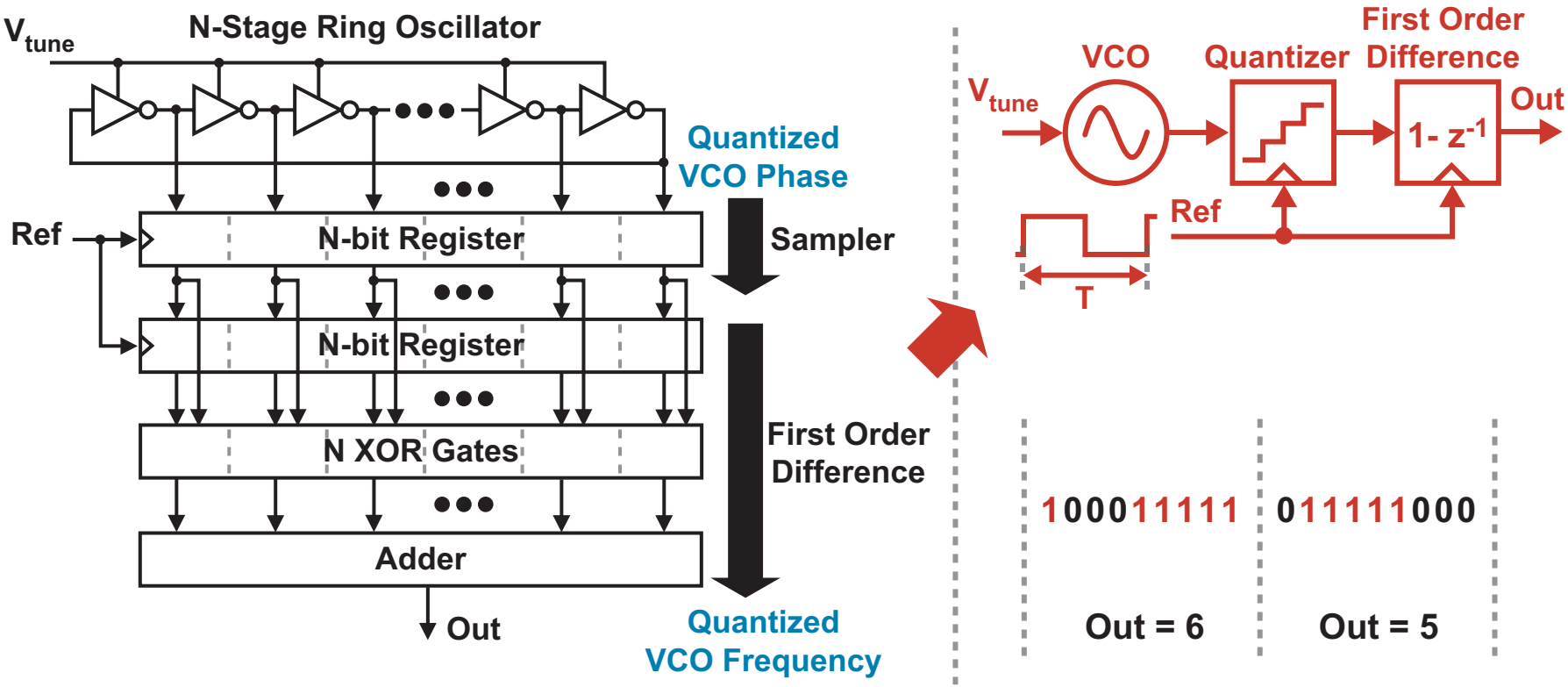
A Better Implementation for High Speed Conversion





- Assume a high Ref clock frequency (i.e., 1 GHz)
- Increase number of stages, *N,* such that transitions never cycle through any stage more than once per Ref clock period
- Use registers and XOR gates to determine transition count
  - Avoidance of reset action improves operating speed

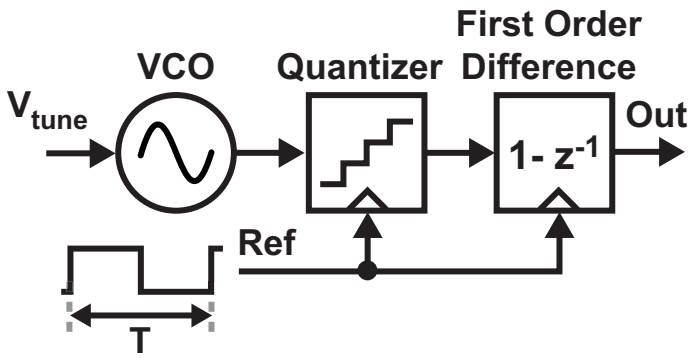
A First Step Toward Modeling



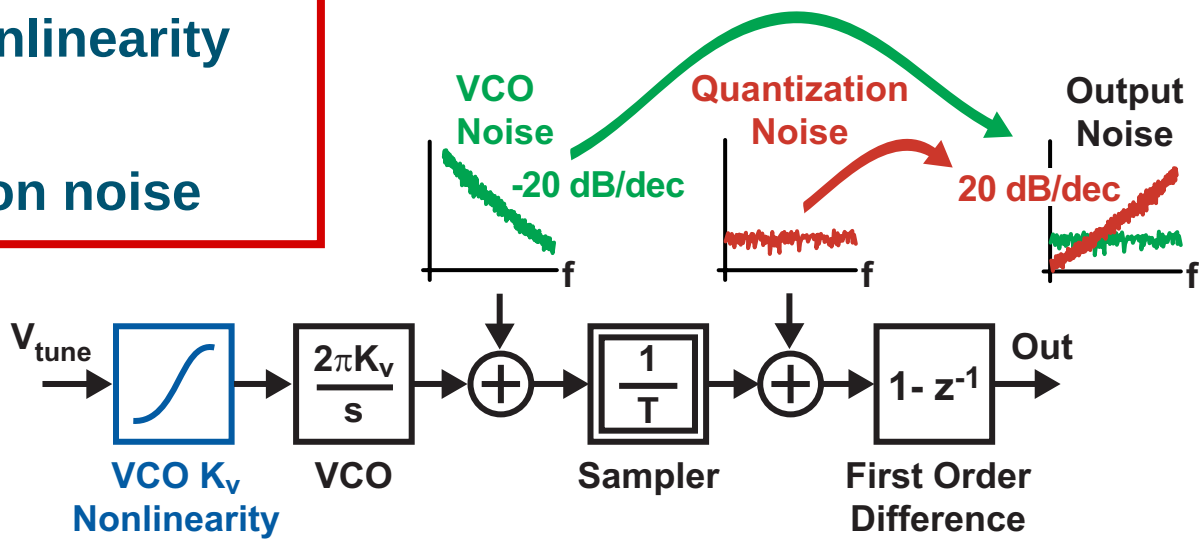
- VCO provides quantization, register provides sampling
  - Model as separate blocks for convenience
- Addition of XOR operation on current and previous samples corresponds to a first order difference operation
  - Extracts VCO frequency from the sampled VCO phase signal

Corresponding Frequency Domain Model

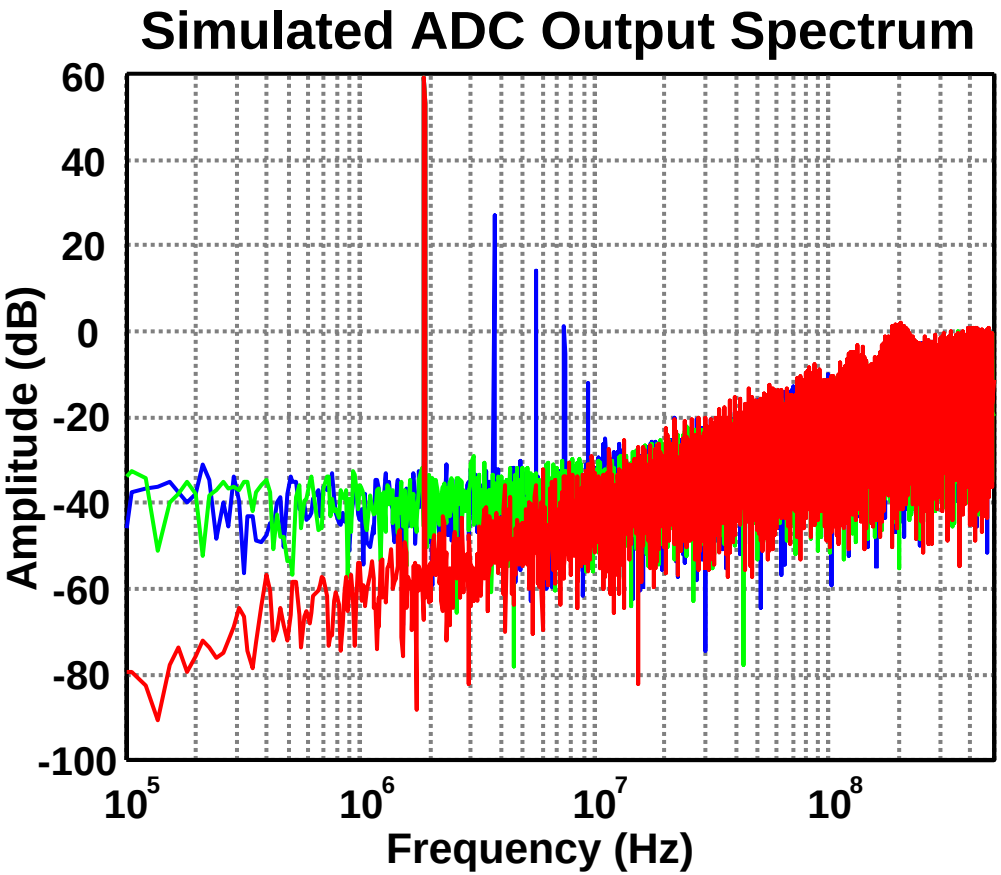
- VCO modeled as integrator and K_v nonlinearity
- Sampling of VCO phase modeled as scale factor of 1/T
- Quantizer modeled as addition of quantization noise



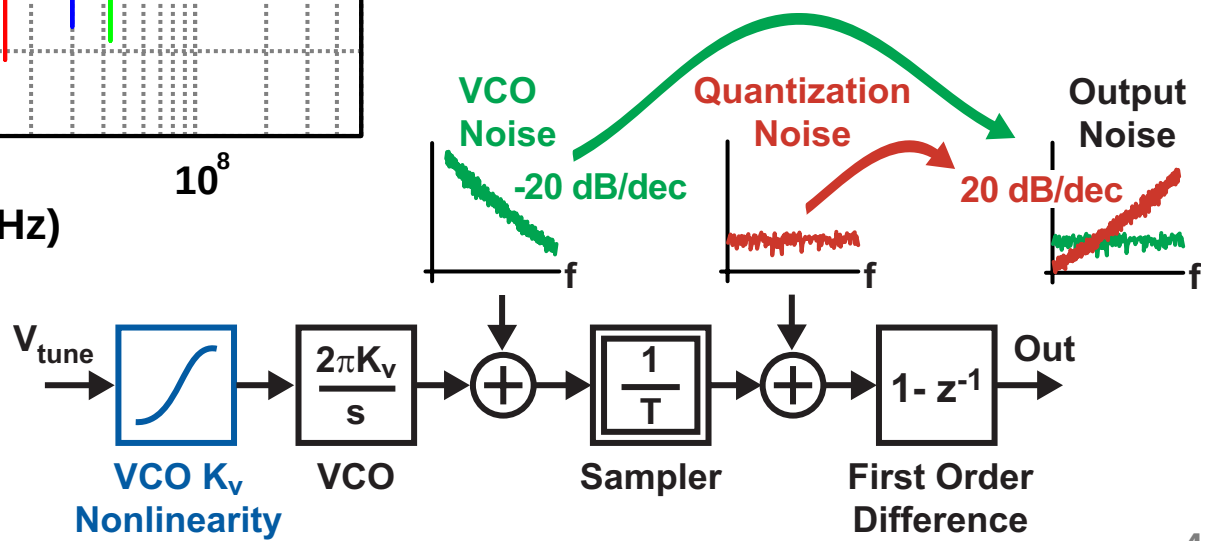
- Key non-idealities:
  - VCO K_v nonlinearity
  - VCO noise
  - Quantization noise



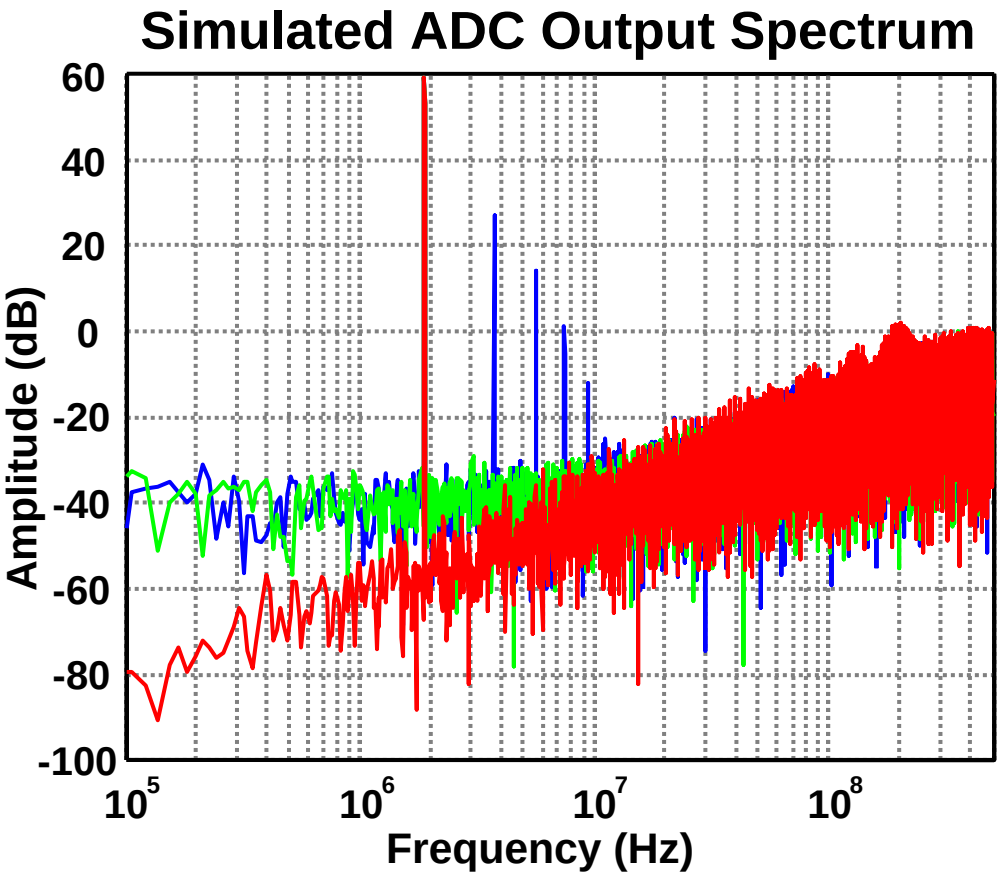
Example Design Point for Illustration



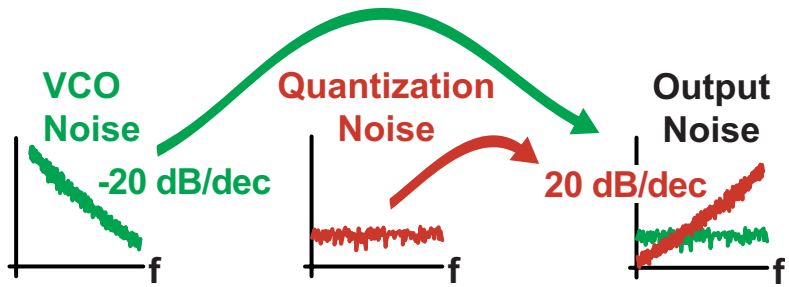
- Ref clk: 1/T = 1 GHz
- 31 stage ring oscillator
  - Nominal delay per stage: 65 ps
- K_{VCO} = 500 MHz/V
  - ±5% linearity
- VCO noise: -100 dBc/Hz at 10 MHz offset



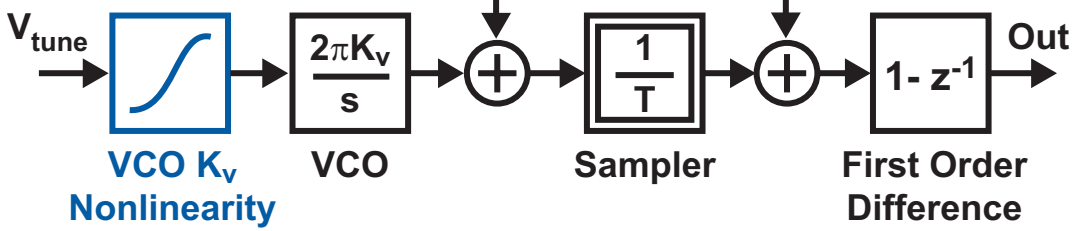
SNR/SNDR Calculations with 20 MHz Bandwidth



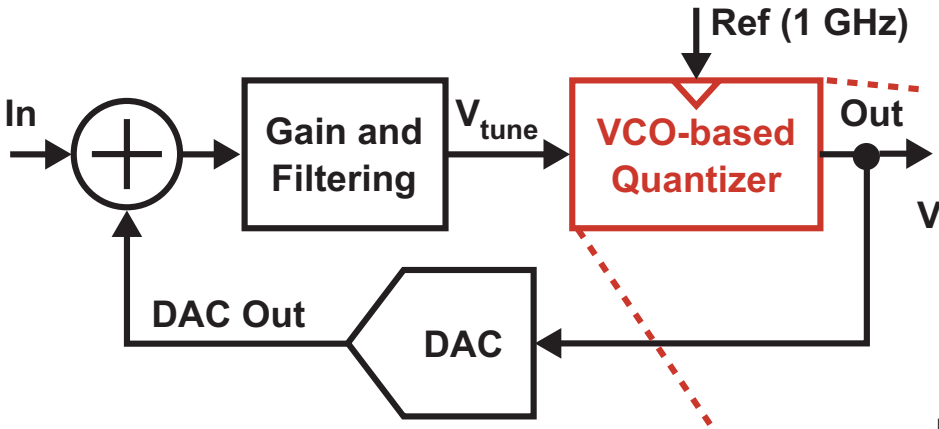
Conditions	SNDR
Ideal	68.2 dB
VCO Thermal Noise	65.4 dB
VCO Thermal + Nonlinearity	32.2 dB



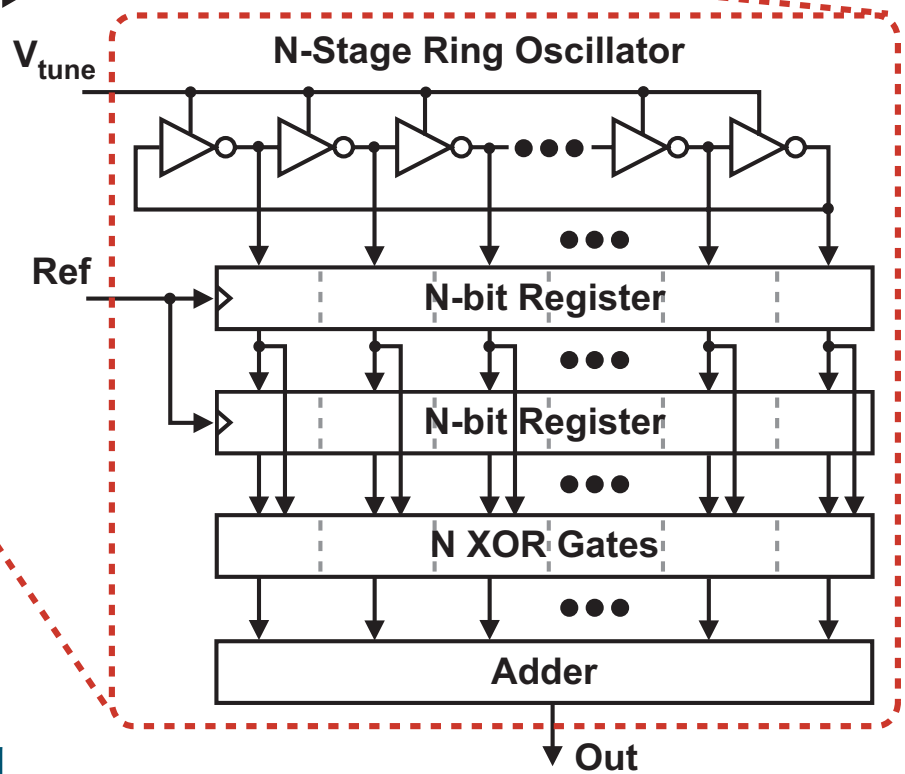
VCO K_v nonlinearity is the key performance bottleneck



Reducing the Impact of Nonlinearity using Feedback

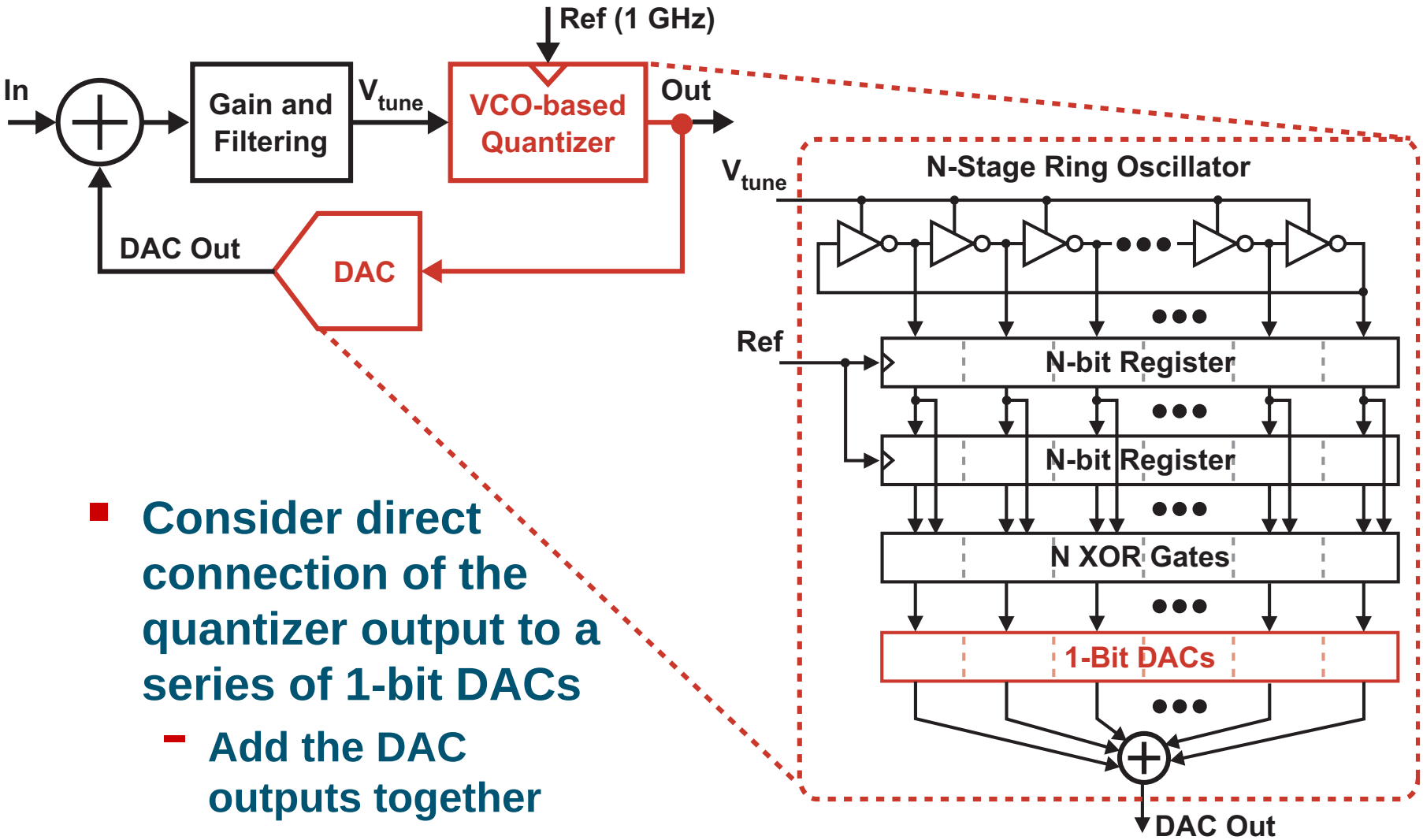


Iwata, Sakimura, TCAS II, 1999
Naiknaware, Tang, Fiez, TCAS II, 2000



- Place VCO-based quantizer within a continuous-time Sigma-Delta ADC structure
  - Quantizer nonlinearity suppressed by preceding gain stage
- Must achieve a highly linear DAC structure
  - Otherwise, noise folding and other bad things happen …

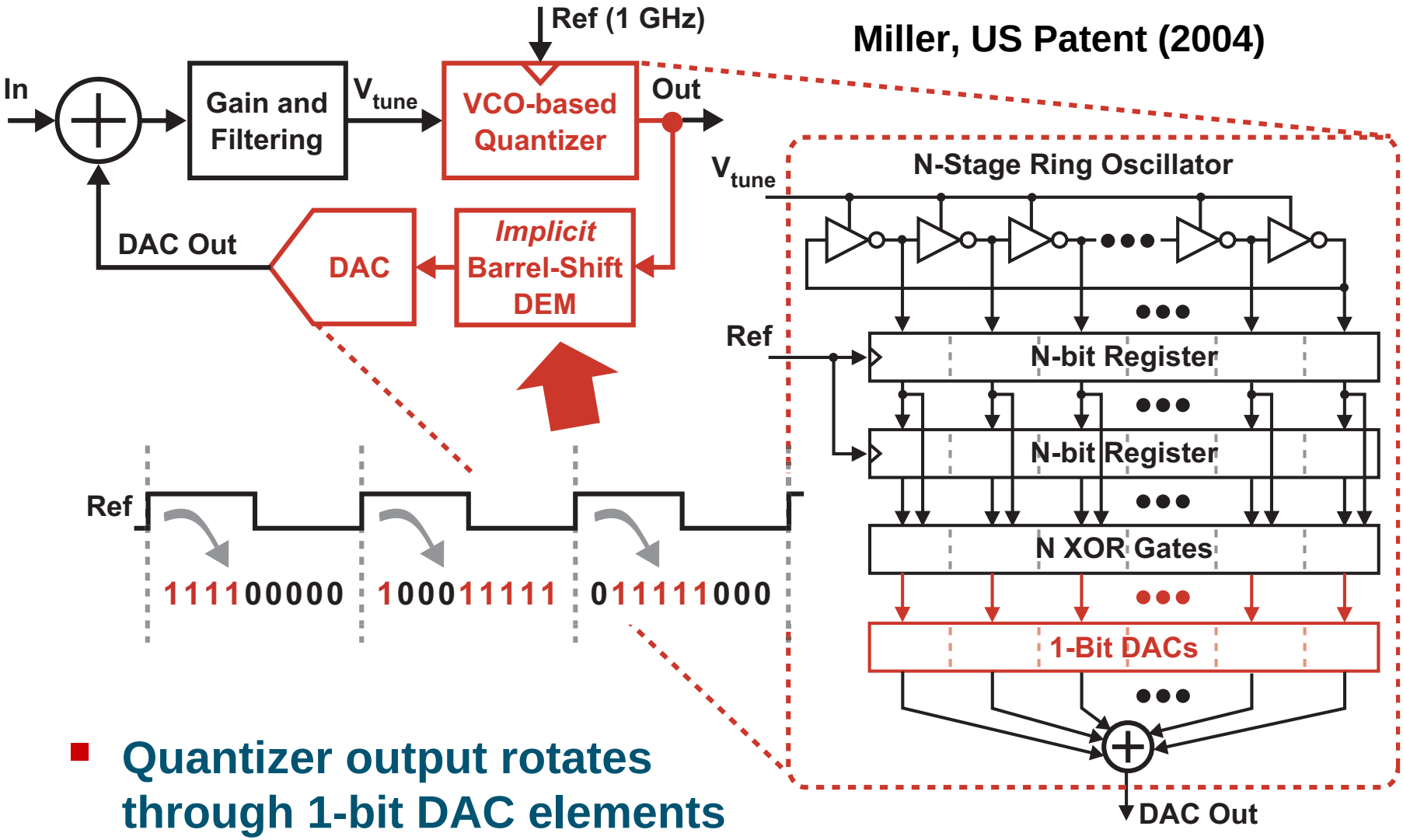
A Closer Look at the DAC Implementation



- Consider direct connection of the quantizer output to a series of 1-bit DACs
  - Add the DAC outputs together

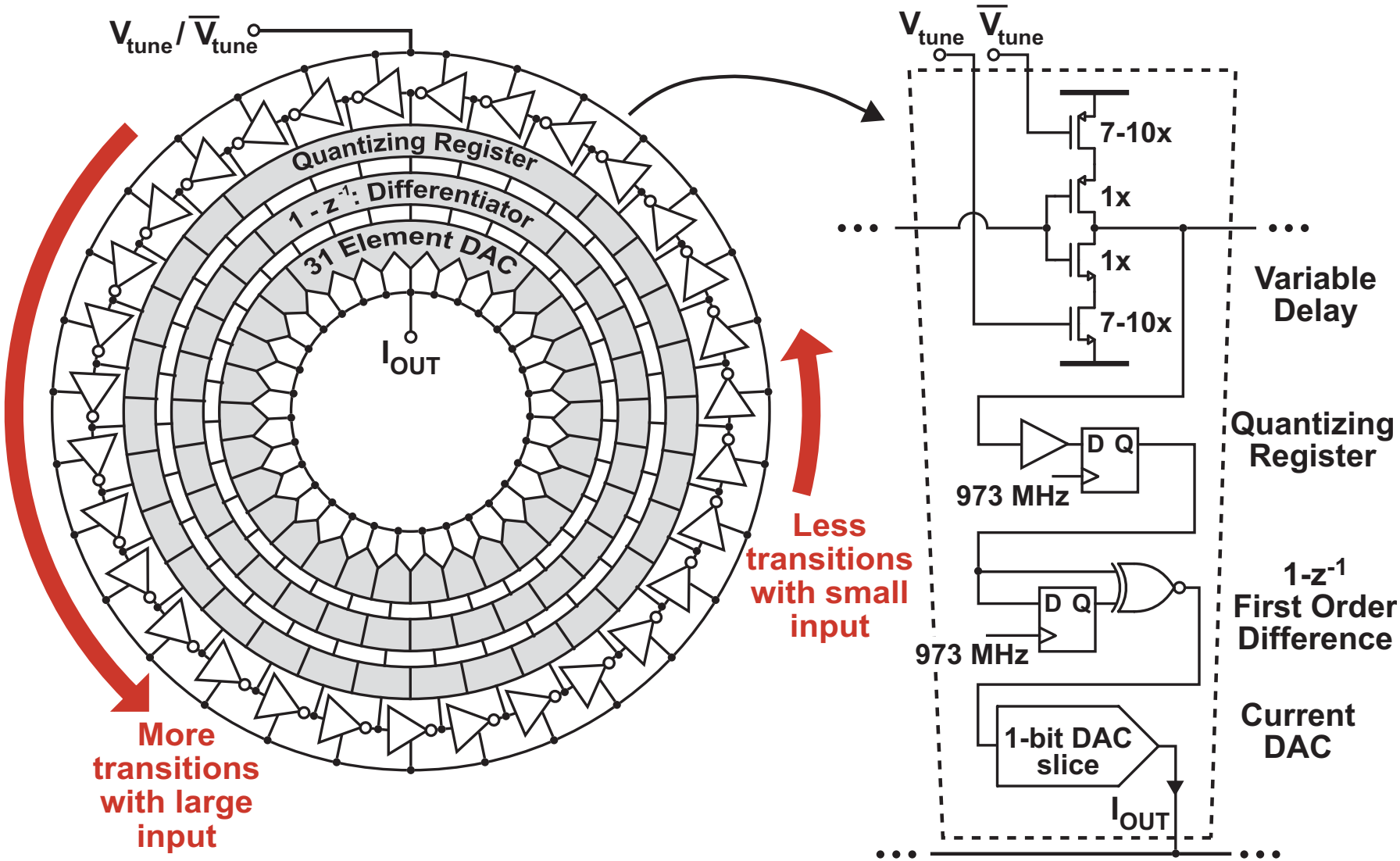
What is so special about doing this?

Key Insight: Quantizer Acts as a Barrel-Shifter

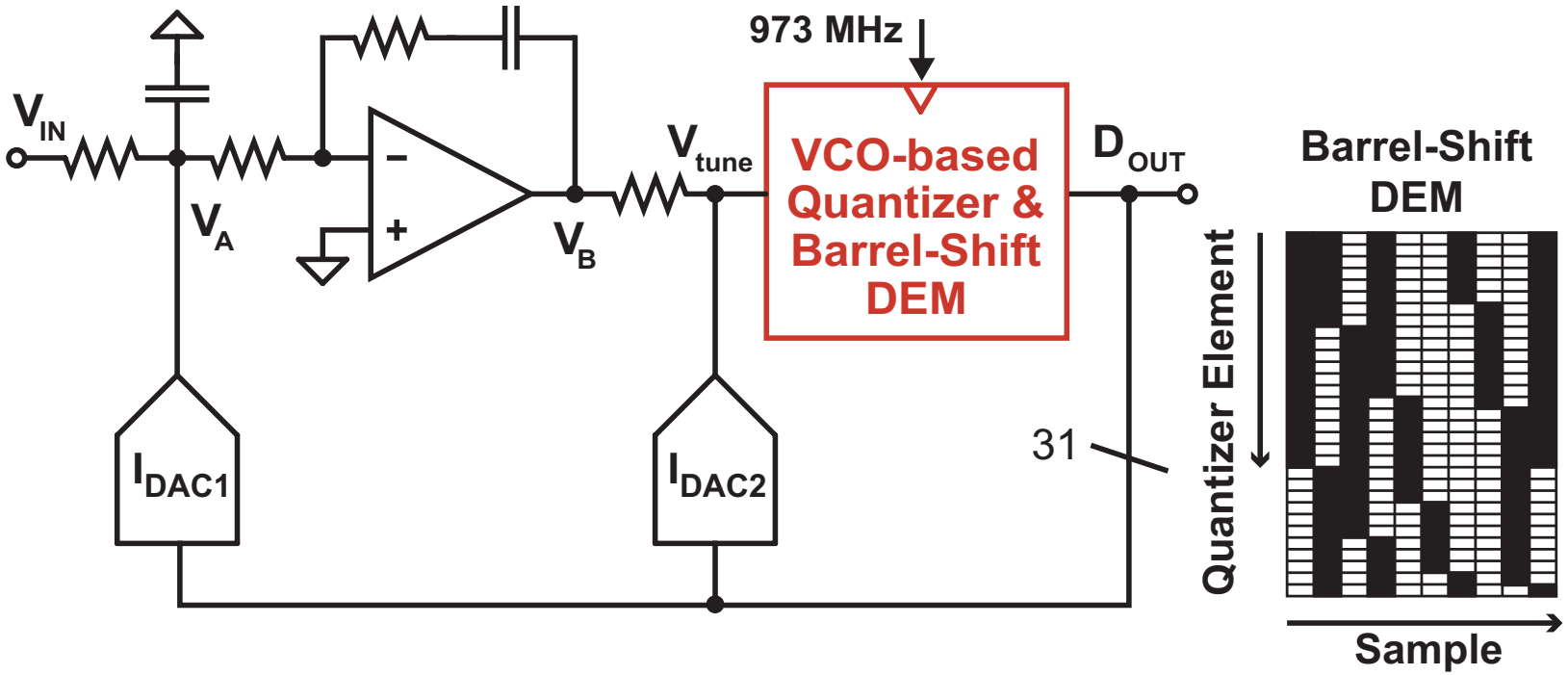


- Quantizer output rotates through 1-bit DAC elements
  - Acts to shape DAC mismatch and linearize its behavior

A Geometric View of the VCO Quantizer/DEM and DAC

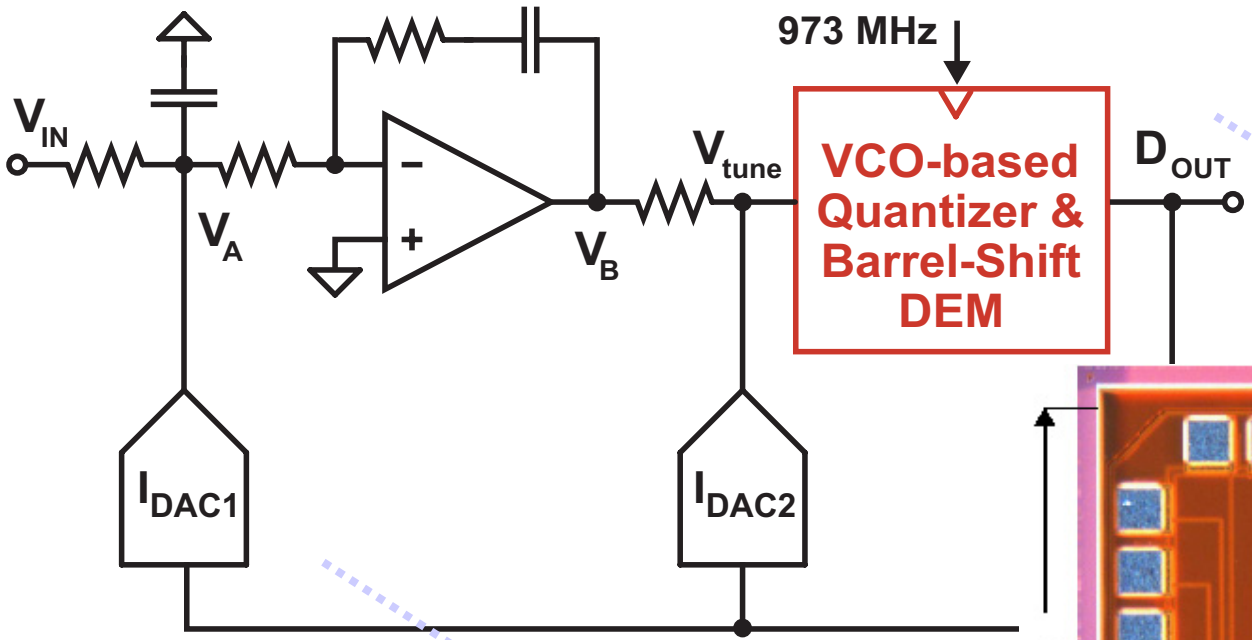


Our Prototype

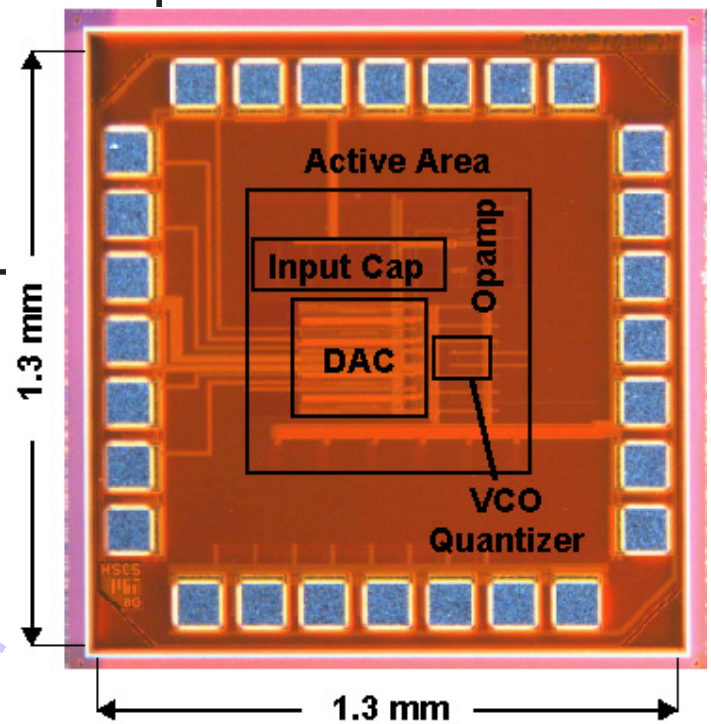


- Second order dynamics achieved with only *one* op-amp
  - Op-amp forms one integrator
  - I_{dac1} and passive network form the other (lossy) integrator
  - Minor loop feedback compensates delay through quantizer
- *Third order* noise shaping is achieved!
  - VCO-based quantizer adds an extra order of noise shaping

Custom IC Implementing the Prototype

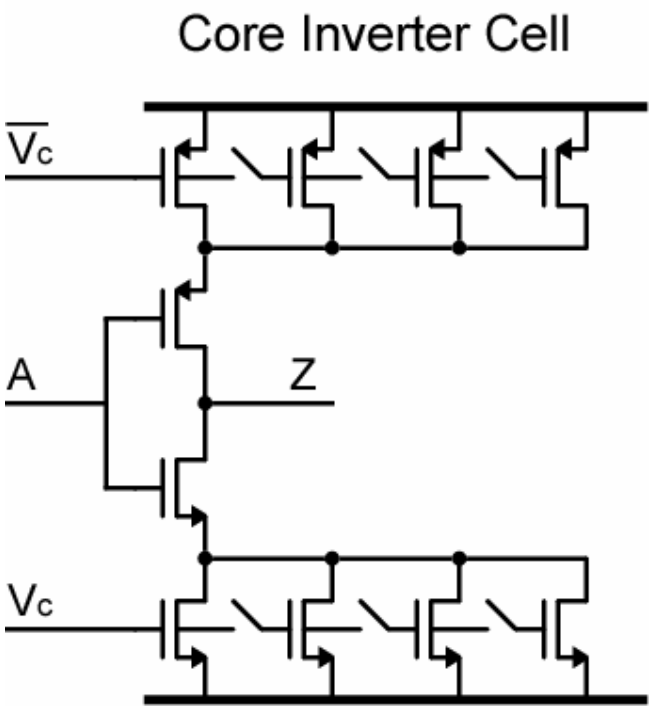


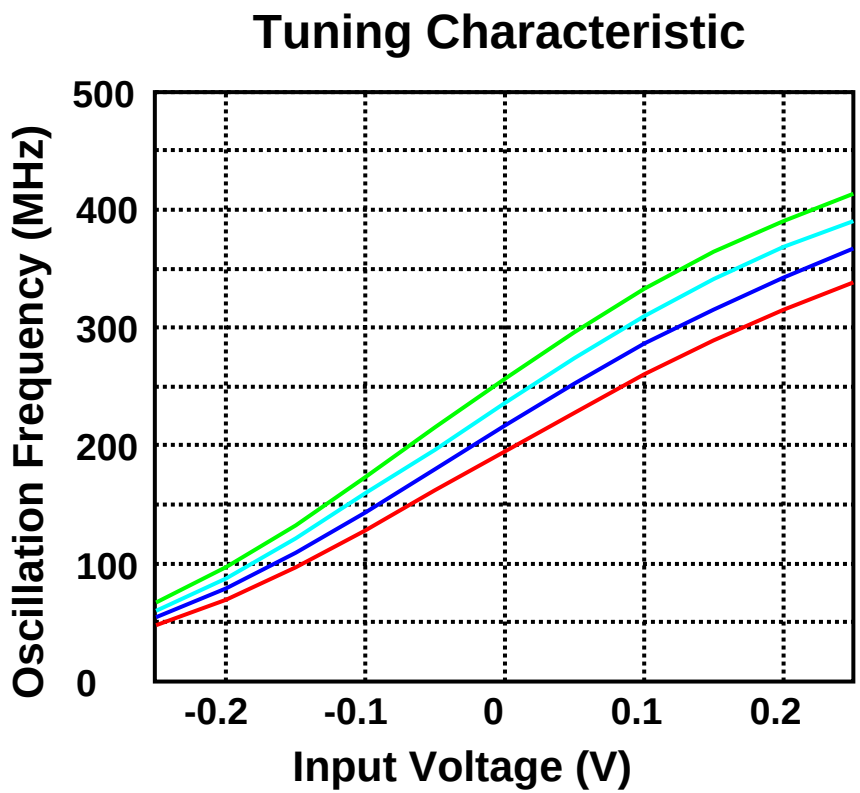
Straayer, Perrott
VLSI 2007



- 0.13u CMOS
- Power: 40 mW
- Active area: 700u X 700u
- Peak SNDR: 67 dB (20 MHz BW)
- Conversion efficiency: 0.5 pJ/conv. step

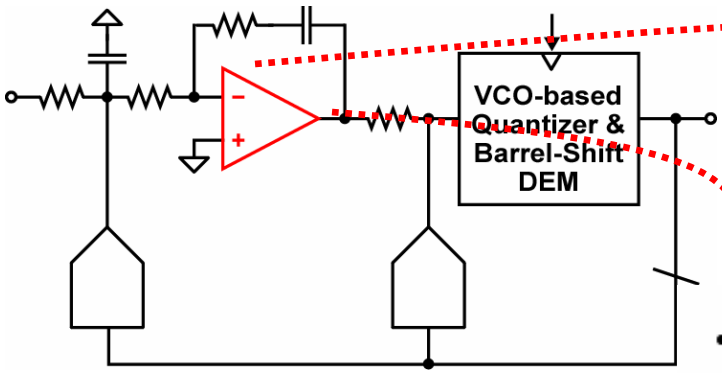
Design of the VCO Core Inverter Cell





- 31 stages
- Fast for good resolution (< 100 psec / stage)
- Large K_{VCO} (600-700 MHz) with good dynamic range
- 2 bits of coarse tuning for process variations
- < 8 mW for 1 GSPS 5-bit quantizer / DEM

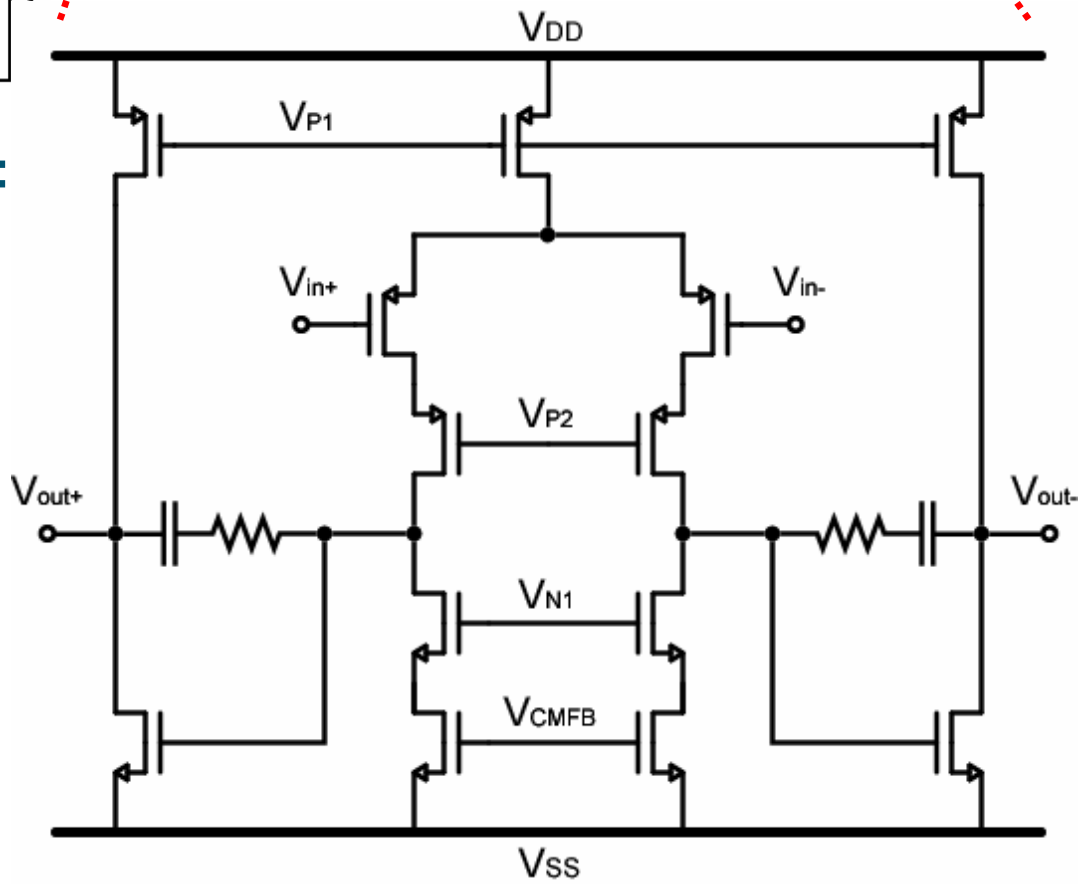
Opamp Design is Straightforward



Simulated Performance:

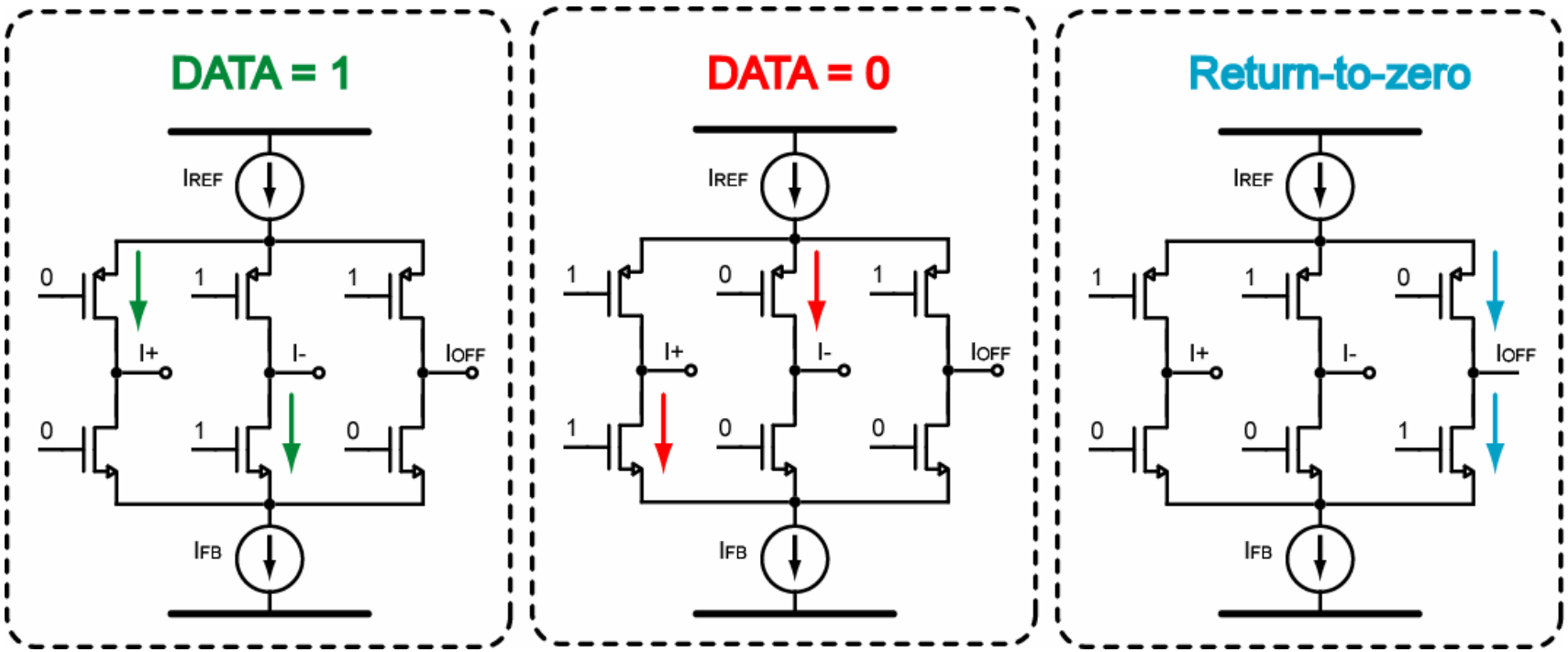
- A_V = 55 dB
- GBW = 2 GHz
- P_{DISS} = 15 mW

High SNR of VCO-based quantizer allows reduced opamp gain (A_V)

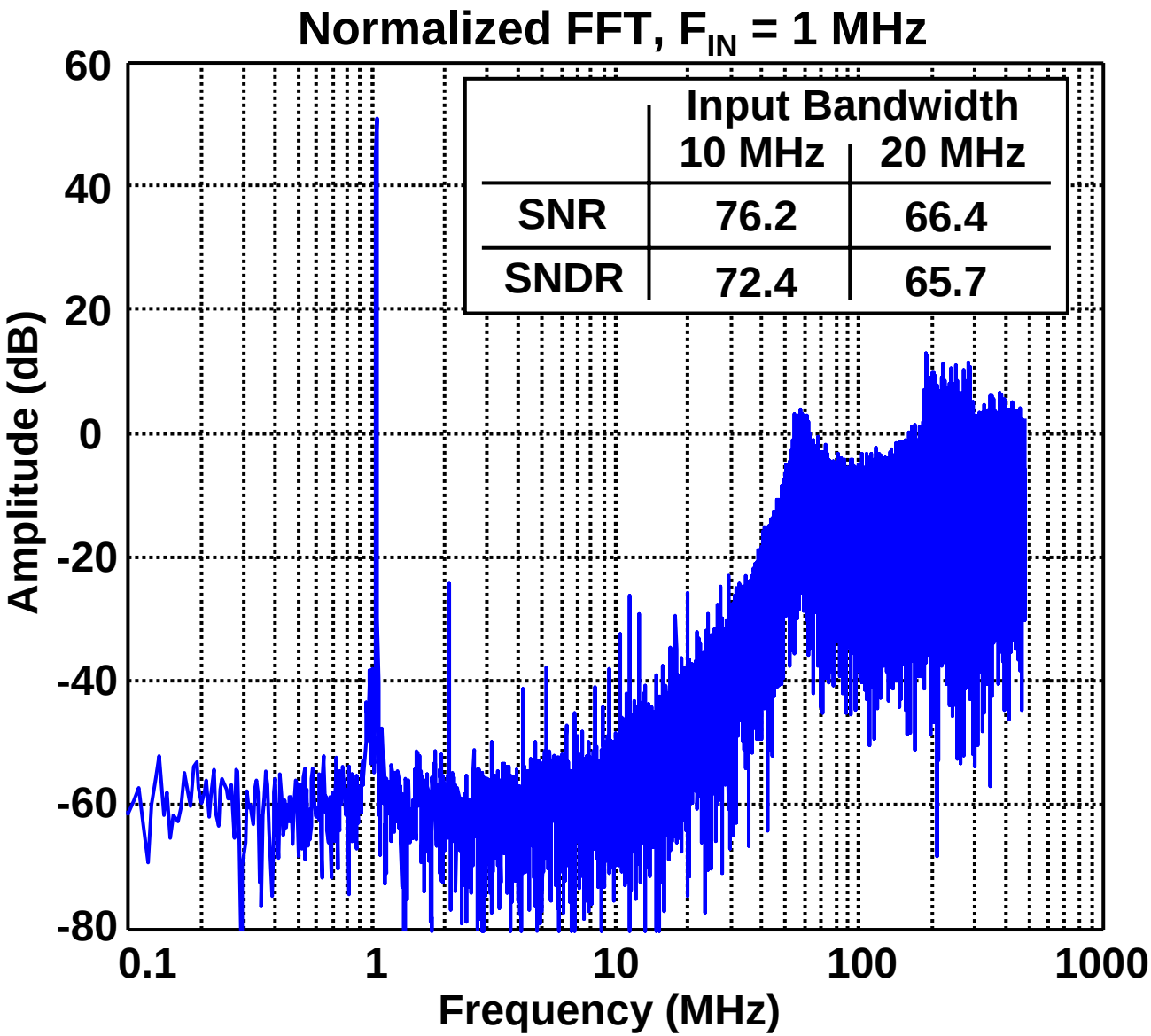


Primary Feedback DAC Schematic

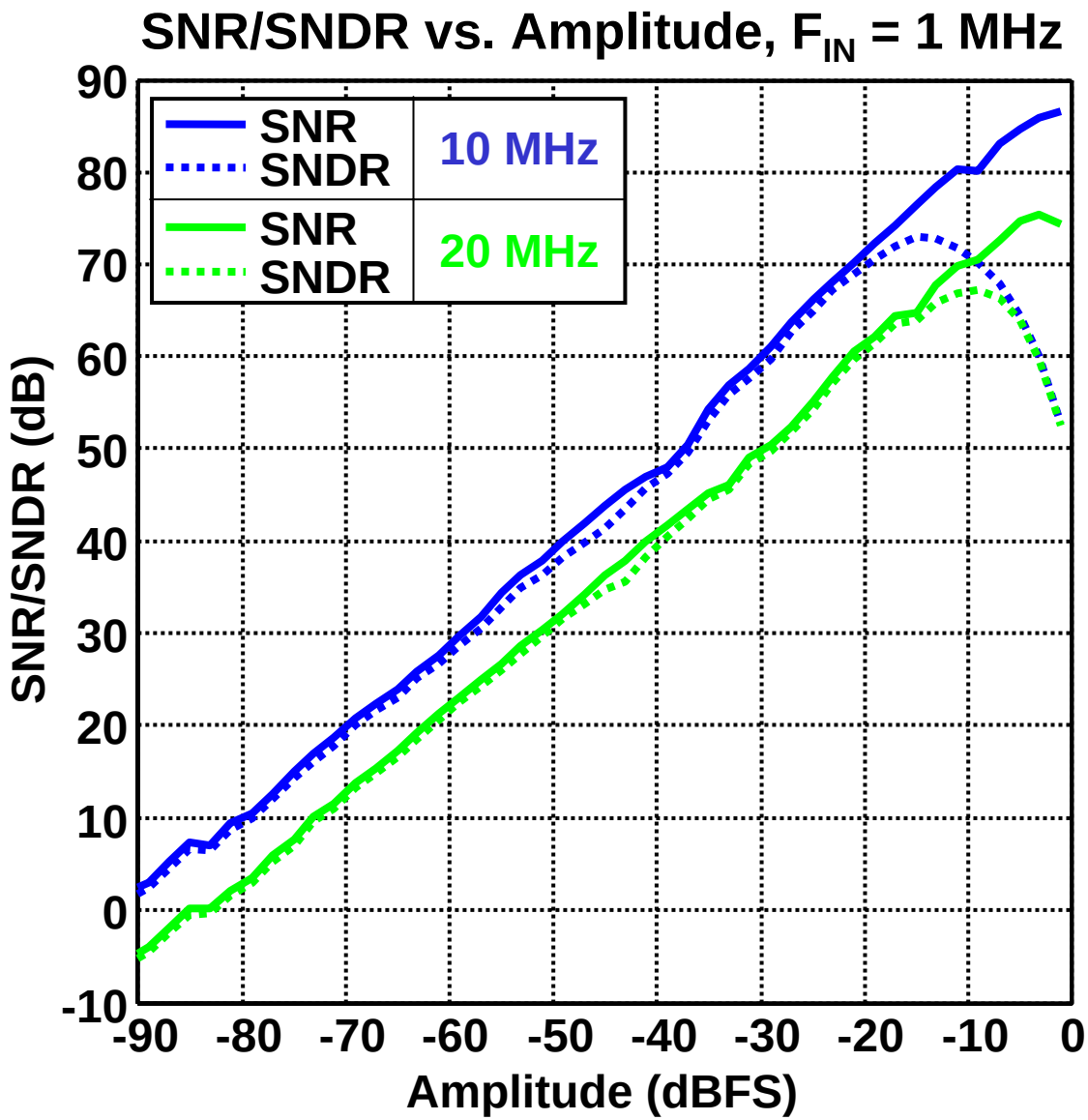
- Fully differential RZ pulses
- Triple-source current steering
- I_{OFF} is terminated off-chip



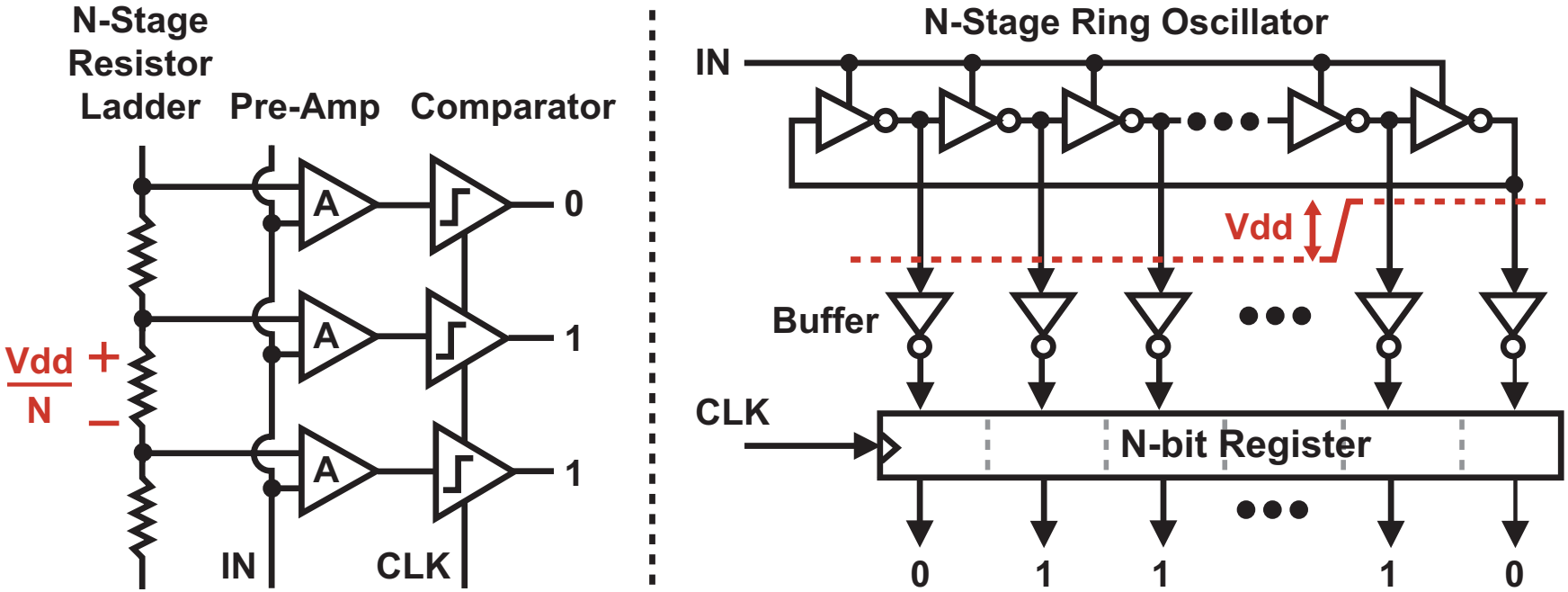
Measured Spectrum From Prototype



Measured SNR/SNDR Vs. Input Amplitude



Summarizing the Benefits of VCO-based Quantization

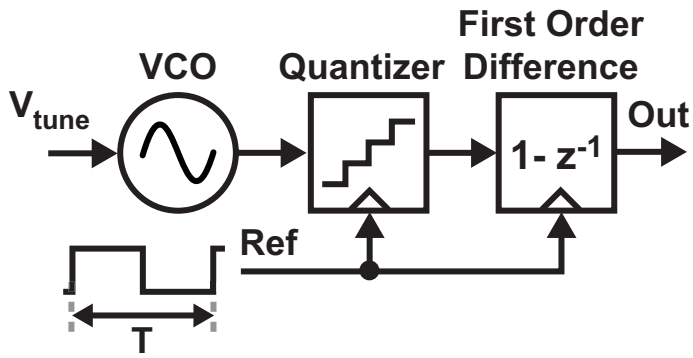


- Much more digital implementation
  - No resistor ladder or differential gain stages
- Offset and mismatch is not of concern in the design
- Metastability behavior is improved

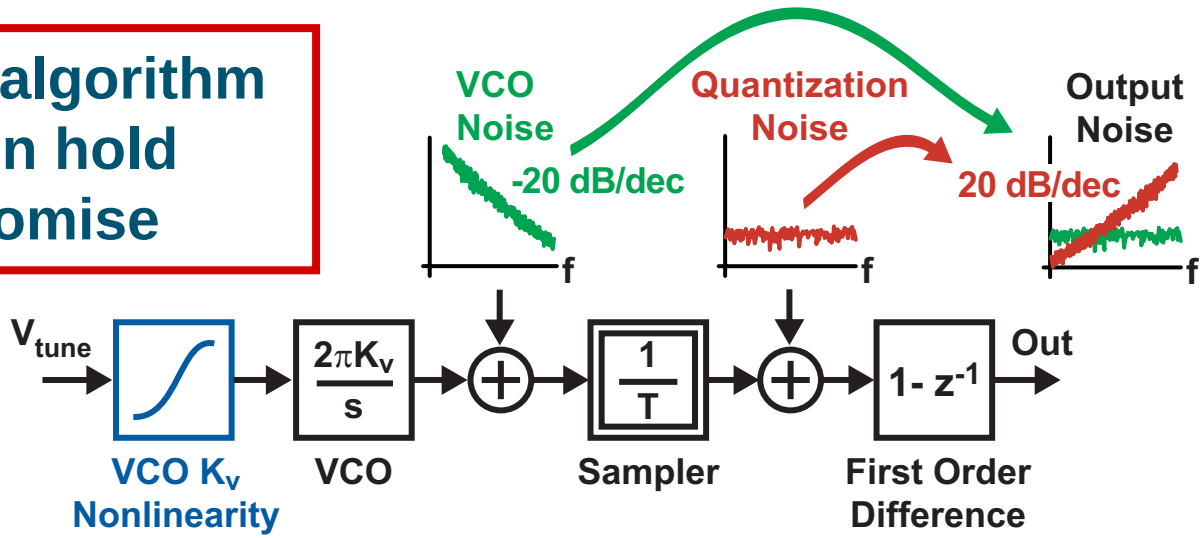
Implementation is high speed, low power, low area

How Do We Get Better Performance in the Future?

- Key issue: VCO voltage to frequency nonlinearity
- Possible paths to improvement
  - Analog calibration
  - Digital calibration
  - A more appropriate CT Sigma-Delta ADC topology



System and algorithm innovation hold much promise



Conclusions

- **VCO-based quantization is a promising component for achieving low power, high resolution, analog-to-digital conversion**
  - **High speed, low power, low area implementation since offset and mismatch is not of concern**
  - **First order noise shaping of quantization noise**
    - Lowers open loop gain requirements in CT Sigma-Delta ADC since quantizer has high SNR
  - **Improved metastability behavior**

- **12-bit ENOB, 10 MHz bandwidth ADC was demonstrated with 40 mW of power consumption**

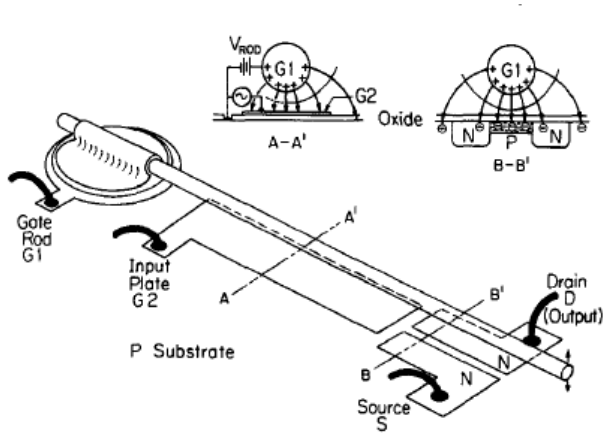
- **Key focus for future designs: reduce impact of VCO nonlinearity**

MEMS-based Clocking

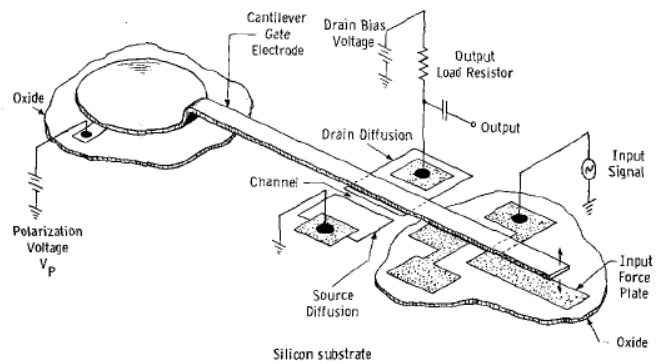
Aaron Partridge, SiTime, Inc.

Early Developments

- **Early MEMS resonator, 1965**
  - **The "Resonant Gate Transistor"**



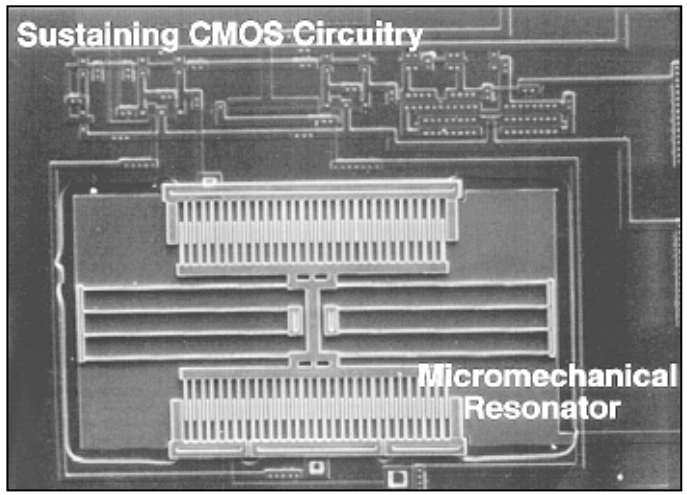
H.C. Nathanson, App. Phys. Lett. 1965



H.C. Nathanson, Trans. Elec. Des. 1967

Early Developments

- **Early MEMS resonator, 1965**
  - **The “Resonant Gate Transistor”**
- **Poly resonators and integrated electronics**
  - **True MEMS oscillators on a chip**



C.T.C. Nguyen, R.T. Howe, JSSC 1999

Early Developments

- **Early MEMS resonator, 1965**
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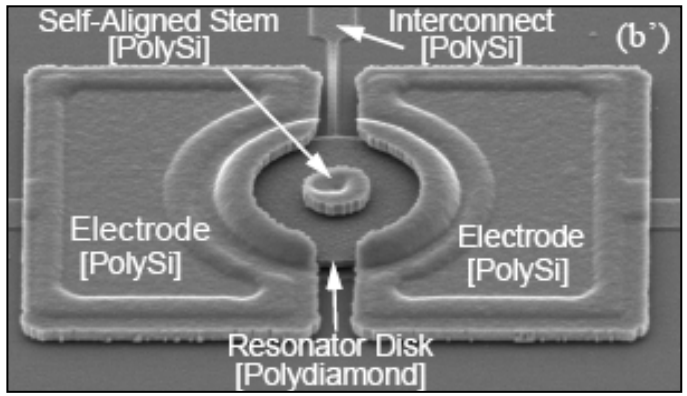
- **Poly resonators and integrated electronics**
  - **True MEMS oscillators on a chip**
- **Sometimes exotic materials**
  - **Diamond, Silicon Carbide**



J. Wang, C.T.C. Nguyen, MEMS'2004

Early Developments

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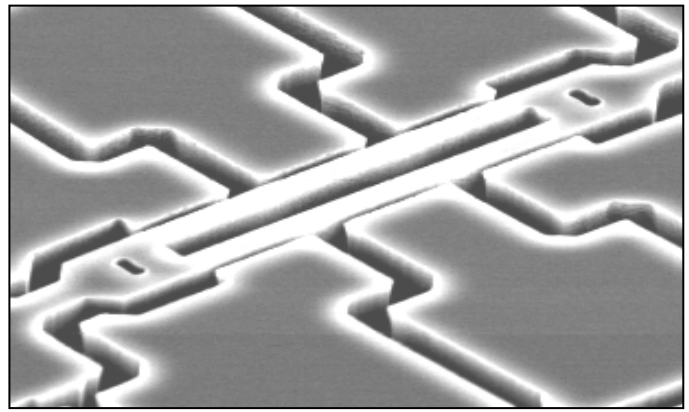
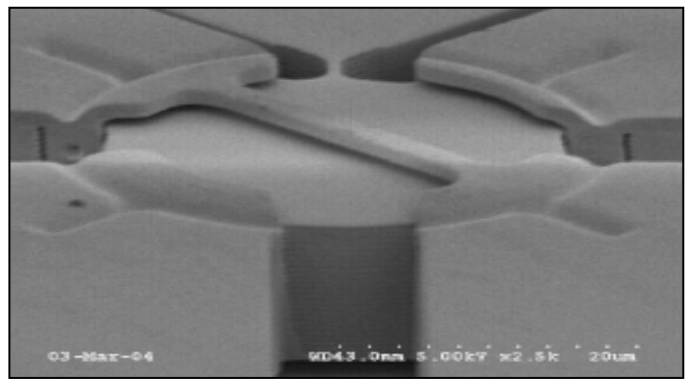
  - **The "Resonant Gate Transistor"**
- **Poly resonators and integrated electronics**
  - **True MEMS oscillators on a chip**
- **Sometimes exotic materials**
  - **Diamond, Silicon Carbide**
- **Now often trenched into SOI**
  - **Single Crystal Material**



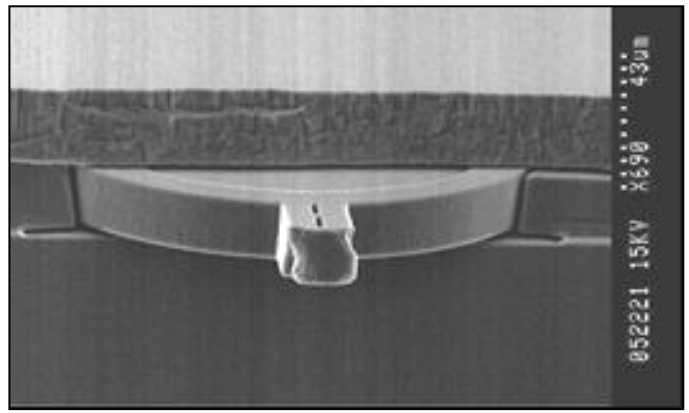
Tuning fork resonator trenched into SOI wafer surface.



S. Pourkamali, F. Ayazi, 2004

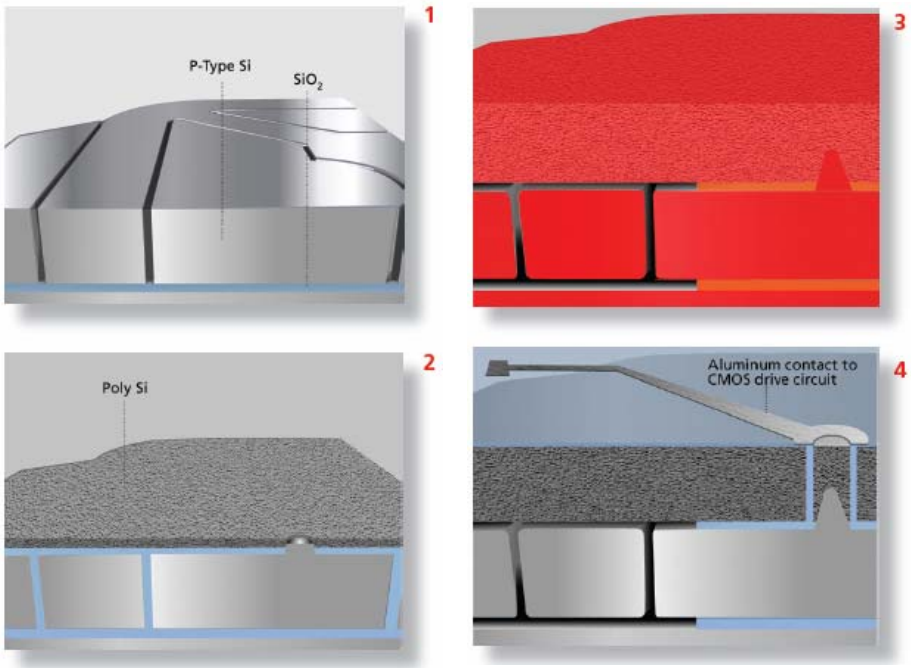
Early Developments

- **Early MEMS resonator, 1965**
  - **The "Resonant Gate Transistor"**
- **Poly resonators and integrated electronics**
  - **True MEMS oscillators on a chip**
- **Sometimes exotic materials**
  - **Diamond, Silicon Carbide**
- **Now often trenched into SOI**
  - **Single Crystal Material**
- **After 40 years, MEMS oscillators are on the market**



Tuning fork resonator in SOI with encapsulation cover.

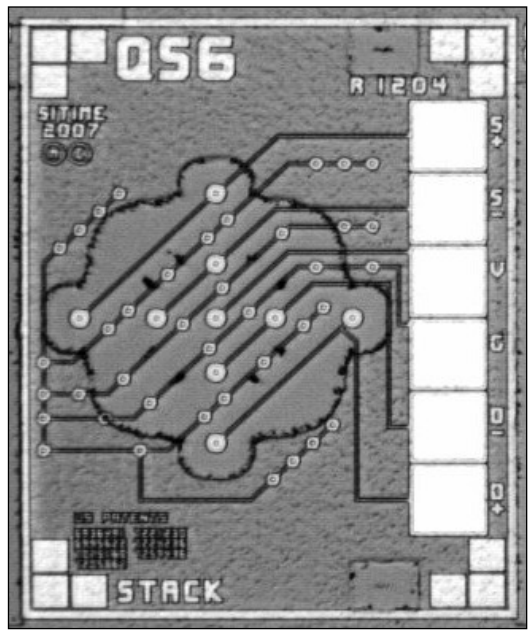
Key MEMS Fabrication Process Steps



- MEMS FirstTM invented by Markus Lutz, SiTime founder.
- EpiSealTM invented by Dr. Aaron Partridge, SiTime founder.
- The process took more than seven years to develop at Bosch, Stanford, and SiTime.

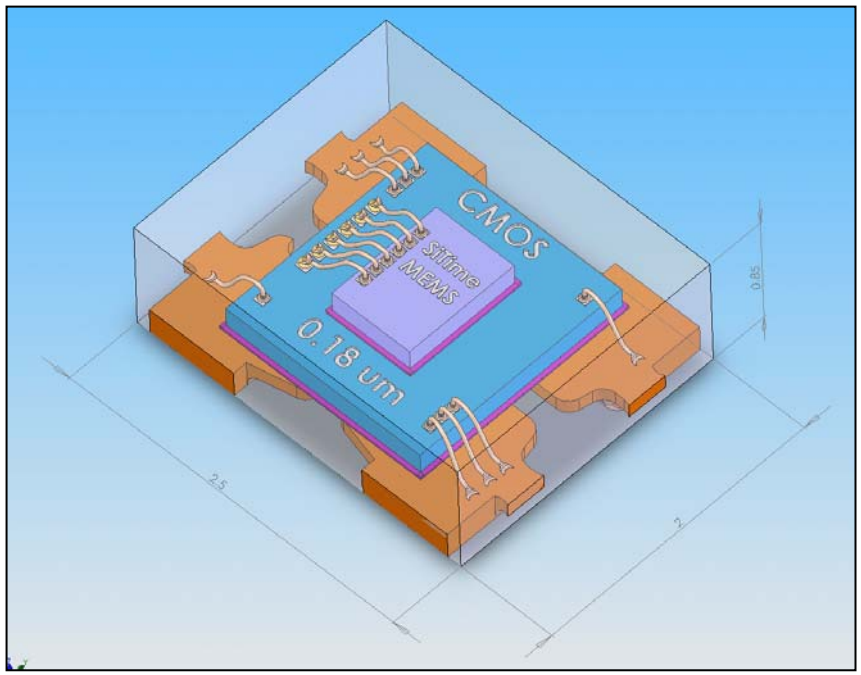
Completed Resonators

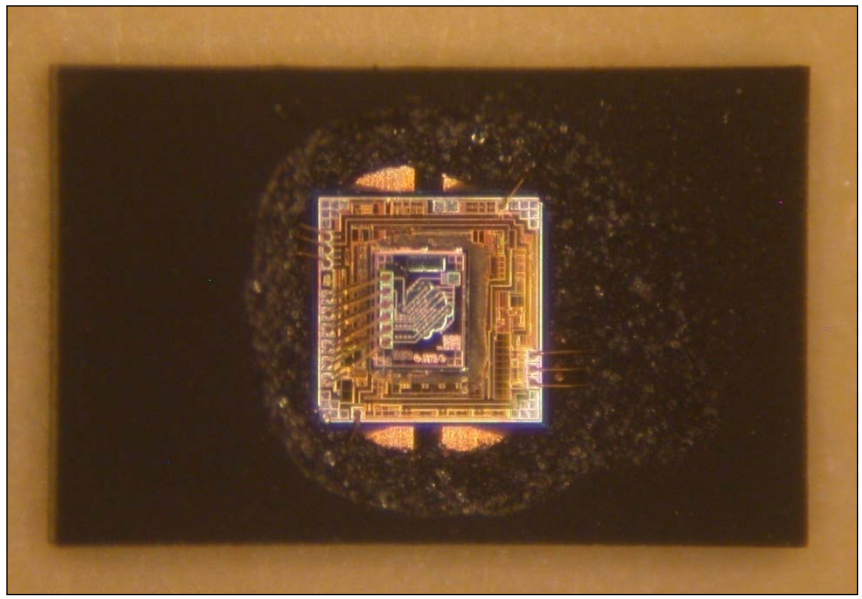
- **Size**
  - **140 micron thin**
  - **0.8 x 0.6 mm footprint**
- **Mechanically robust**
  - **Quad structure of resonator**
  - **SiTime's patented EpiSealTM protects the resonator** at the wafer level
- **Low cost**
  - **Standard IC packaging**
  - **50,000 resonators per wafer**



Stacked Die Construction

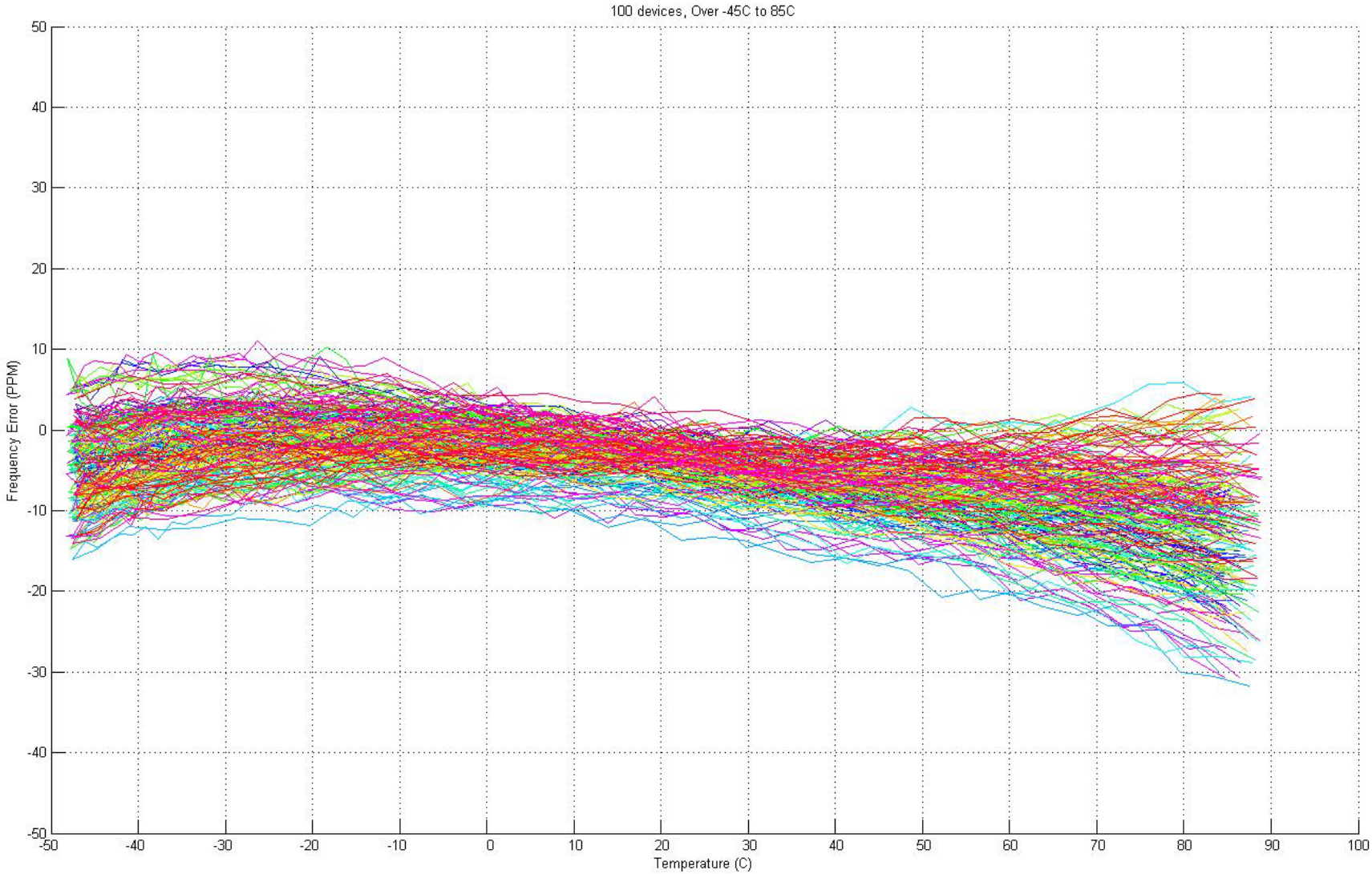
Fabrication Solid Model



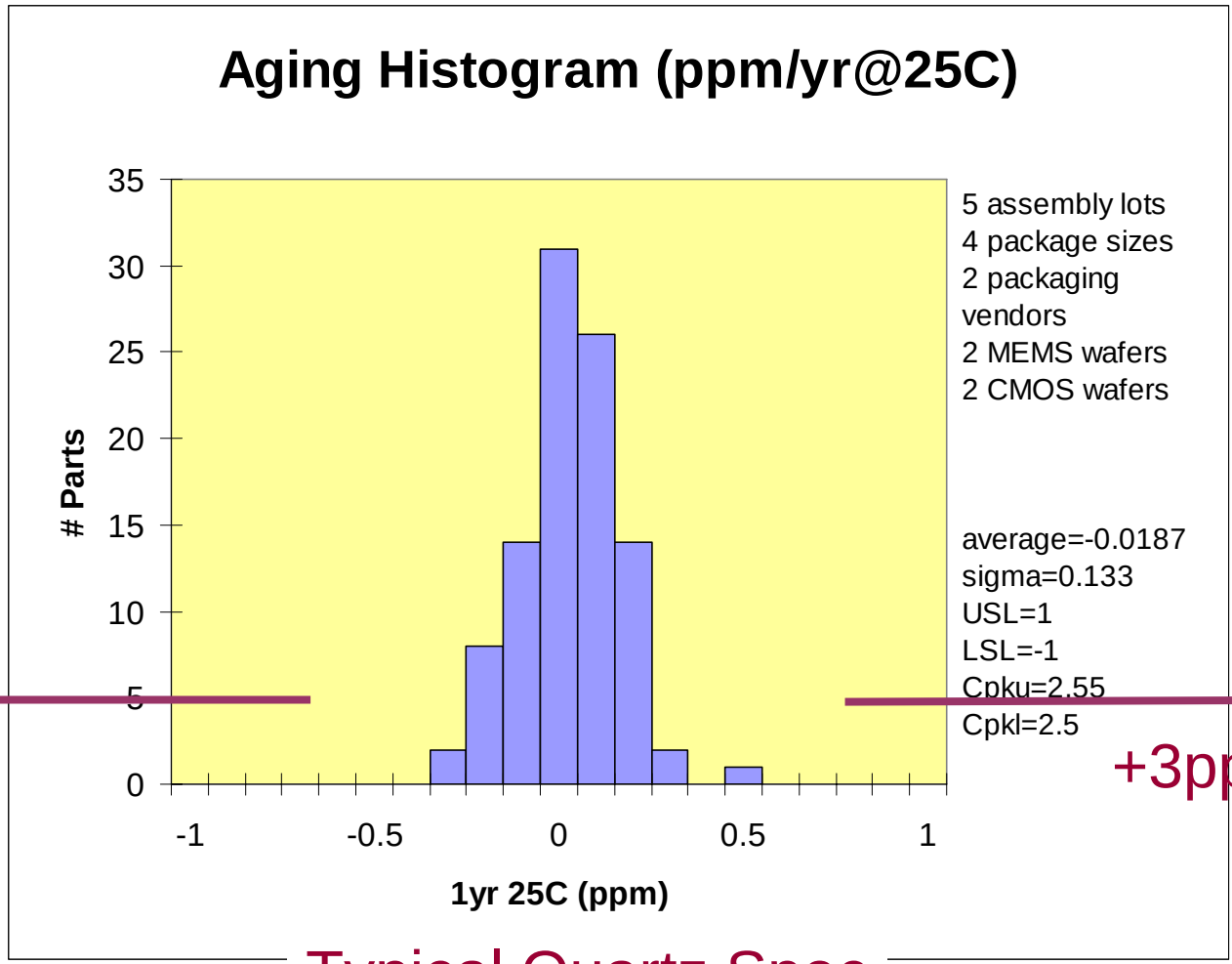


De-lid die photo

Frequency Stability Over Temperature

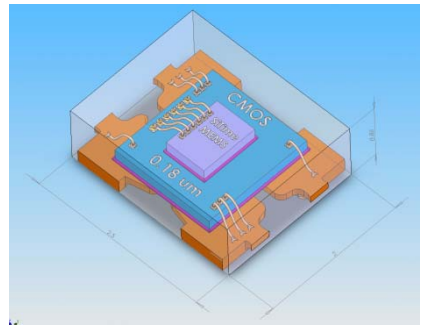


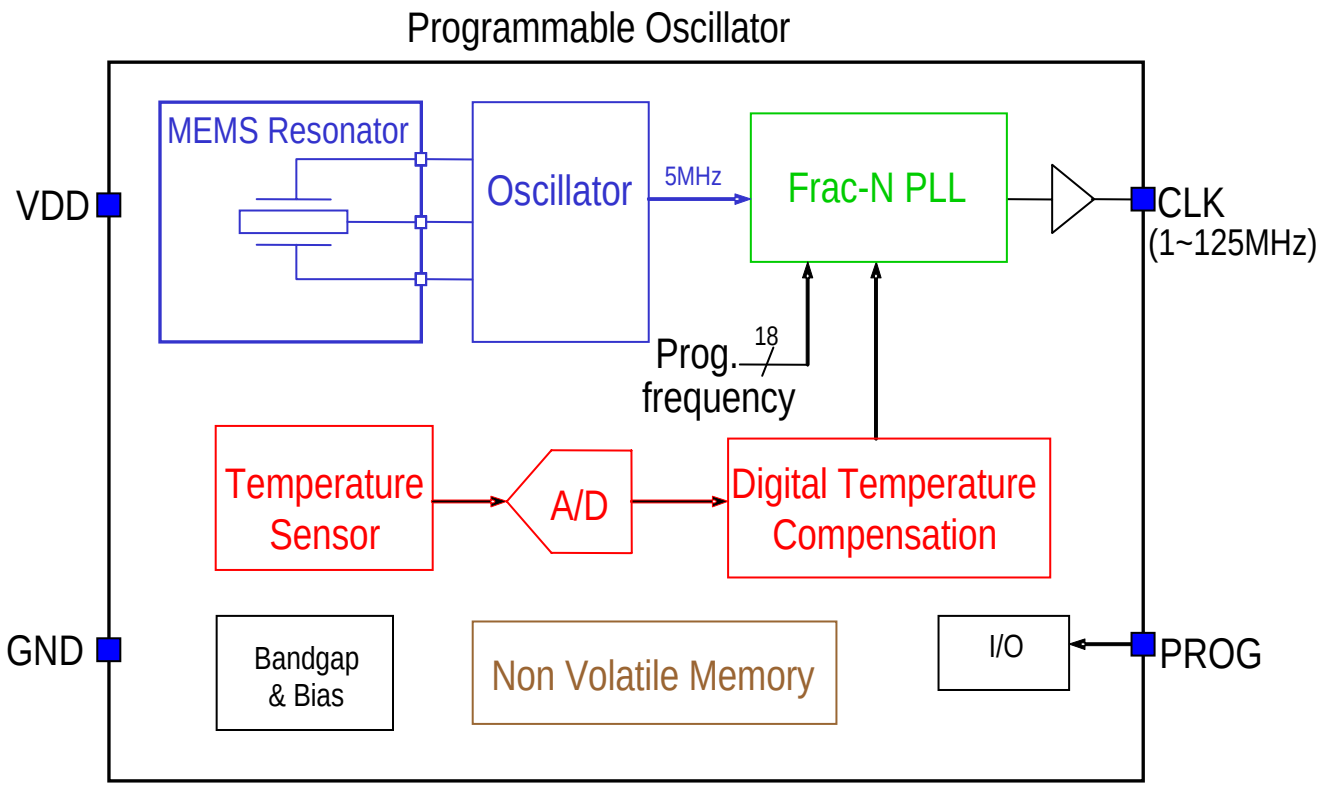
Frequency Stability: Aging 1year

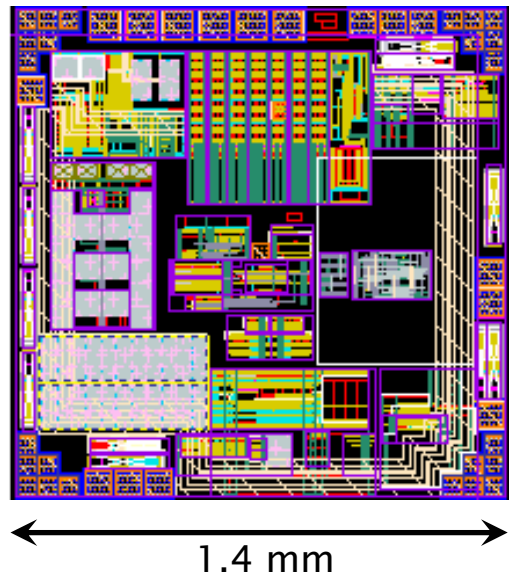


Typical Quartz Spec

Enough MEMS, What About the System Design?





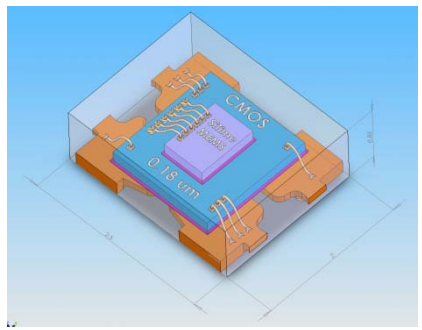


SiT8002 General Purpose Programmable Oscillators

In Mass Production!

- Drop-in replacements for quartz-based oscillators
  - Pin-out compatible
  - Footprint compatible
- Flexible architecture
  - Any Frequency: 1 MHz to 125 MHz
  - Any Voltage: 1.8 V, 2.5 V, or 3.3 V
  - Standby or Output Enable Modes
  - +/- 50 ppm over -40 to +85 C
- Always-in-stock: 3 week lead time
- Highly Mechanically Robust
  - 50,000G Shock test
  - 70G Vibration test from 20 to 1 kHz

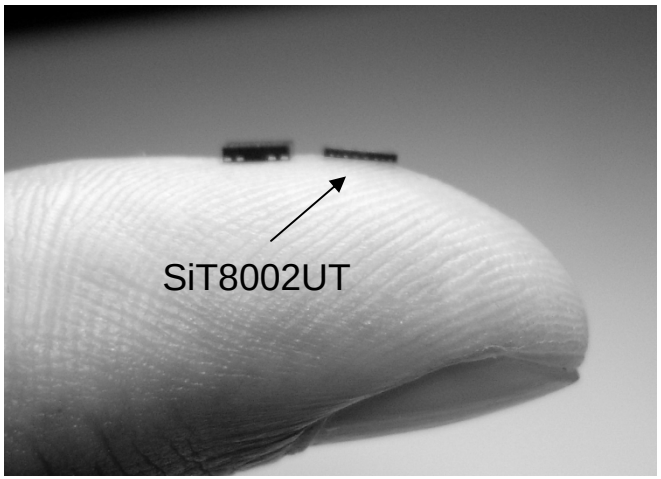
Pin Number	Pin Name	Pin Type	Pin Description
1	ST	Digital In	Standby
2	GND	Power	Connect to Ground
3	CLK	Digital Out	Clock Output
4	VDD	Power	Connect 1.8V, 2.5V or 3.3V



Frequency Range	Accuracy	Jitter	Current Consumption	Startup Time	VDD	Packages	Temp. Range
1 – 125 MHz	+/- 50 ppm +/- 100 ppm	20 ps rms period jitter	< 15 mA (no load)	Typical 12 ms	1.8, 2.5, 3.3 +/- 5%	2520, 3225, 5032, 7050	-40 to +85 C -10 to +70 C

SiT8002UT World's Thinnest Programmable Osc.

Samples NOW!



SiT8002UT: Flexible Timing Solution in a Tiny Package

- **Package thinness of <400 micron**
  - **Footprint: 3.5 x 3.0 mm**
  - **+/- 100 ppm over -40 to +85 C**

Frequency Range	Accuracy	Jitter	Current Consumption	Startup Time	VDD	Packages	Temp. Range
1 – 125 MHz	**+/- 100 ppm**	**20 ps rms period jitter**	**< 15 mA (no load)**	**Typical 12 ms**	**1.8, 2.5, 3.3 +/- 5%**	**3.5 x 3.0 x** 0.37 **mm**	**-40 to +85 C**

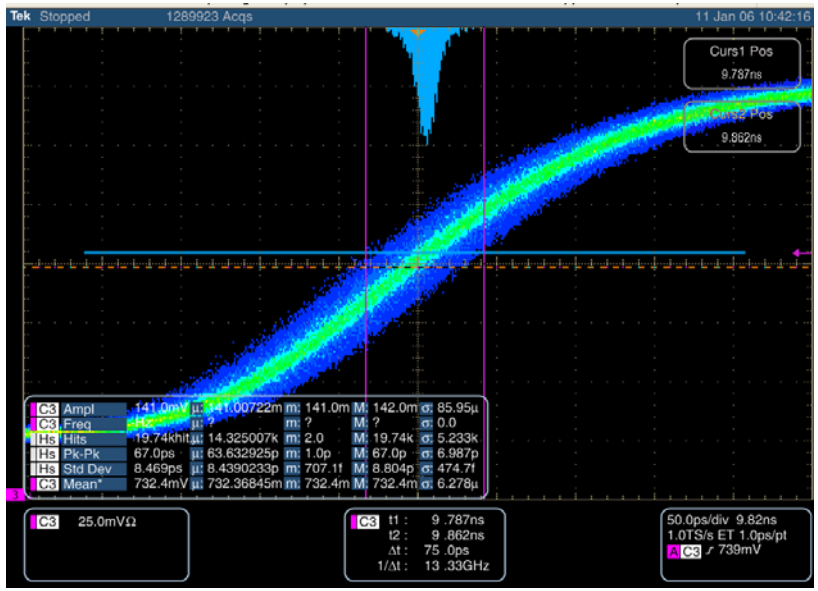
SiT8102 Lowest Jitter Programmable Oscillator

In Pre-Production!

SiT8102: High Performance Oscillator

- <1ps rms phase jitter (random)
- < 4 ps rms Period jitter

- **Typical programmable quartz oscillators:**
  - 15-25 ps rms Period jitter
- **Small size: 2.5x2.0x0.8 mm**
- **Typical applications:**
  - SATA, SAS, FibreChannel, Firewire (1394), Ethernet, 10G Ethernet, PCI Express



Frequency Range	Accuracy	Period Jitter	Current Consumption	Startup Time	VDD	Packages	Temp. Range
1 – 200 MHz	+/- 25ppm +/-50ppm +/-100ppm	<4 ps rms period jitter	< 17 mA (no load)	10 ms max	1.8, 2.5, 3.3V +/- 5%	2520, 3225, 5032, 7050	-40 to +85 C -10 to +70 C

Conclusions

- **Clock generation is required in all communication and computation systems**
  - **Quartz crystals have provided accurate timing for 40 years**
    - Present a barrier to achieving higher levels of integration
- **MEMS-based clocking allows higher levels of integration**
  - **Temperature and process variations can be handled through circuit design and calibration**
  - **Provides a platform for clocking solutions with expanded functionality and very high levels of integration**

Summary of Short Course

- **PLLs have been around for over 70 years, but still present an exciting research area**
  - **Digital phase-locked loops provide an exciting platform for improving PLL performance**
    - Joint circuit/algorithm approaches
    - New TDC designs will be key to excellent performance
  - **Analog circuits will continue to play an important role**
    - Achieve high resolution and speed much more efficiently than digital circuits
  - **New technologies will allow better performance and higher levels of integration**
    - Optical/electrical integration
    - MEMS-based resonator technology