Tutorial on
Digital Phase-Locked Loops
CICC 2009

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Why Are Digital Phase-Locked Loops Interesting?

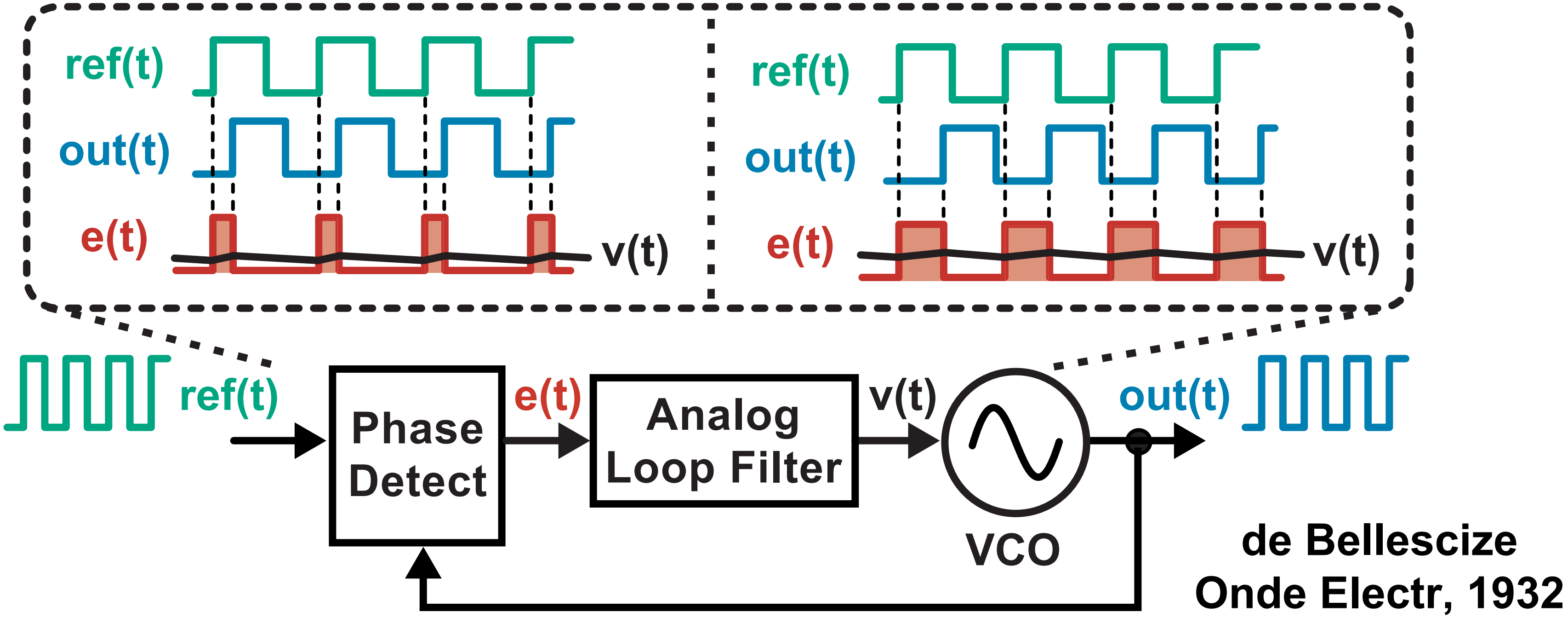
- **Performance is important**
  - **Phase noise can limit wireless transceiver performance**
  - **Jitter can be a problem for digital processors**

- **The standard analog PLL implementation is problematic in many applications**
  - **Analog building blocks on a mostly digital chip pose design and verification challenges**
  - **The cost of implementation is becoming too high …**

Can digital phase-locked loops offer excellent performance with a lower cost of implementation?

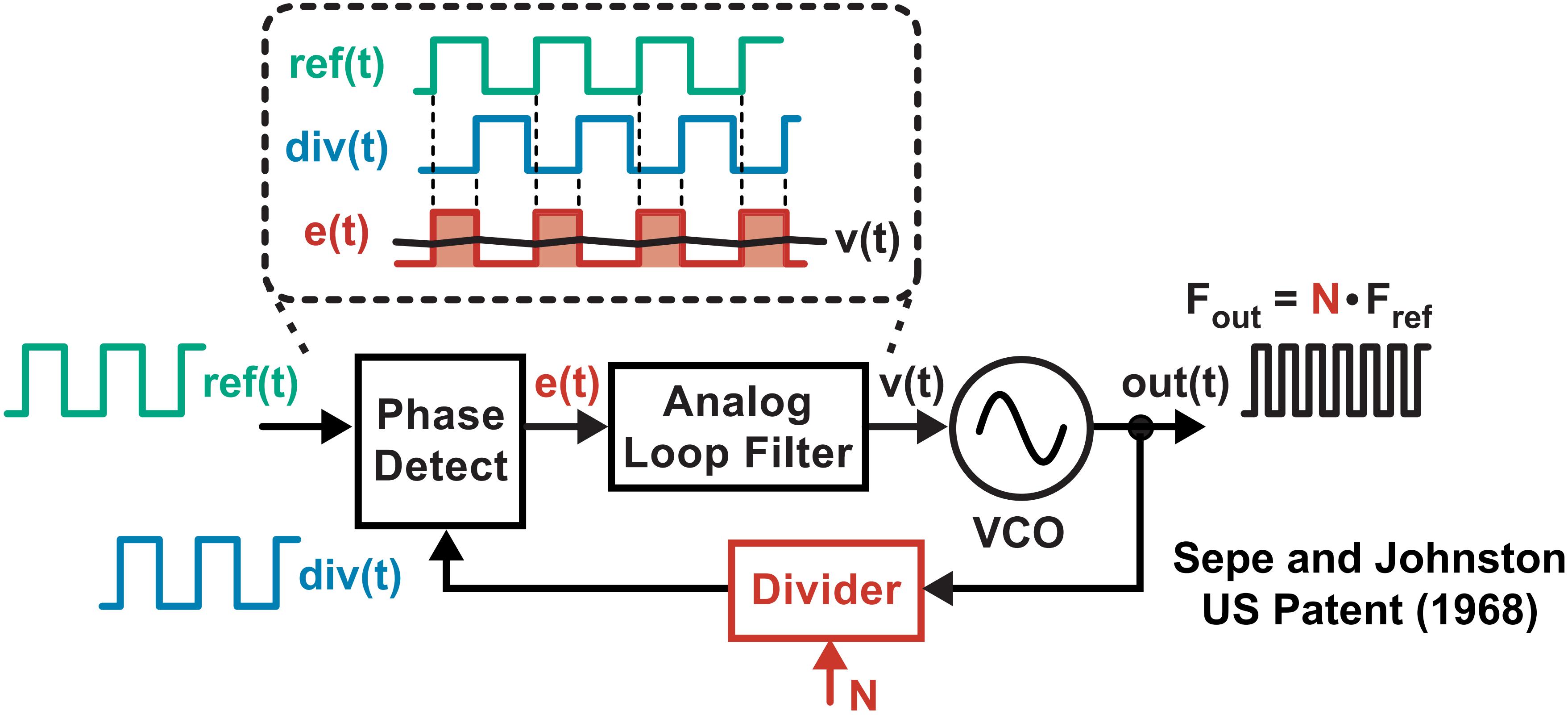
Just Enough PLL Background …

What is a Phase-Locked Loop (PLL)?



- **VCO efficiently provides oscillating waveform with variable frequency**
- **PLL synchronizes VCO frequency to input reference frequency through feedback**
  - **Key block is phase detector**
    - Realized as *digital gates* that create pulsed signals

Integer-N Frequency Synthesizers

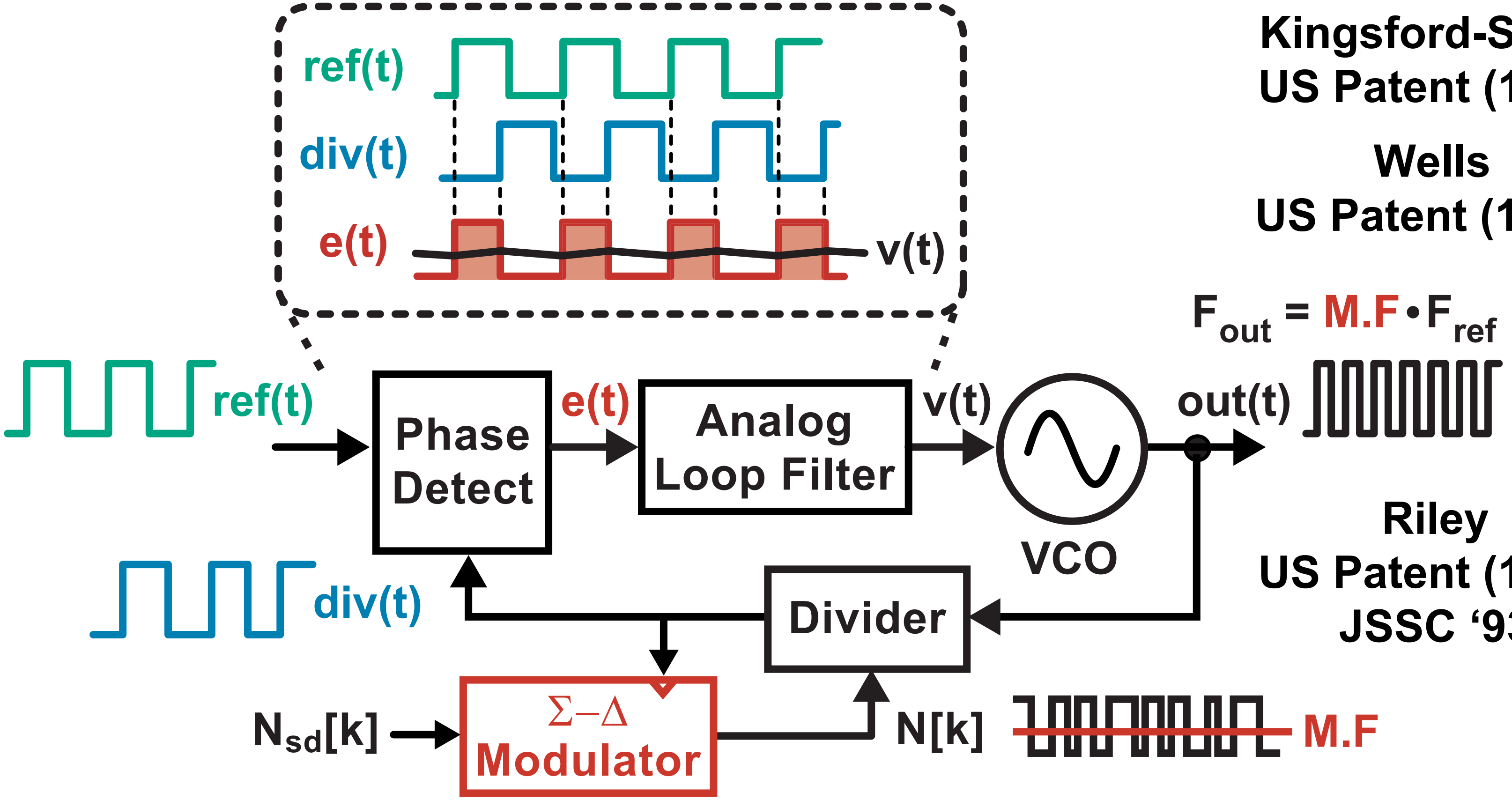


Sepe and Johnston
US Patent (1968)

- Use digital counter structure to divide VCO frequency
  - Constraint: must divide by integer values
- Use PLL to synchronize reference and divider output

Output frequency is digitally controlled

Fractional-N Frequency Synthesizers



Kingsford-Smith
US Patent (1974)

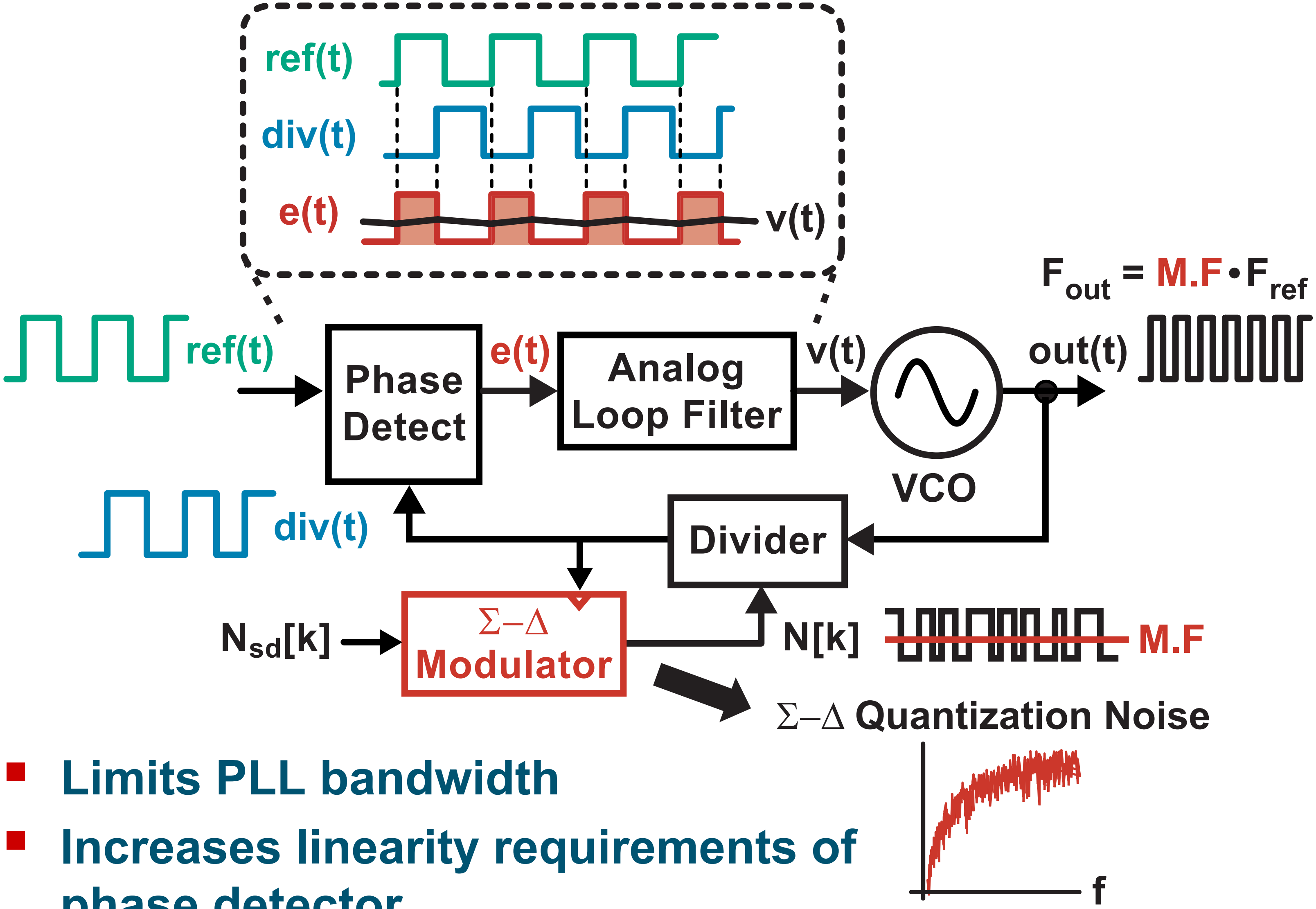
Wells
US Patent (1984)

Riley
US Patent (1989)
JSSC '93

- **Dither divide value to achieve fractional divide values**
  - **PLL loop filter smooths the resulting variations**

Very high frequency resolution is achieved

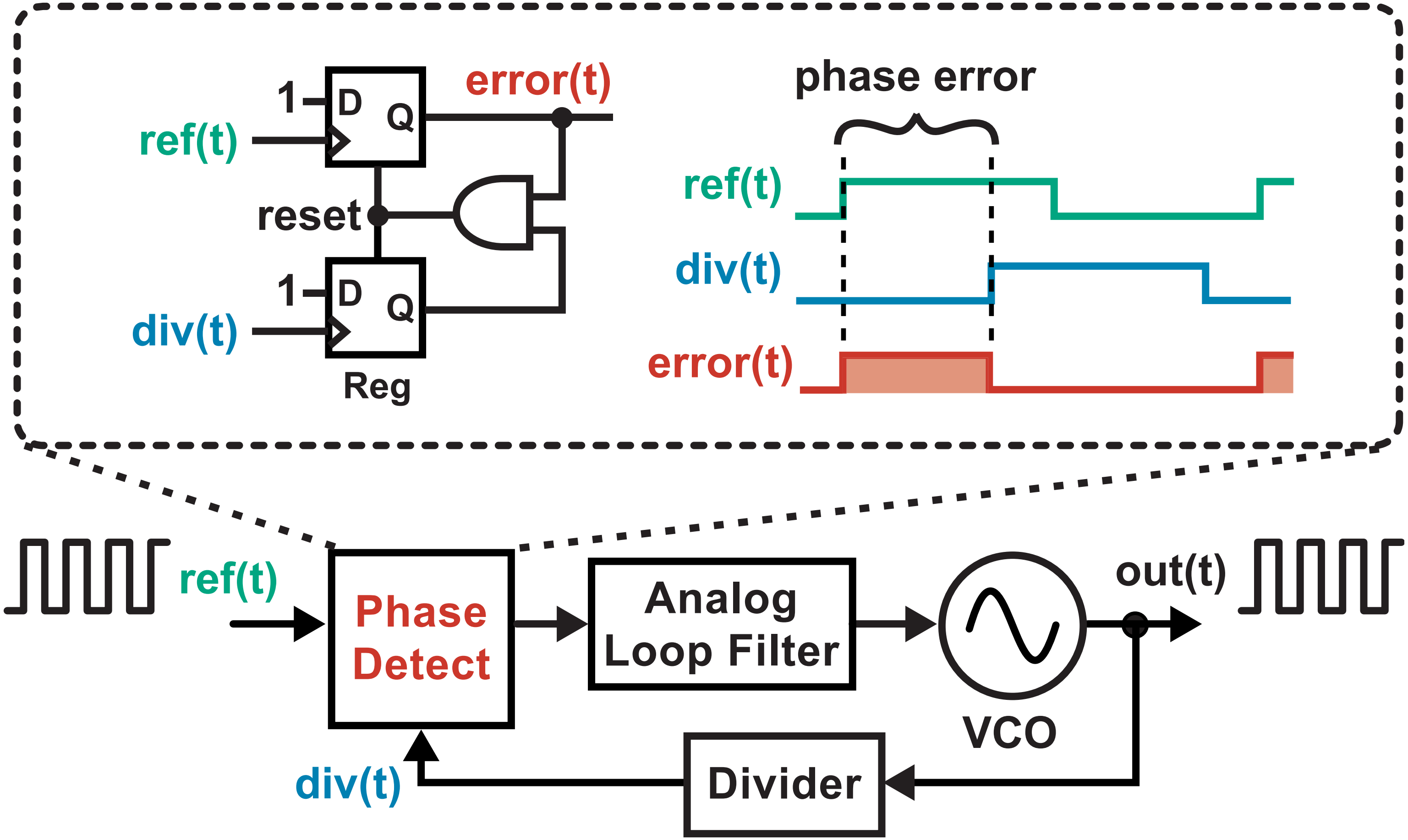
The Issue of Quantization Noise



- Limits PLL bandwidth
- Increases linearity requirements of phase detector

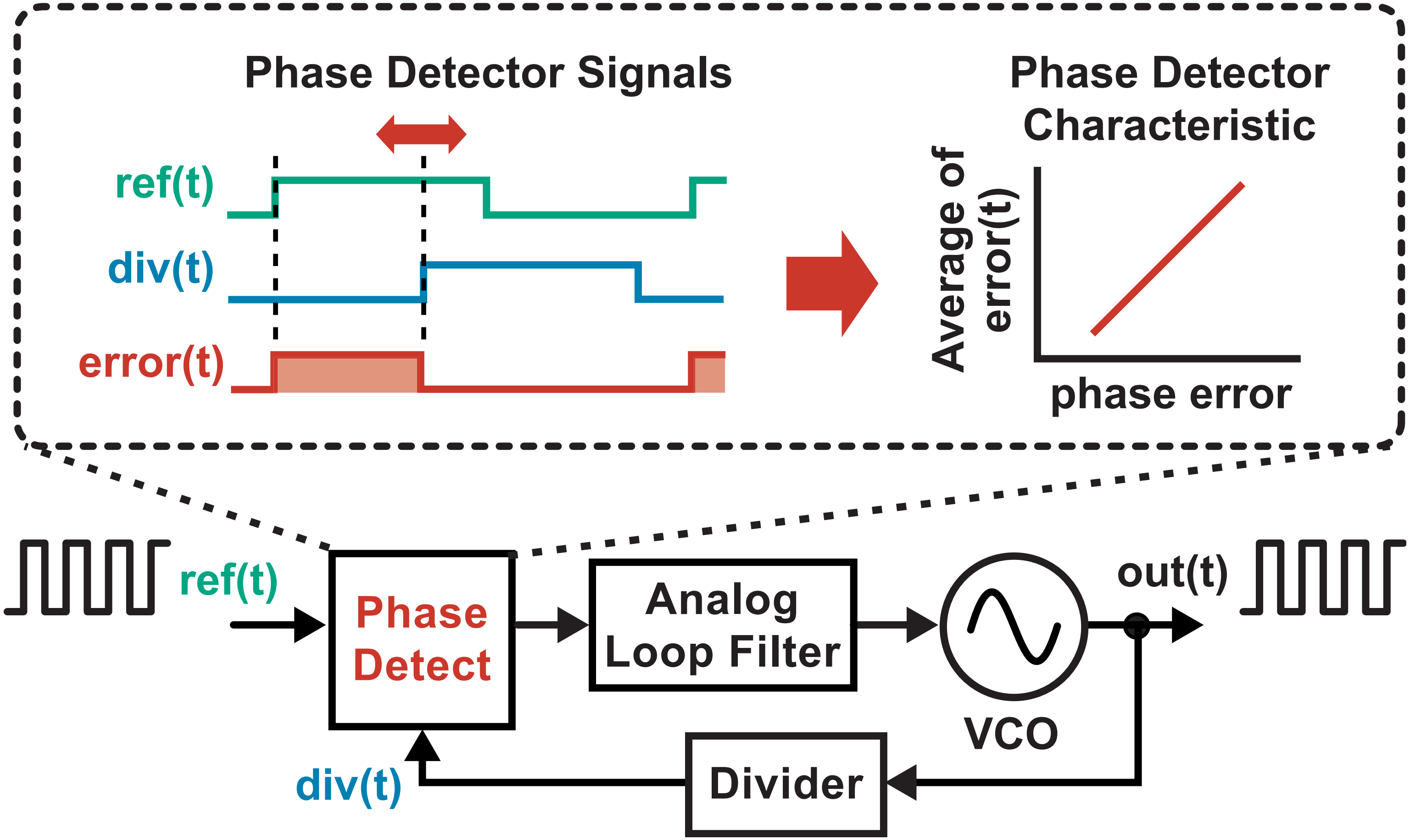
Striving for a Better PLL Implementation

Analog Phase Detection



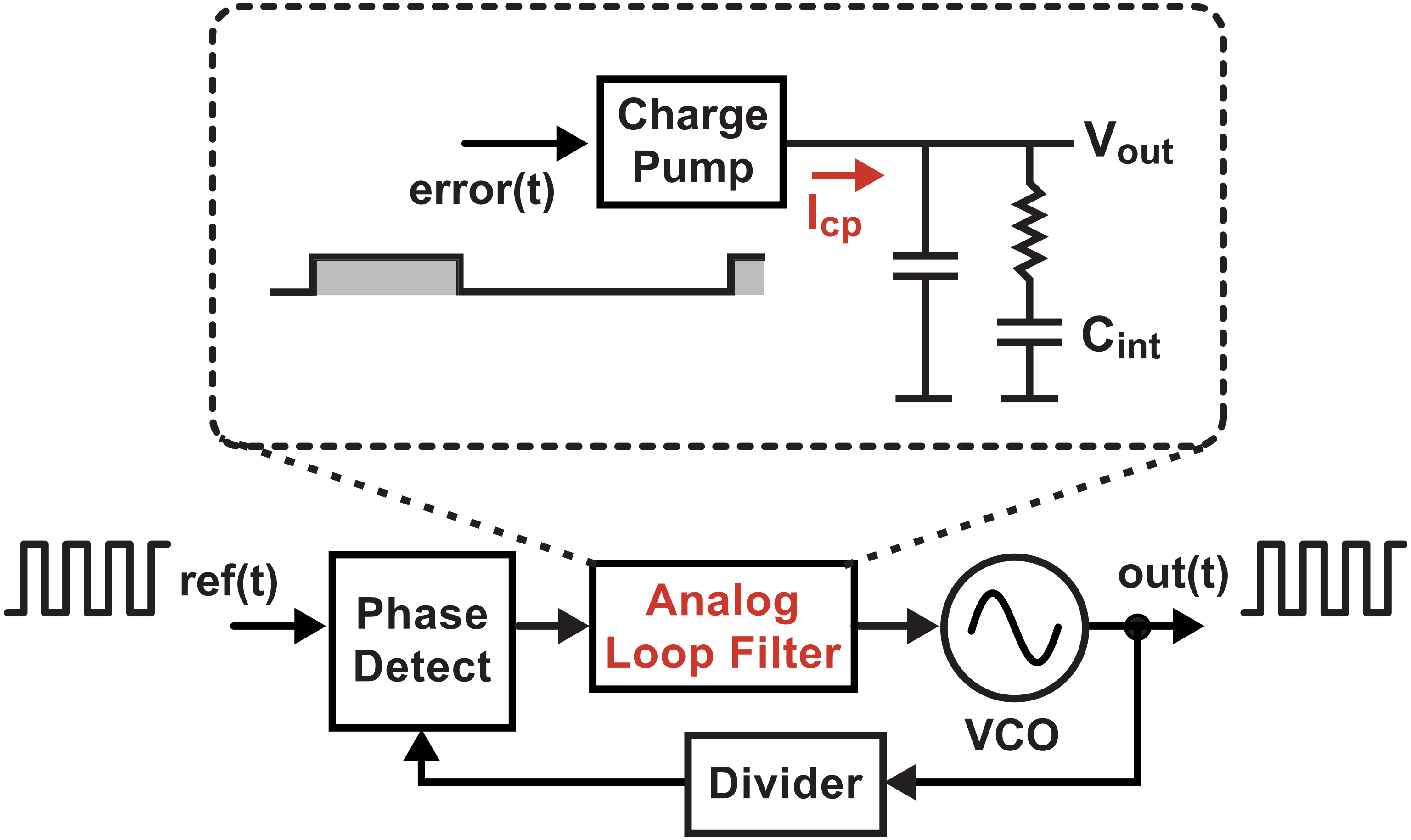
- Pulse width is formed according to phase difference between two signals
- Average of pulsed waveform is applied to VCO input

Tradeoffs of Analog Approach



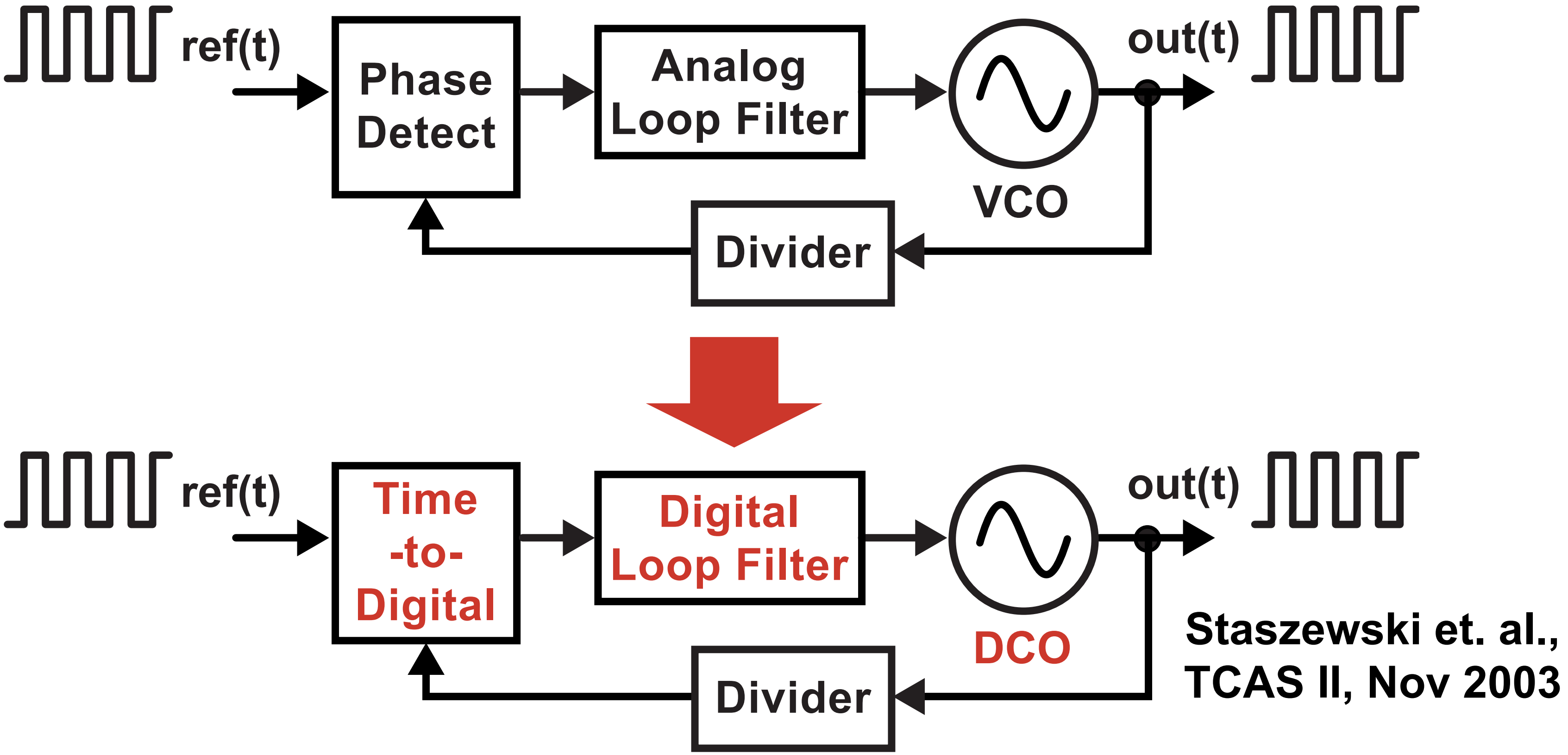
- **Benefit: average of pulsed output is a continuous, linear function of phase error**
- **Issue: analog loop filter implementation is undesirable**

Issues with Analog Loop Filter



- **Charge pump: output resistance, mismatch**
- **Filter caps: leakage current, *large area***

Going Digital …



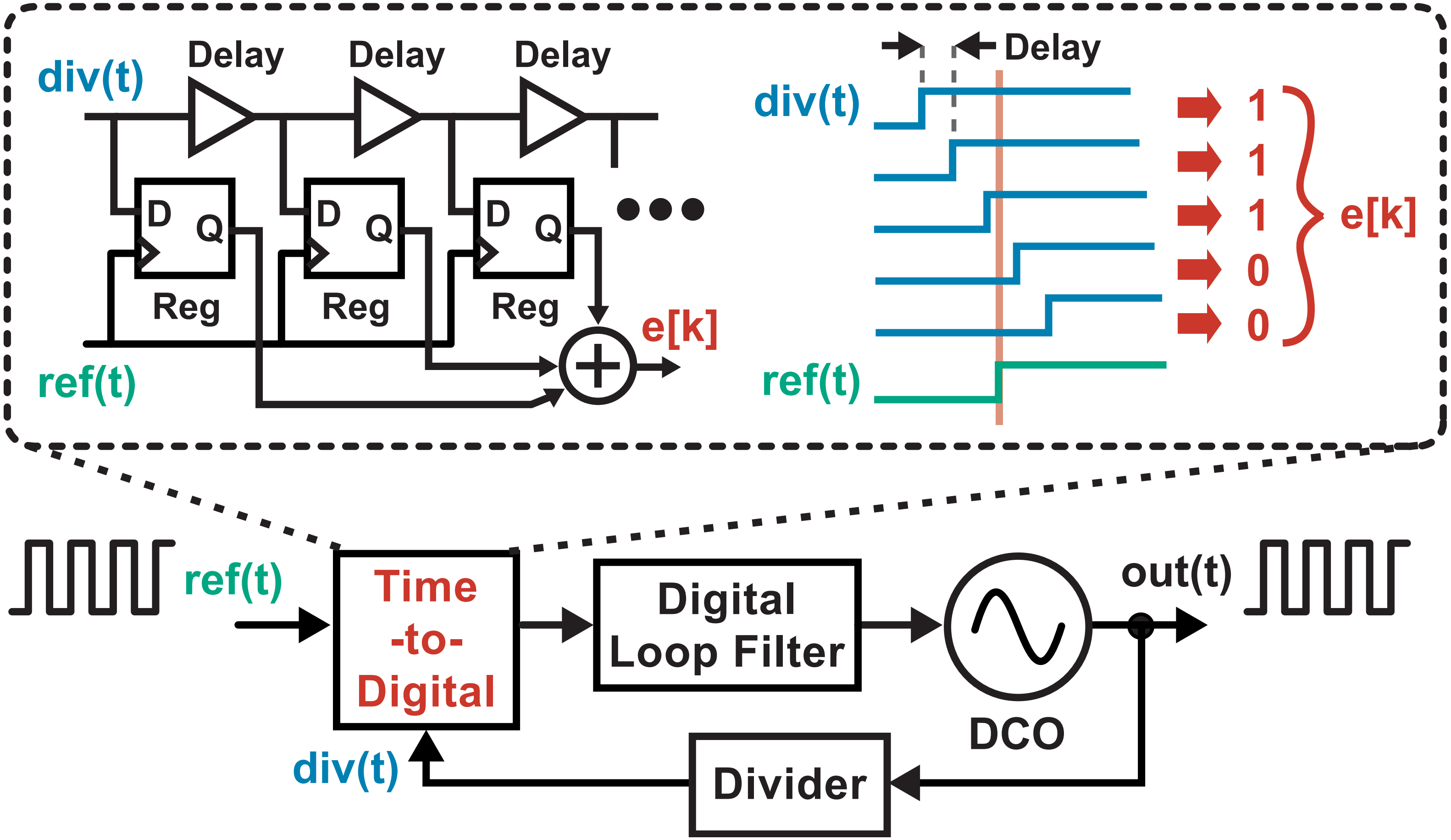
Staszewski et. al., TCAS II, Nov 2003

- Digital loop filter: compact area, insensitive to leakage
- Challenges:
  - Time-to-Digital Converter (TDC)
  - Digitally-Controlled Oscillator (DCO)

Outline of Talk

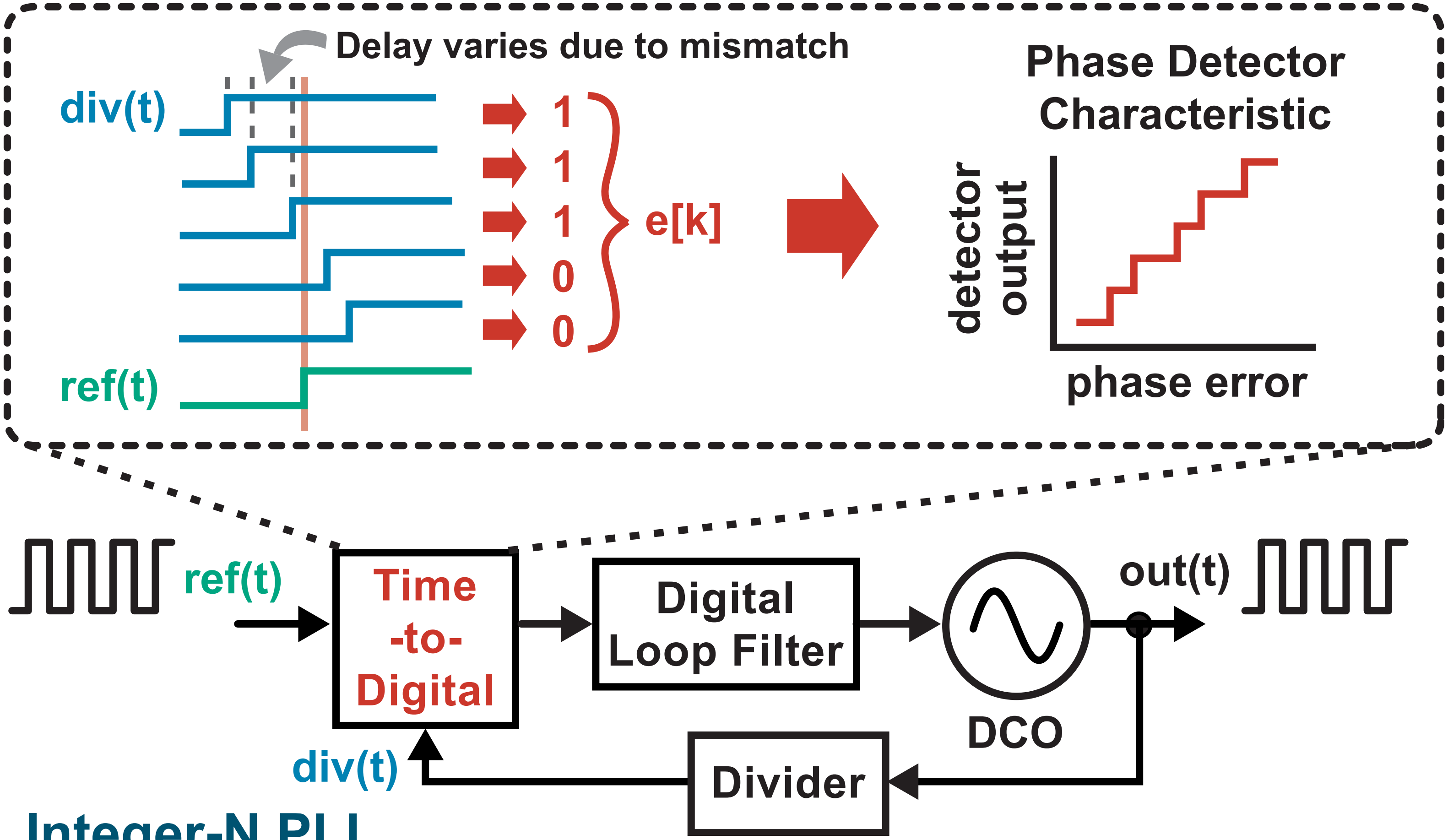
- Overview of Key Blocks (TDC and DCO)
- Modeling & CAD Tools
- High Performance TDC design
- Quantization Noise Cancellation
- DCO based on an efficient passive DAC structure
- Divider Design
- Loop Filter Design
- Prototype with measured Results

Classical Time-to-Digital Converter



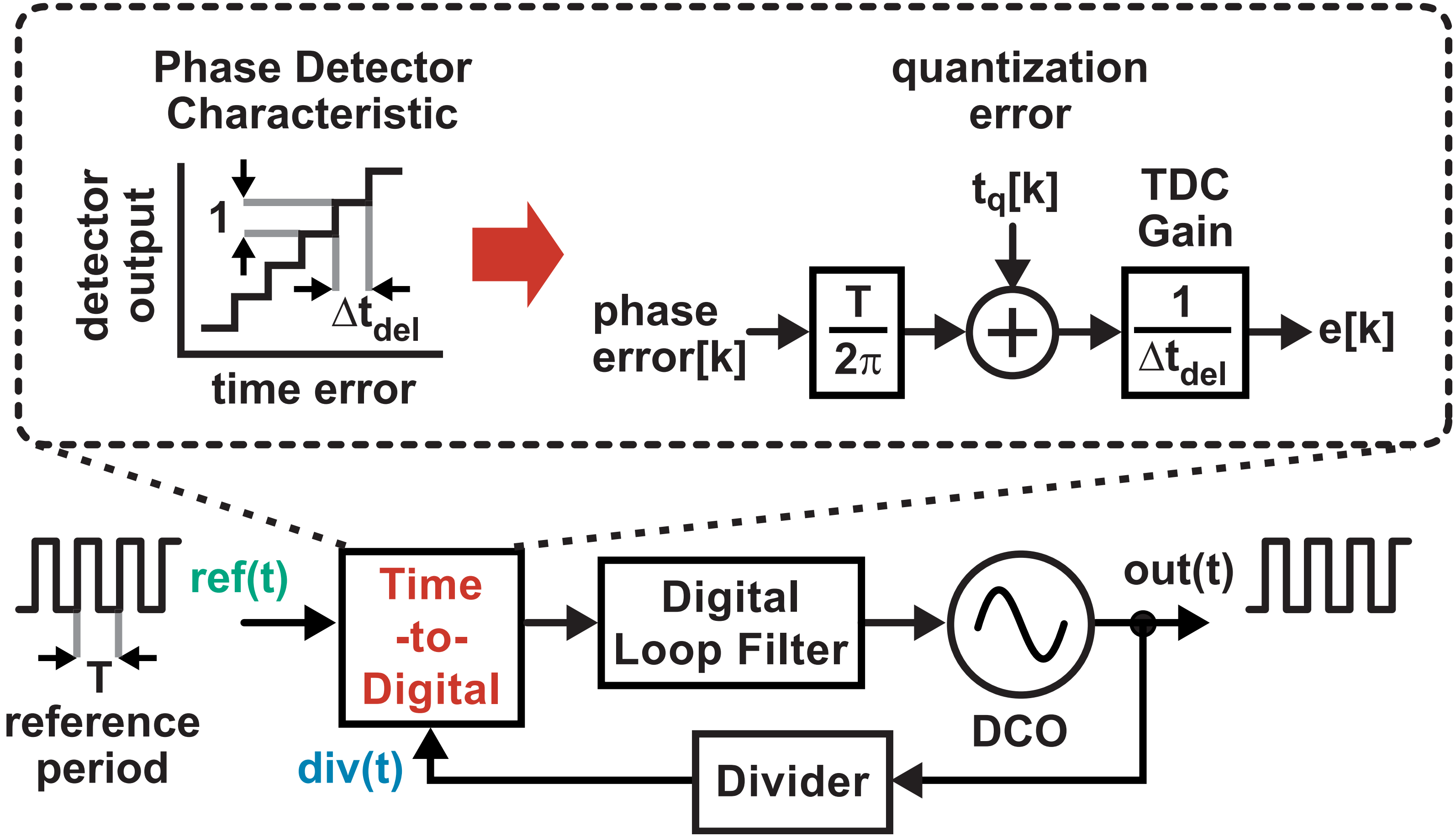
- Resolution set by a “Single Delay Chain” structure
  - Phase error is measured with delays and registers
- Corresponds to a flash architecture

Impact of Limited Resolution and Delay Mismatch



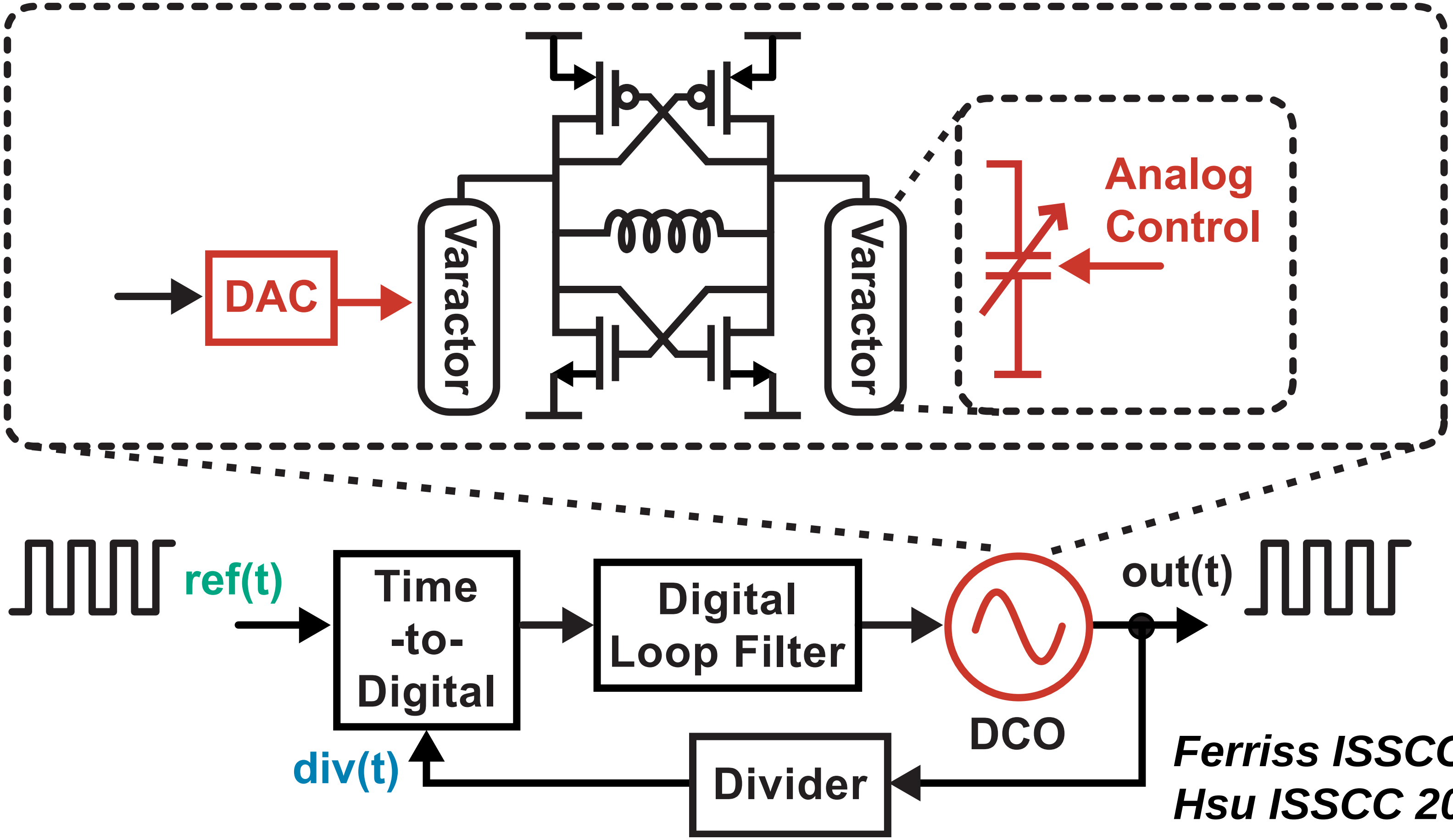
- **Integer-N PLL**
  - **Limit cycles due to limited resolution (unless high ref noise)**
- **Fractional-N PLL**
  - **Fractional spurs due to non-linearity from delay mismatch**

Modeling of TDC



- Phase error converted to time error by scale factor: *$T/2\pi$*
- TDC introduces quantization error: *$t_q[k]$*
- TDC gain set by average delay per step: *Δt_{del}*

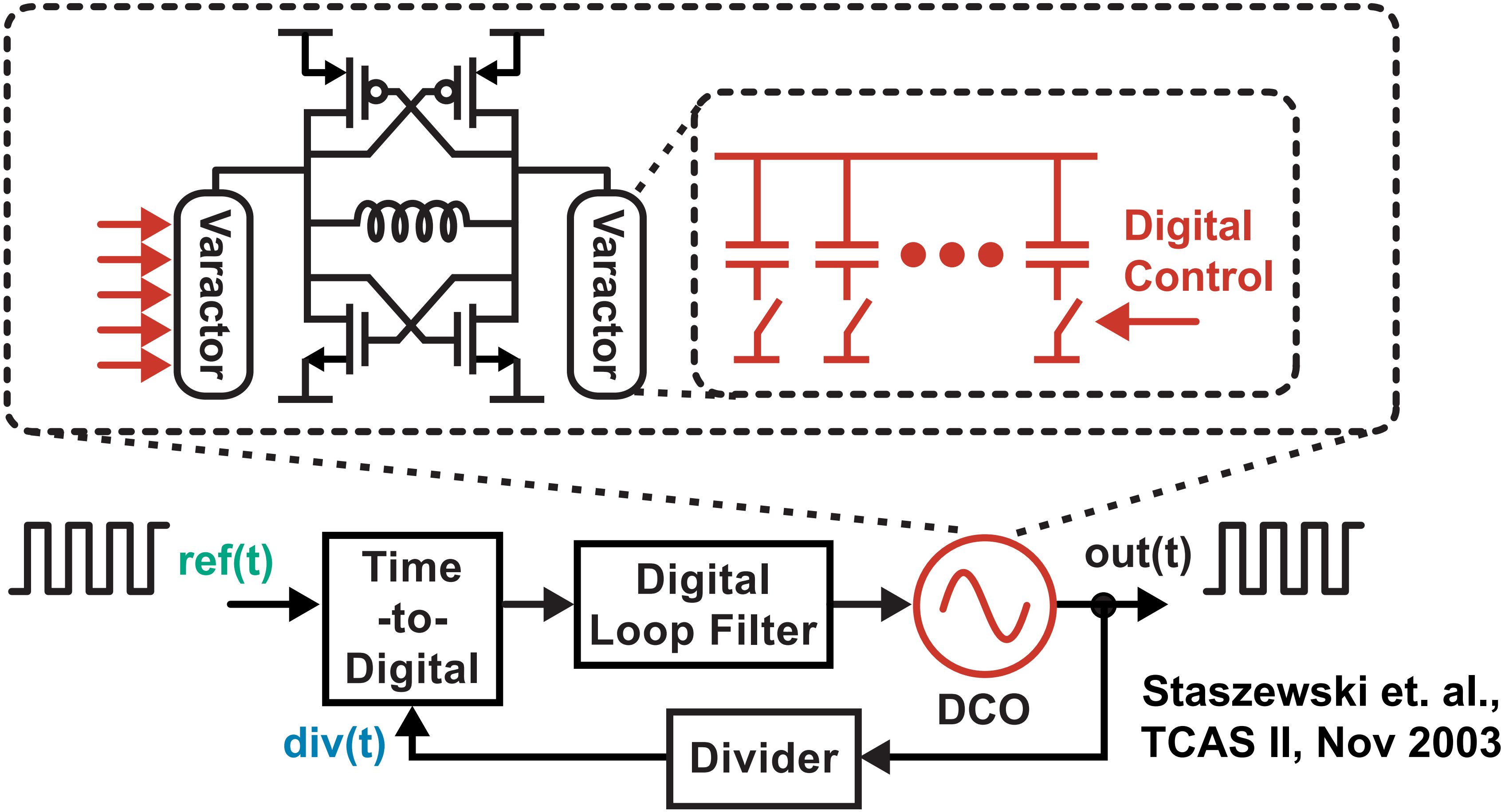
A Straightforward Approach for Achieving a DCO



Ferriss ISSCC 2007
Hsu ISSCC 2008

- Use a DAC to control a conventional LC oscillator
  - Allows the use of an existing VCO within a digital PLL
  - Can be applied across a broad range of IC processes

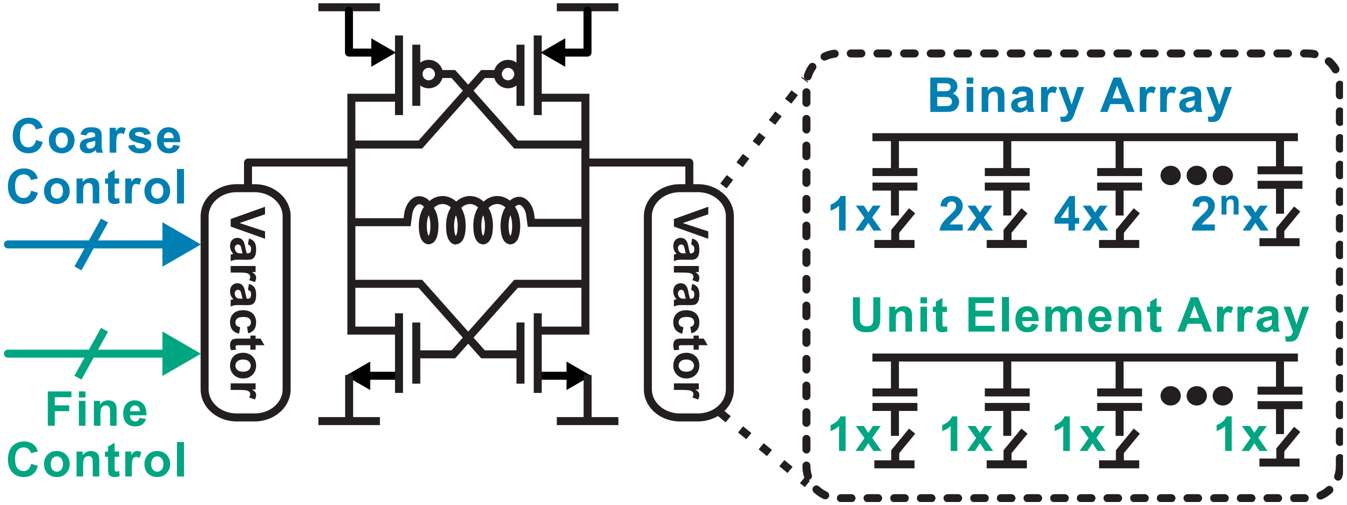
A Much More Digital Implementation



Staszewski et. al., TCAS II, Nov 2003

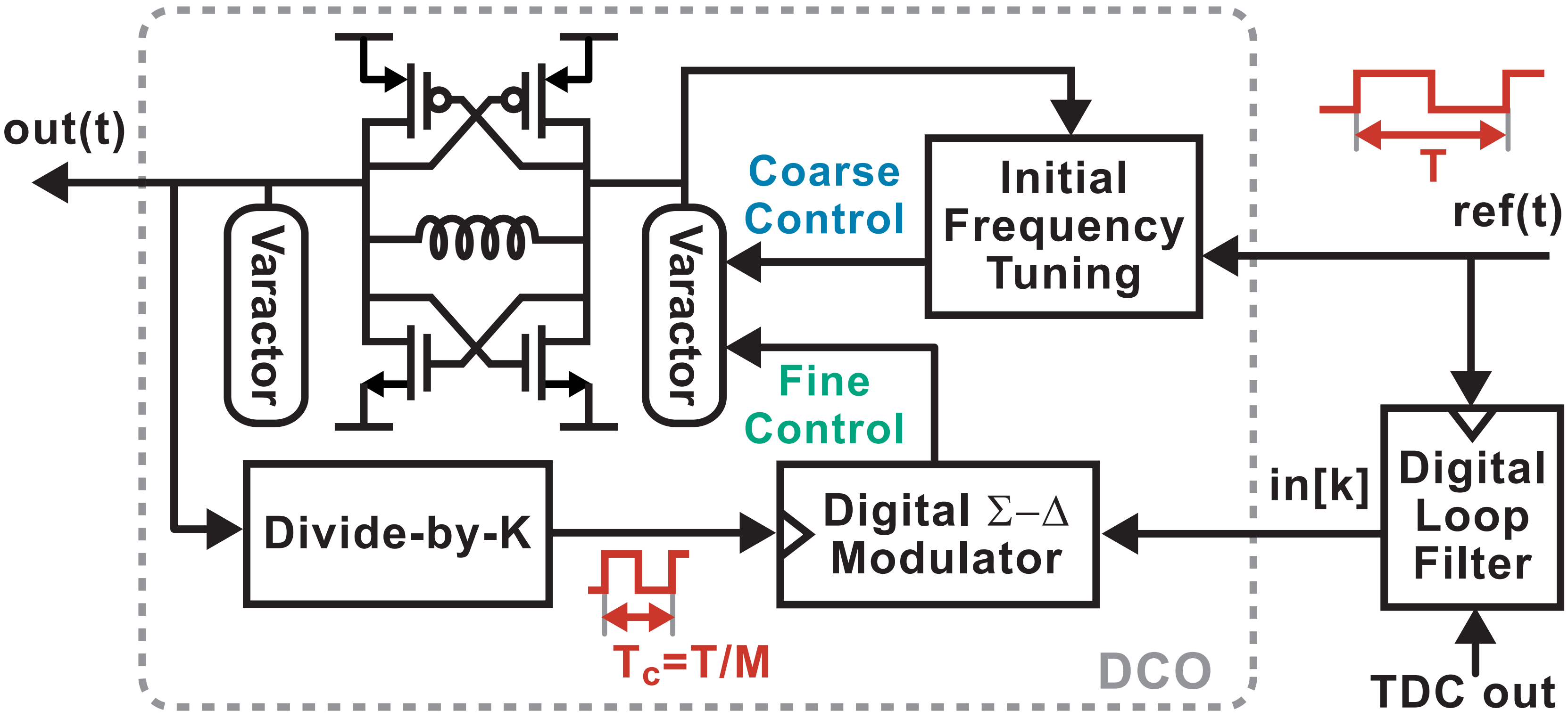
- Adjust frequency in an LC oscillator by switching in a variable number of small capacitors
  - Most effective for CMOS processes of 0.13u and below

Leveraging Segmentation in Switched Capacitor DCO



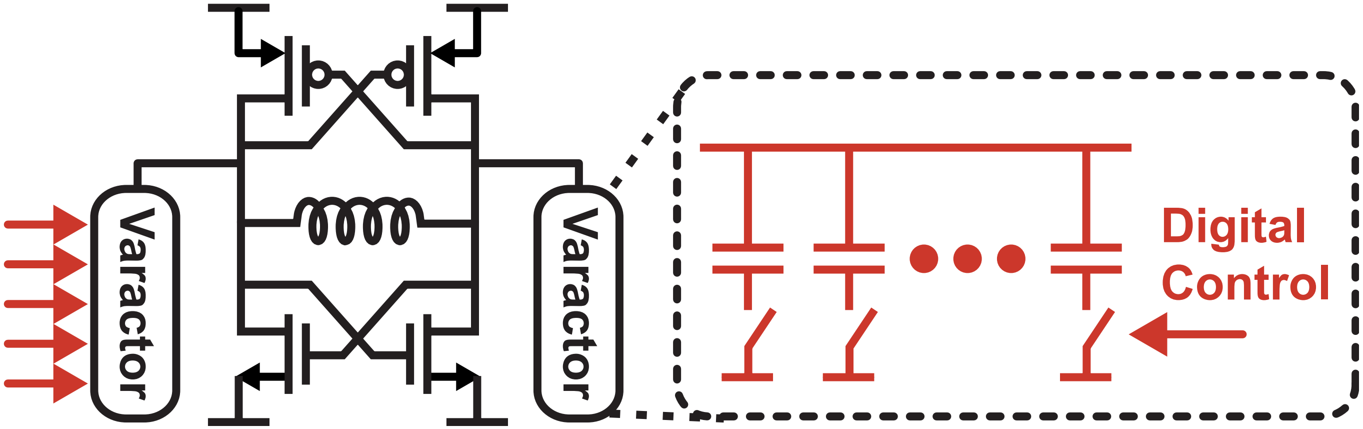
- Similar in design as *segmented* capacitor DAC structures
  - Binary array: efficient control, but may lack monotonicity
  - Unit element array: monotonic, but complex control
- Coarse and fine control segmentation of DCO
  - Coarse control: active only during initial frequency tuning (leverage binary array)
  - Fine control: controlled by PLL feedback (leverage unit element array to guarantee monotonicity)

Leveraging Dithering for Fine Control of DCO

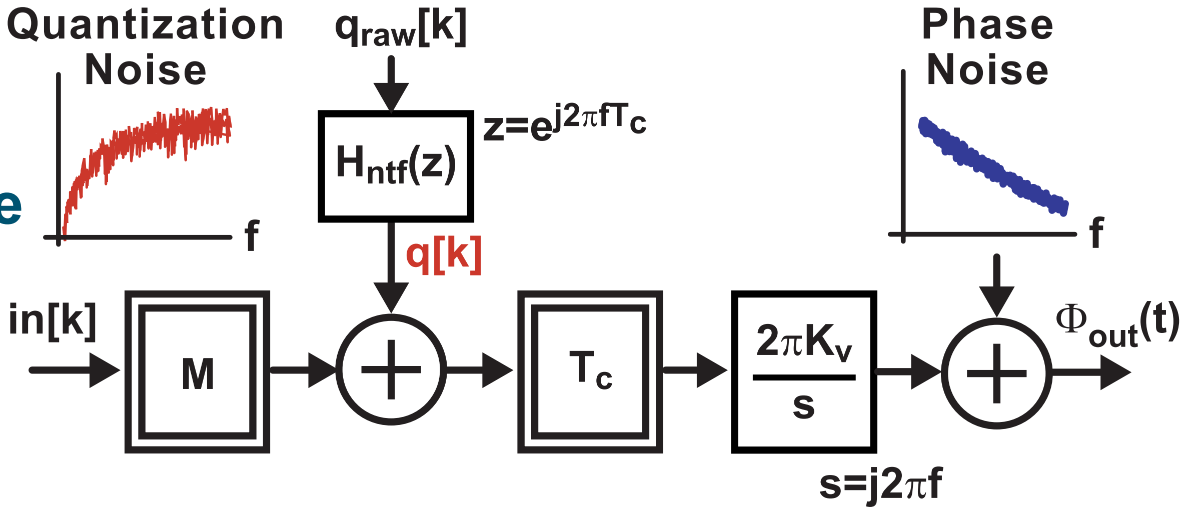


- **Increase resolution by Σ–Δ dithering of fine cap array**
- **Reduce noise from dithering by**
  - **Using small unit caps in the fine cap array**
  - **Increasing the dithering frequency (defined as *$1/T_c$*)**
    - We will assume $1/T_c = M/T$ (i.e. M times reference frequency)

Calculation of Noise Spectrum: Switched Cap DCO

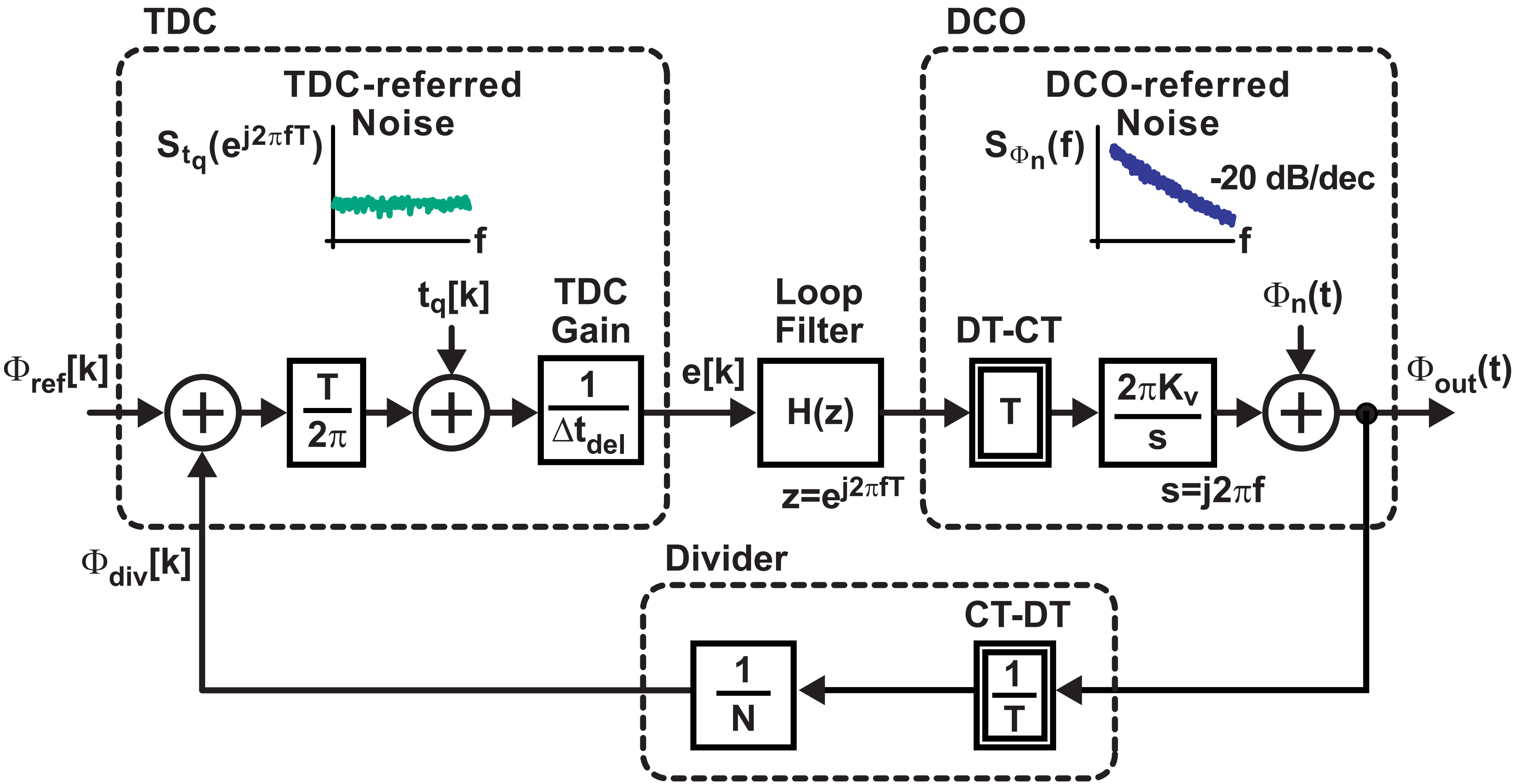


- **Phase noise**
  - **Same as for conventional VCO (tank *Q*, etc.)**
- **Quantization noise from dithering**
  - **See Section 3 of Supplemental Slides**



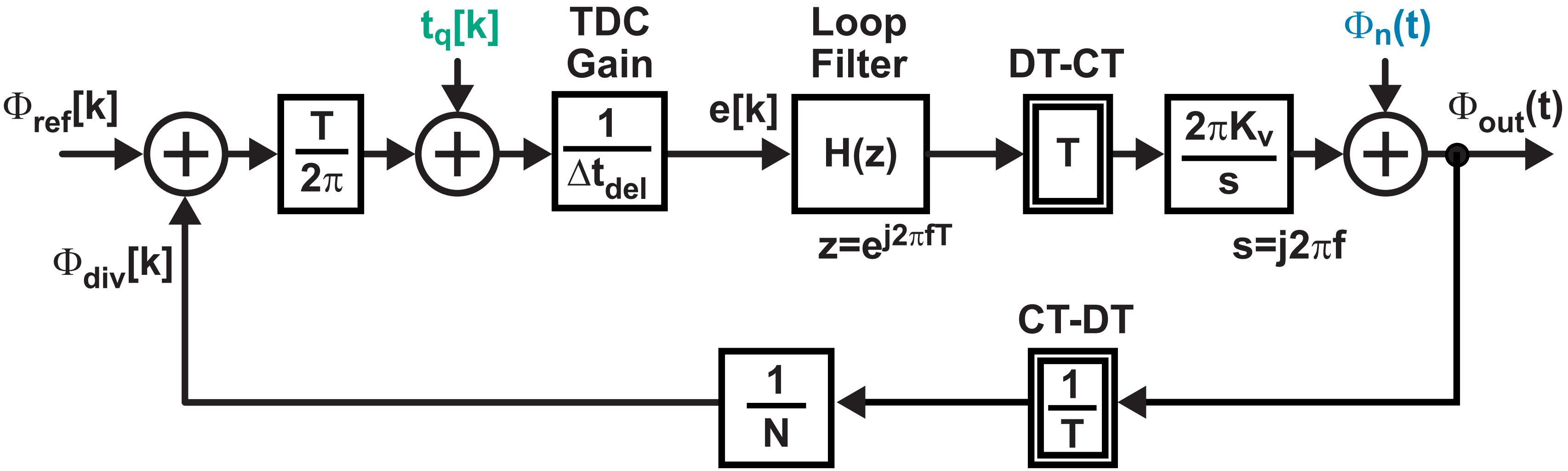
Modeling

Overall Digital PLL Model



- **TDC and DCO-referred noise influence overall phase noise according to associated transfer functions to output**
- **Calculations involve both discrete *and* continuous time**

Key Transfer Functions



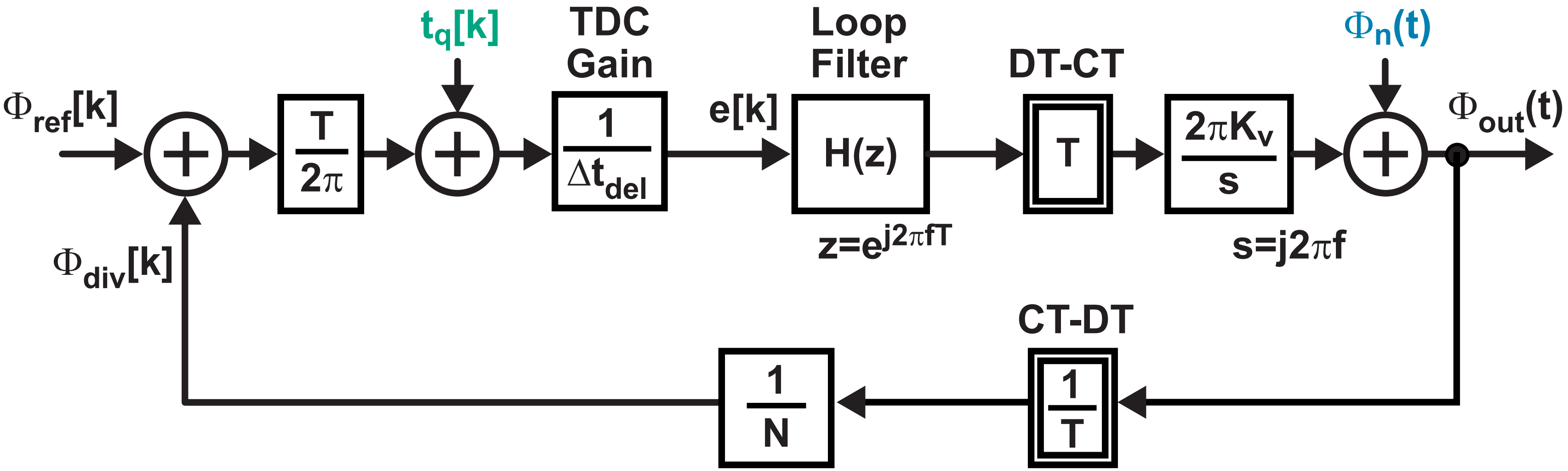
- **TDC-referred noise**

$$\frac{\Phi_{out}}{t_q} = \frac{(1/\Delta t_{del})H(e^{j2\pi fT})T2\pi K_v/(2\pi jf)}{1+(1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

- **DCO-referred noise**

$$\frac{\Phi_{out}}{\Phi_n} = \frac{1}{1+(1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

Introduce a Parameterizing Function



- **Define open loop transfer function *A(f)* as:**

$$A(f) = (1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)$$

- **Define closed loop parameterizing function *G(f)* as:**

$$\boxed{G(f) = \frac{A(f)}{1+A(f)}}$$

  - **Note: *G(f)* is a lowpass filter with DC gain = 1**

Transfer Function Parameterization Calculations

- **TDC-referred noise**

$$\frac{\Phi_{out}}{t_q} = \frac{(1/\Delta t_{del})H(e^{j2\pi fT})T2\pi K_v/(2\pi jf)}{1+(1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

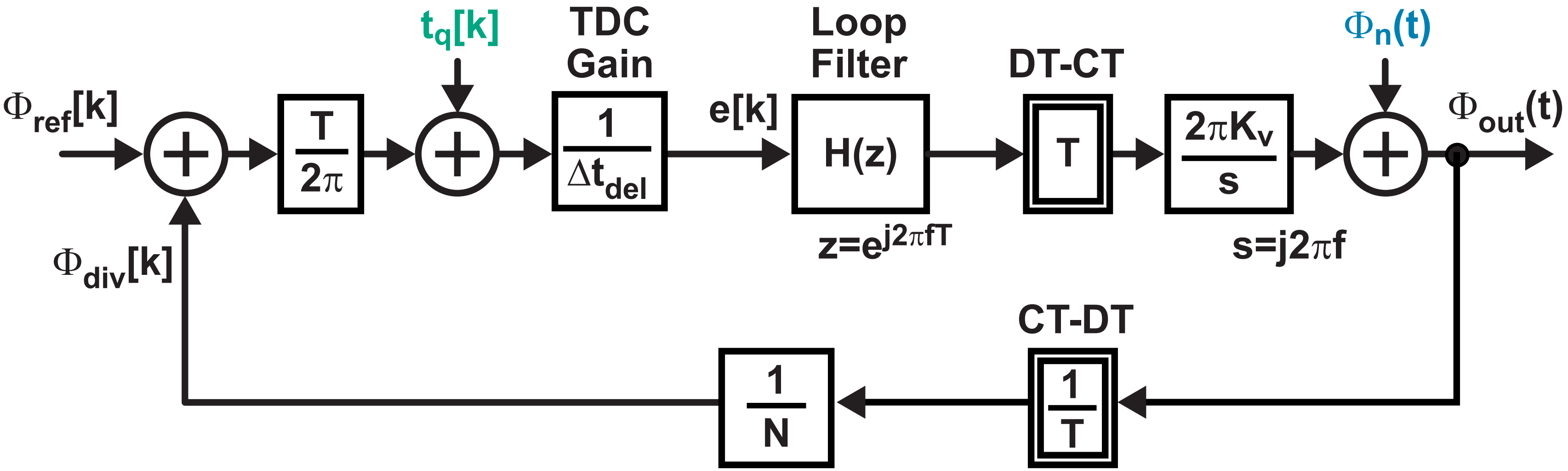
$$= \frac{2\pi NA(f)}{1+A(f)} = \boxed{2\pi NG(f)}$$

- **DCO-referred noise**

$$\frac{\Phi_{out}}{\Phi_n} = \frac{1}{1+(1/\Delta t_{del})H(e^{j2\pi fT})TK_v/(2\pi jf)(1/N)}$$

$$= \frac{1}{1+A(f)} = \frac{1+A(f)-A(f)}{1+A(f)} = \boxed{1-G(f)}$$

Key Observations



- TDC-referred noise

$$\frac{\Phi_{out}}{t_q} = 2\pi N G(f)$$

Lowpass with a DC gain of 2π*N*

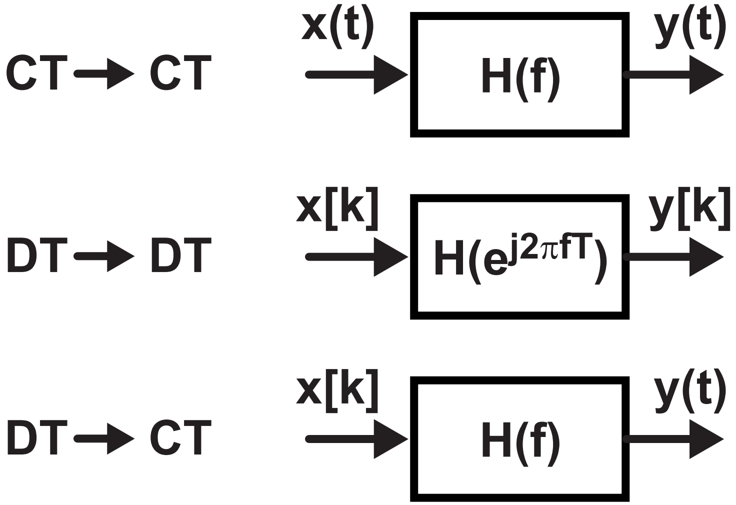
- DCO-referred noise

$$\frac{\Phi_{out}}{\Phi_n} = 1 - G(f)$$

Highpass with a high frequency gain of 1

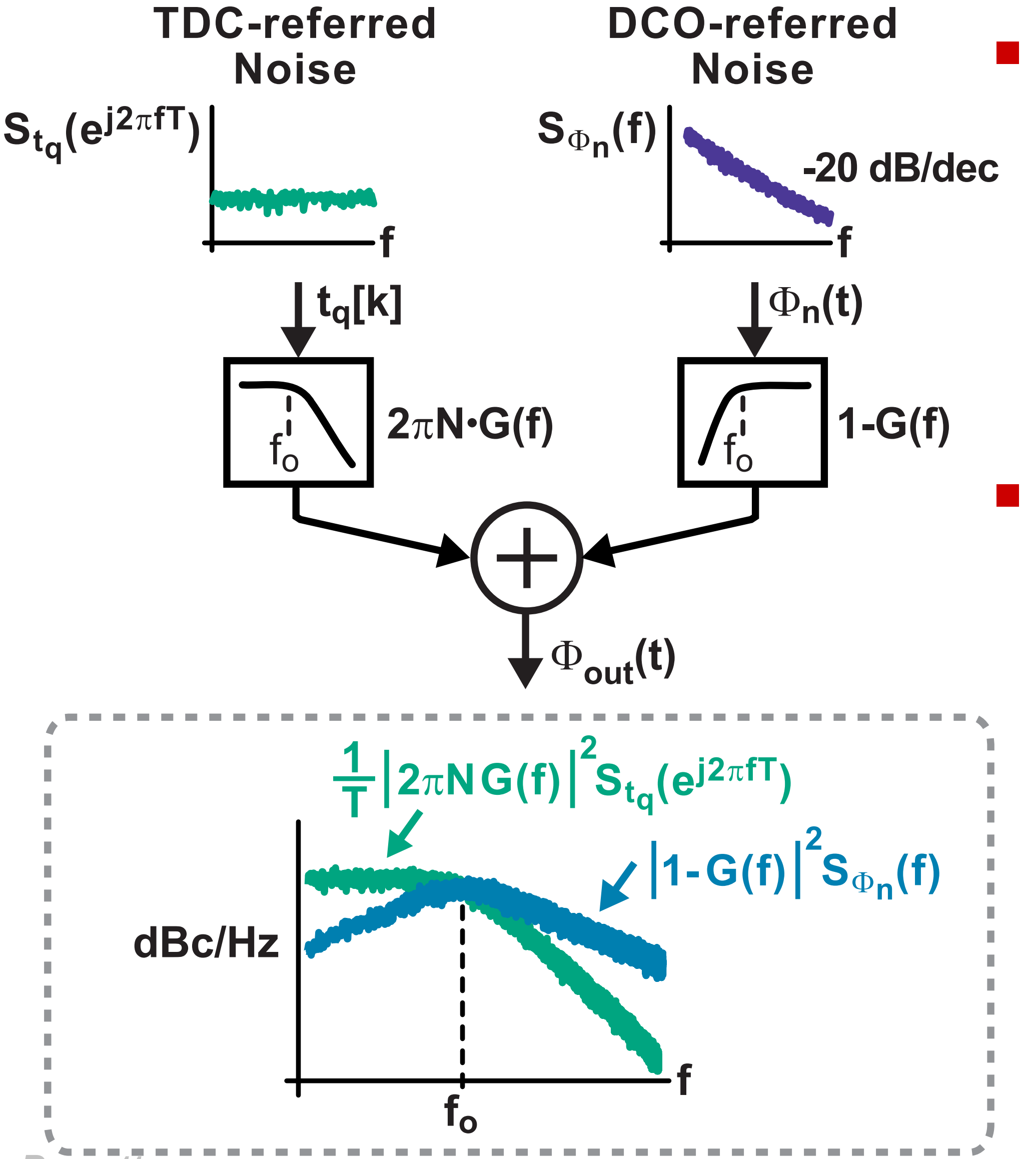
How do we calculate the output phase noise?

Spectral Density Calculations



- CT ➡ CT $$S_y(f) = |H(f)|^2 S_x(f)$$
- DT ➡ DT $$S_y(e^{j2\pi fT}) = |H(e^{j2\pi fT})|^2 S_x(e^{j2\pi fT})$$
- DT ➡ CT $$S_y(f) = \frac{1}{T}|H(f)|^2 S_x(e^{j2\pi fT})$$

Phase Noise Calculation



- TDC noise
  - DT to CT calculation
  - Dominates PLL phase noise at low frequency offsets
- DCO noise
  - CT to CT calculation
  - Dominates PLL phase noise at high frequency offsets

Example Calculation for Delay Chain TDC

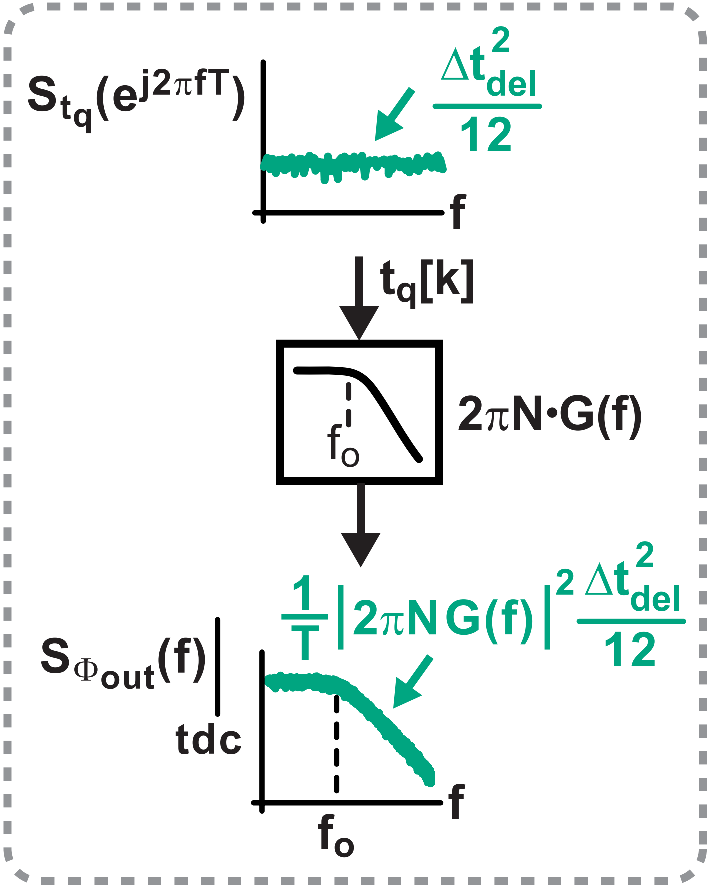
- Ref freq = *1/T* = 50 MHz,
  Out freq = 3.6 GHz

$$\Rightarrow \; N = \frac{3600}{50} = 72$$

- Inverter delay = *Δt_{del}* = 20 ps

$$S_{\Phi_{out}}(f)\Big|_{\text{tdc}} = \frac{1}{T}|2\pi N G(f)|^2 \frac{\Delta t_{del}^2}{12}$$

$$= 3.4\cdot 10^{-10}|G(f)|^2$$



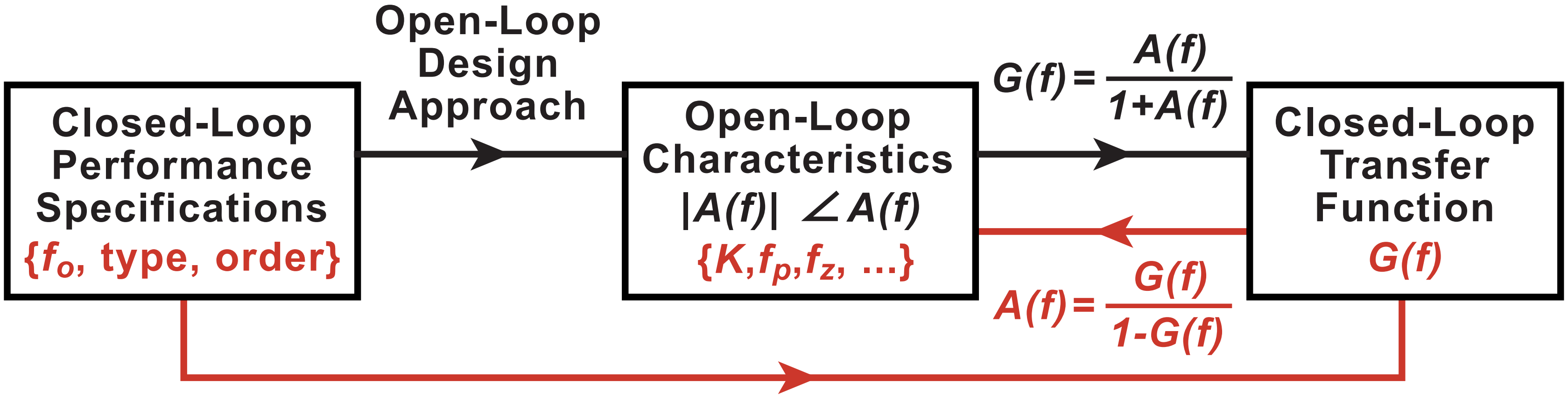
$S_{t_q}(e^{j2\pi fT})$
$\frac{\Delta t_{del}^2}{12}$
f
$t_q[k]$
f_o
$2\pi N\cdot G(f)$
$S_{\Phi out}(f)$
tdc
$\frac{1}{T}|2\pi N G(f)|^2 \frac{\Delta t_{del}^2}{12}$
f
f_o

- Note: *G(f)* = 1 at low offset frequencies

$$\boxed{10\log(3.4\cdot 10^{-10}) = -94.7\ dBc/Hz\ \text{(at low offset freq.)}}$$

CAD Tools

Closed Loop PLL Design Approach


Closed-Loop Performance Specifications
{f_o, type, order}
Open-Loop Design Approach
Open-Loop Characteristics
$|A(f)|$ $\angle A(f)$
$\{K, f_p, f_z, \ldots\}$
$G(f) = \dfrac{A(f)}{1+A(f)}$
$A(f) = \dfrac{G(f)}{1-G(f)}$
Closed-Loop Transfer Function
$G(f)$

Proposed Closed Loop Design Approach

Lau and Perrott, DAC, June 2003

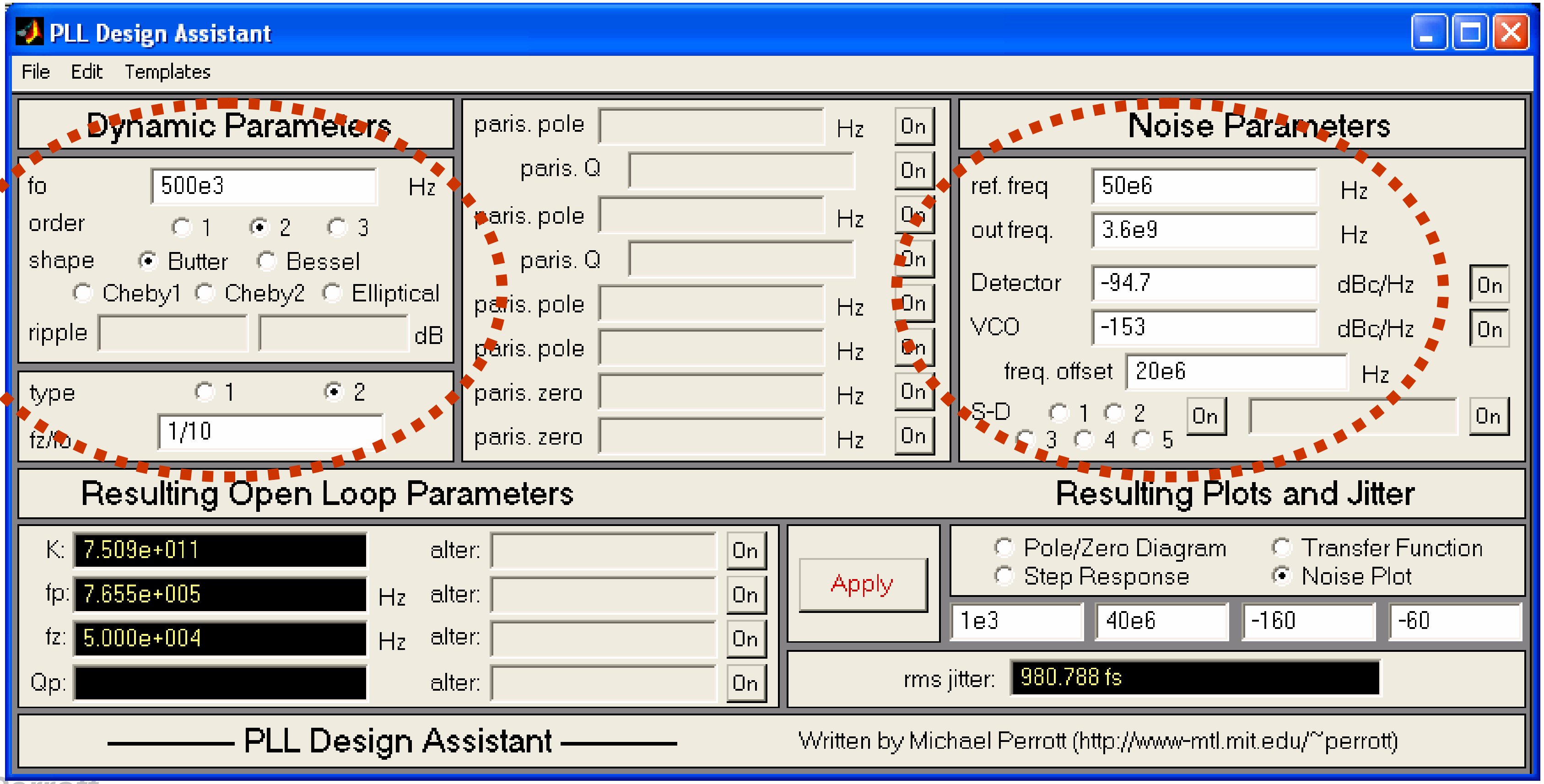
- Classical open loop approach
  - Indirectly design *G(f)* using bode plots of *A(f)*
- Proposed closed loop approach
  - Directly design *G(f)* by examining impact of its specifications on phase noise (and settling time)
  - Solve for *A(f)* that will achieve desired *G(f)*

Implemented in *PLL Design Assistant* Software

http://www.cppsim.com

Evaluate Phase Noise with 500 kHz PLL Bandwidth

- **Key PLL parameters:**
  - ***G(f)*: 500 kHz BW, Type II, 2nd order rolloff**
  - **TDC noise: -94.7 dBc/Hz**
  - **DCO noise: -153 dBc/Hz at 20 MHz offset (3.6 GHz carrier)**



Dynamic Parameters

fo 500e3 Hz

order ○ 1 ● 2 ○ 3

shape ● Butter ○ Bessel

○ Cheby1 ○ Cheby2 ○ Elliptical

ripple dB

type ○ 1 ● 2

fz/fo 1/10

paris. pole Hz On

paris. Q On

paris. pole Hz On

paris. Q On

paris. pole Hz On

paris. pole Hz On

paris. zero Hz On

paris. zero Hz On

Noise Parameters

ref. freq 50e6 Hz

out freq. 3.6e9 Hz

Detector -94.7 dBc/Hz On

VCO -153 dBc/Hz On

freq. offset 20e6 Hz

S-D ○ 1 ○ 2 ○ 3 ○ 4 ○ 5 On On

Resulting Open Loop Parameters

K: 7.509e+011 alter: On

fp: 7.655e+005 Hz alter: On

fz: 5.000e+004 Hz alter: On

Qp: alter: On

Resulting Plots and Jitter

○ Pole/Zero Diagram ○ Transfer Function

○ Step Response ● Noise Plot

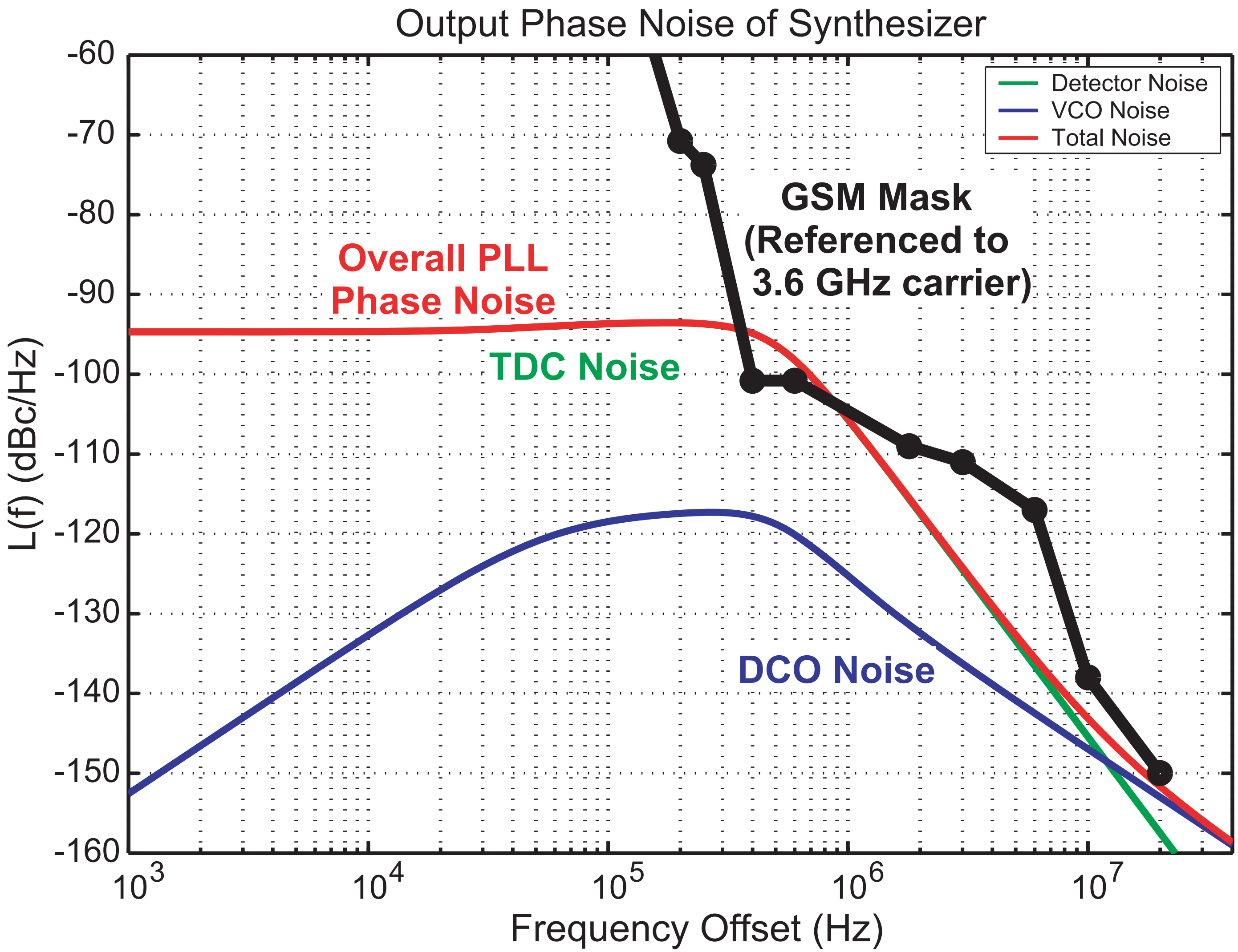
1e3 40e6 -160 -60

rms jitter: 980.788 fs

PLL Design Assistant

Written by Michael Perrott (http://www-mtl.mit.edu/~perrott)

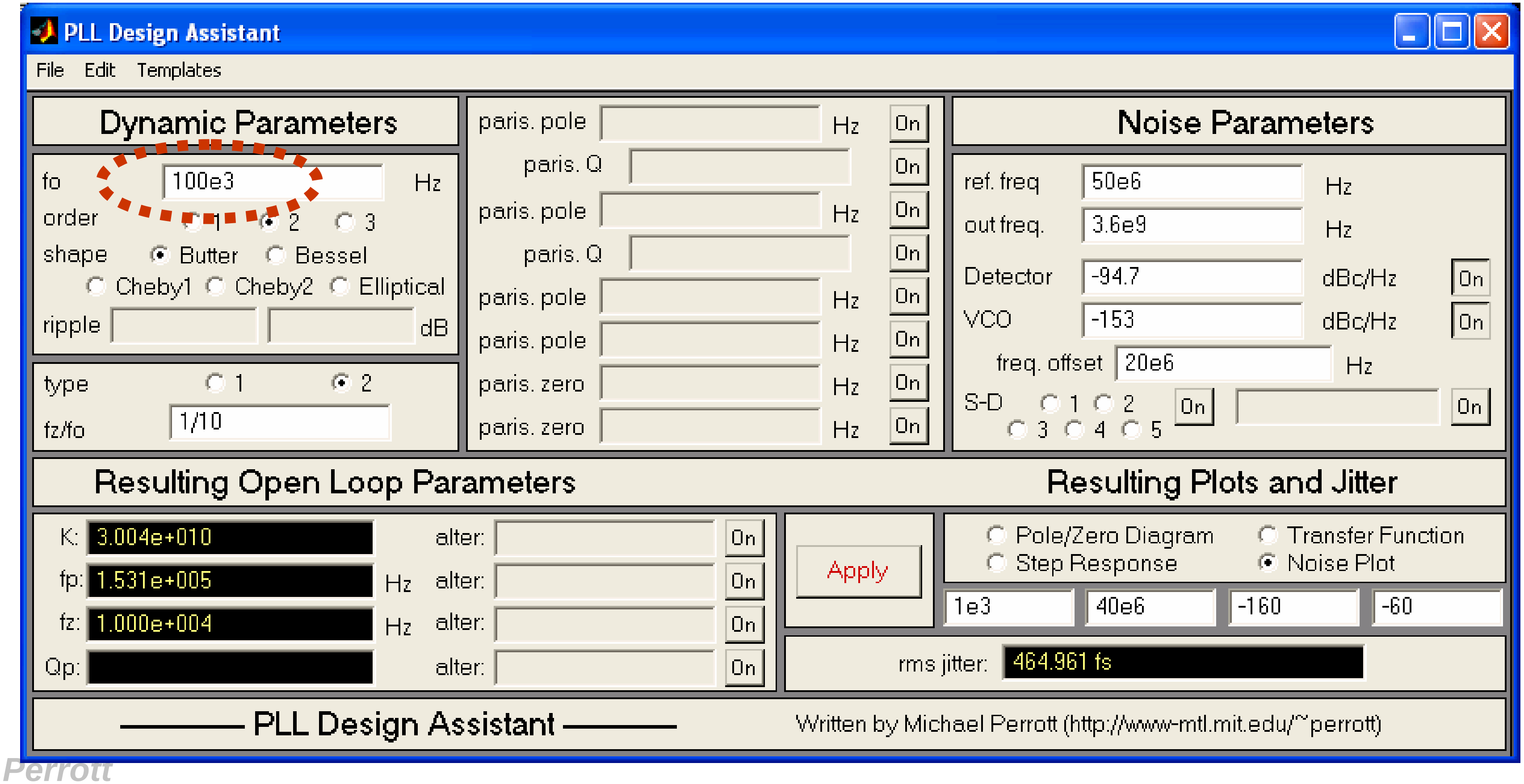
Calculated Phase Noise Spectrum with 500 kHz BW



TDC noise too high for GSM mask with 500 kHz PLL bandwidth

Change PLL Bandwidth to 100 kHz

- **Key PLL parameters:**
  - **G(f): 100 kHz BW, *Type* = 2, *2nd* order rolloff**
  - **TDC noise: -94.7 dBc/Hz**
  - **DCO noise: -153 dBc/Hz at 20 MHz offset (3.6 GHz carrier)**



PLL Design Assistant

Dynamic Parameters

fo: 100e3 Hz

order: ○ 1 ● 2 ○ 3

shape: ● Butter ○ Bessel ○ Cheby1 ○ Cheby2 ○ Elliptical

ripple: dB

type: ○ 1 ● 2

fz/fo: 1/10

paris. pole Hz
paris. Q
paris. pole Hz
paris. Q
paris. pole Hz
paris. pole Hz
paris. zero Hz
paris. zero Hz

Noise Parameters

ref. freq: 50e6 Hz

out freq.: 3.6e9 Hz

Detector: -94.7 dBc/Hz

VCO: -153 dBc/Hz

freq. offset: 20e6 Hz

S-D: ○ 1 ○ 2 ○ 3 ○ 4 ○ 5

Resulting Open Loop Parameters

K: 3.004e+010

fp: 1.531e+005 Hz

fz: 1.000e+004 Hz

Qp:

alter:
alter:
alter:
alter:

Resulting Plots and Jitter

○ Pole/Zero Diagram ○ Transfer Function
○ Step Response ● Noise Plot

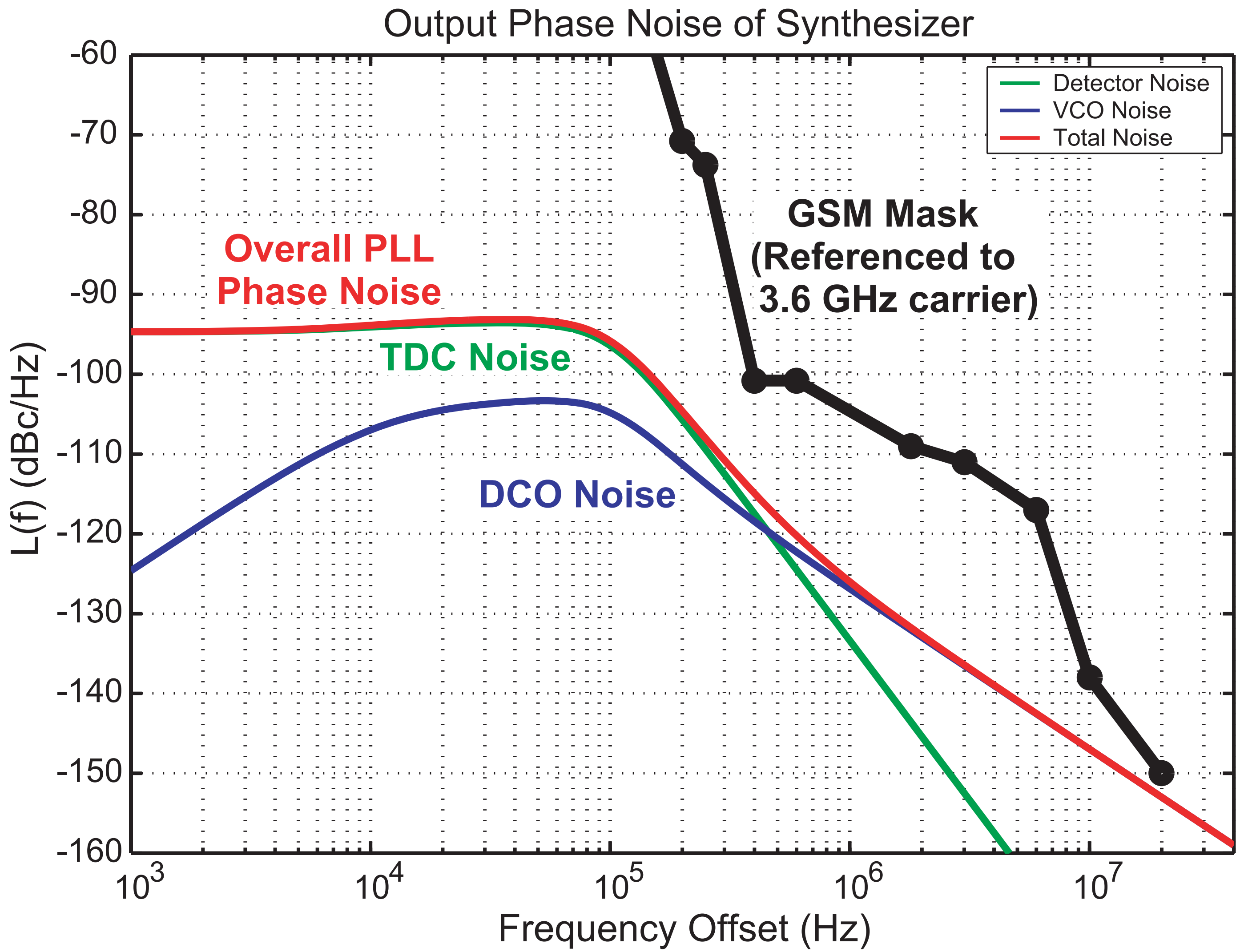
1e3 | 40e6 | -160 | -60

rms jitter: 464.961 fs

—— PLL Design Assistant ——

Written by Michael Perrott (http://www-mtl.mit.edu/~perrott)

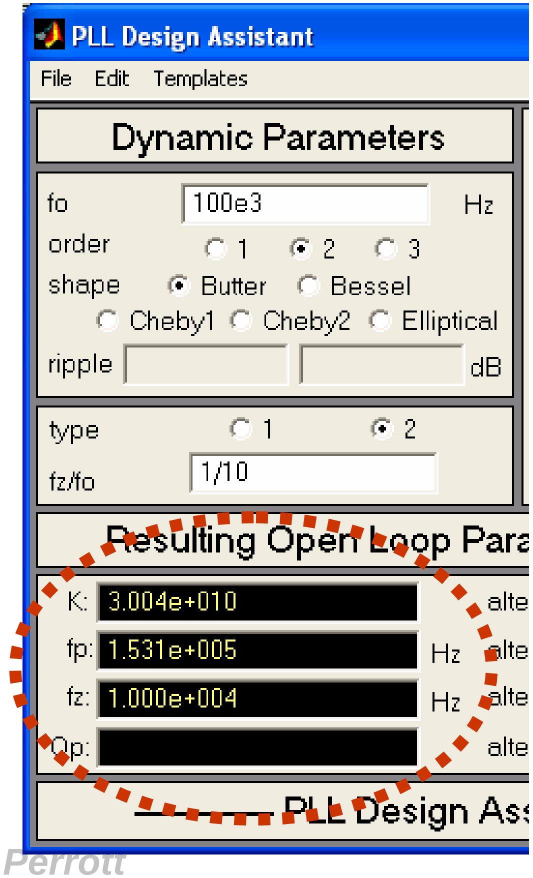
Calculated Phase Noise Spectrum with 100 kHz BW



GSM mask is met with 100 kHz PLL bandwidth

Loop Filter Design using PLL Design Assistant

- **PLL Design Assistant allows fast loop filter design**
  - **See Section 4 of Supplemental Slides**
    - Assumption: *Type* = 2, *2*nd order rolloff



Dynamic Parameters

fo 100e3 Hz

order ○ 1 ● 2 ○ 3

shape ● Butter ○ Bessel ○ Cheby1 ○ Cheby2 ○ Elliptical

ripple dB

type ○ 1 ● 2

fz/fo 1/10

Resulting Open Loop Para

K: 3.004e+010 alte

fp: 1.531e+005 Hz alte

fz: 1.000e+004 Hz alte

Qp: alte

PLL Design Ass

$$H(z) = K_{LF}\left(\frac{1}{1-z^{-1}}\right)\frac{1-b_1z^{-1}}{1-a_1z^{-1}}$$

- **Where:**

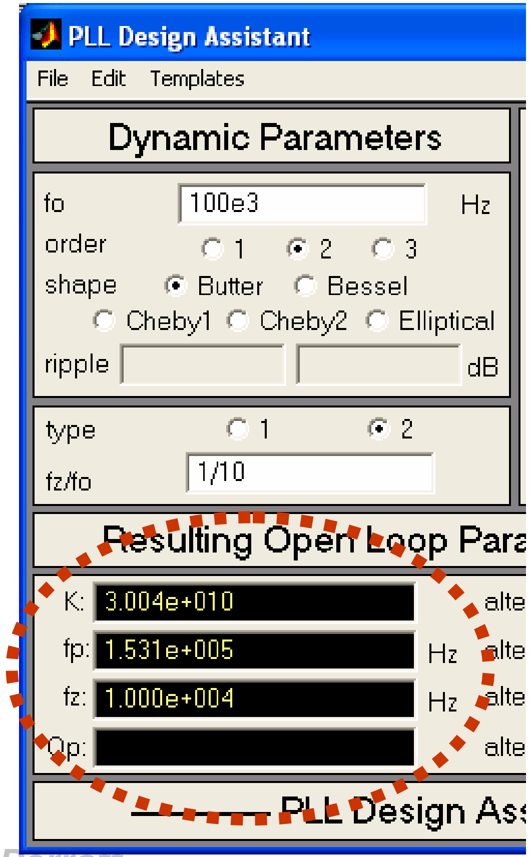
$$a_1 = \frac{1}{1+w_pT} \qquad b_1 = \frac{1}{1+w_zT}$$

$$K_{LF} = \left(\frac{\Delta t_{del}}{T/N}\right)\frac{K}{K_v}\left(\frac{w_p}{w_z}\right)\frac{a_1}{b_1}T$$

- **PLL Design Assistant provides the values of *K*, *w*$_p$ = 2πf$_p$, *w*$_z$ = 2πf$_z$**

Example Digital Loop Filter Calculation

- **Assumptions**
  - **Ref freq (*1/T*) = 50 MHz, Out freq = 3.6 GHz (so *N* = 72)**
  - **Δt_{del} = 20 ps, K_v = 12 kHz/unit cap**
  - **100 kHz bandwidth, *Type* = 2 , *2nd* order rolloff**



Dynamic Parameters

fo 100e3 Hz

order ○ 1 ● 2 ○ 3

shape ● Butter ○ Bessel ○ Cheby1 ○ Cheby2 ○ Elliptical

ripple dB

type ○ 1 ● 2

fz/fo 1/10

Resulting Open Loop Para

K: 3.004e+010 alte

fp: 1.531e+005 Hz alte

fz: 1.000e+004 Hz alte

Qp: alte

PLL Design Ass

$$H(z) = K_{LF}\left(\frac{1}{1-z^{-1}}\right)\frac{1-b_1z^{-1}}{1-a_1z^{-1}}$$

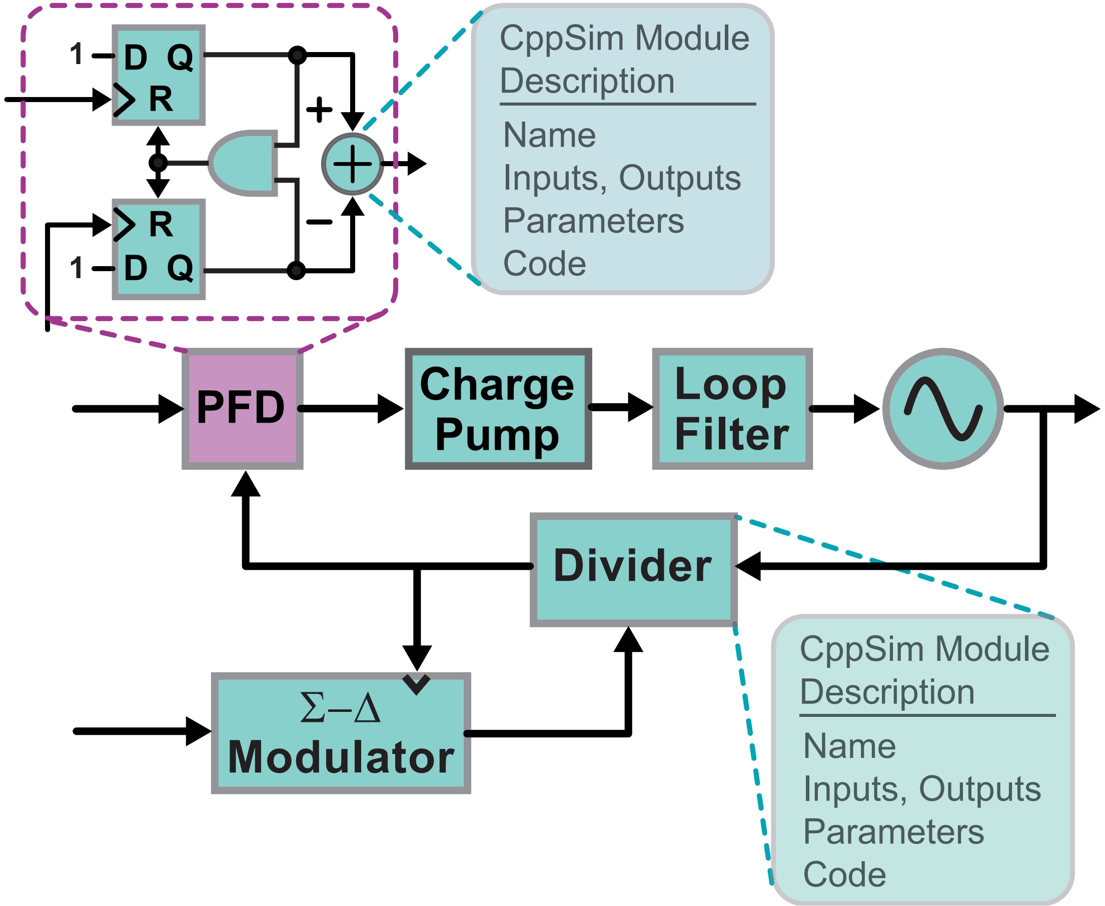
$$b_1 = \frac{1}{1+2\pi 10\text{kHz}/50\text{MHz}} = \boxed{.9987}$$

$$a_1 = \frac{1}{1+2\pi 153\text{kHz}/50\text{MHz}} = \boxed{.9811}$$

$$K_{LF} = \left(\frac{\Delta t_{del}}{T/N}\right)\frac{3\cdot 10^{10}}{12\text{kHz}}\,\frac{153}{10}\,\frac{.9811}{.9987}\,\frac{1}{50\text{MHz}}$$

$$= \left(\frac{\Delta t_{del}}{T/N}\right)0.75 = \boxed{\left(\frac{\Delta t_{del}}{T_{dco}}\right)0.75}$$

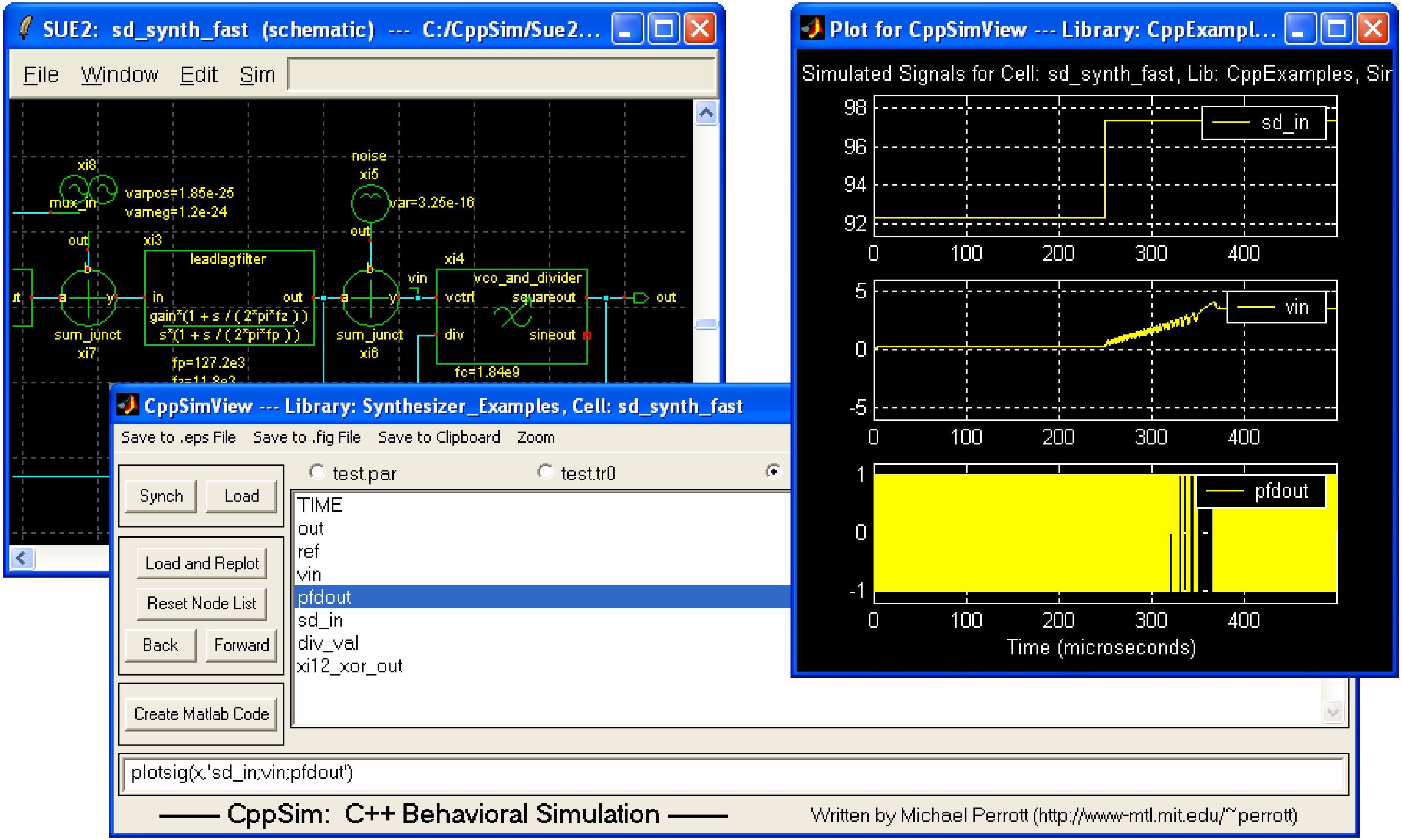
Verify Calculations Using C++ Behavioral Modeling



- Schematic
  - Hierarchical description of *system topology*
- Code blocks
  - Specification of *module behavior* using templated C++ code

- Behavioral environment allows efficient architectural investigation and validation of calculations
  - Fast simulation speed is essential for design investigation

CppSim – A Fast C++ Behavioral Simulator



```
plotsig(x,'sd_in;vin;pfdout')
```

—— CppSim: C++ Behavioral Simulation ——

Written by Michael Perrott (http://www-mtl.mit.edu/~perrott)

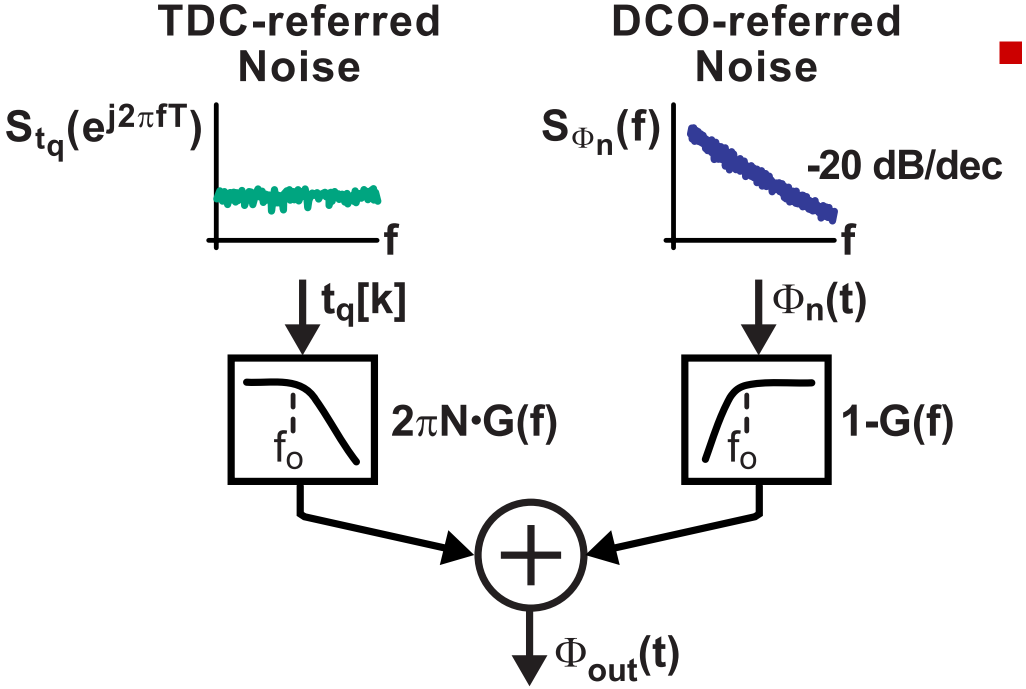
http://www.cppsim.com

How Do We Improve TDC Performance?

Two Key Issues:

- **TDC resolution**
- **Mismatch**

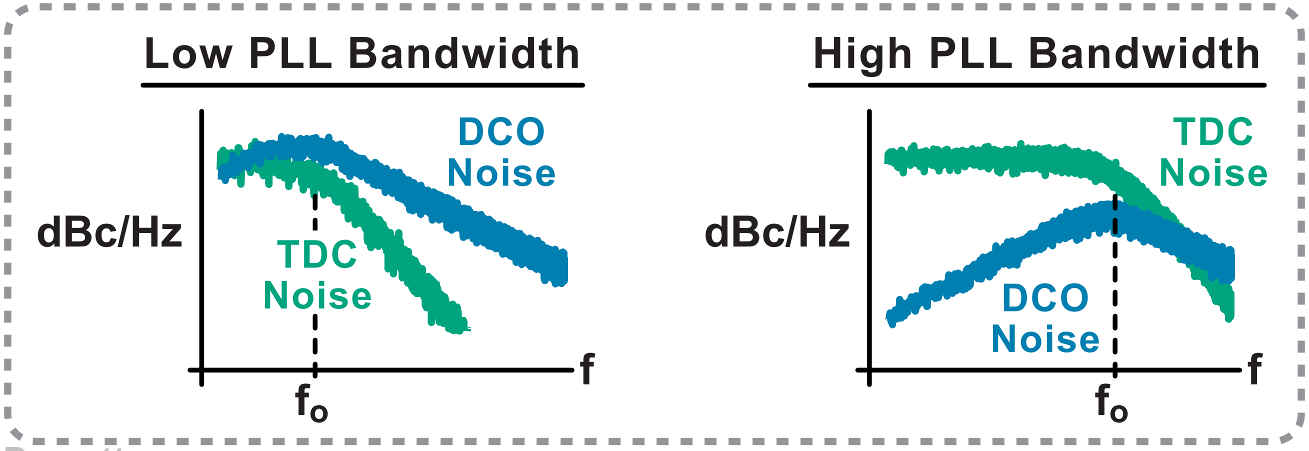
Motivation



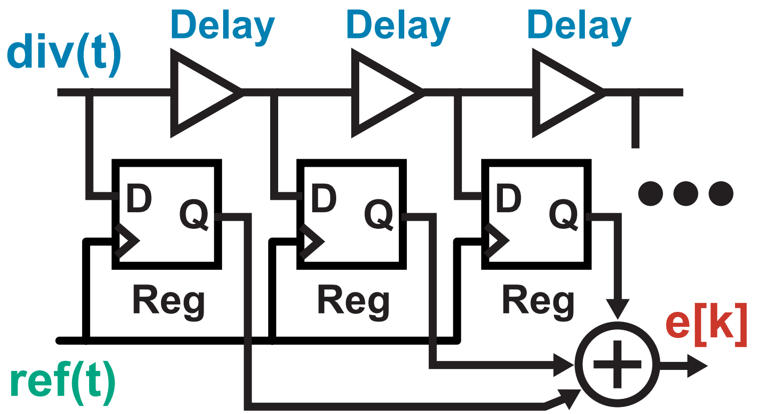
- PLL bandwidth dramatically influences relative impact of TDC and VCO noise

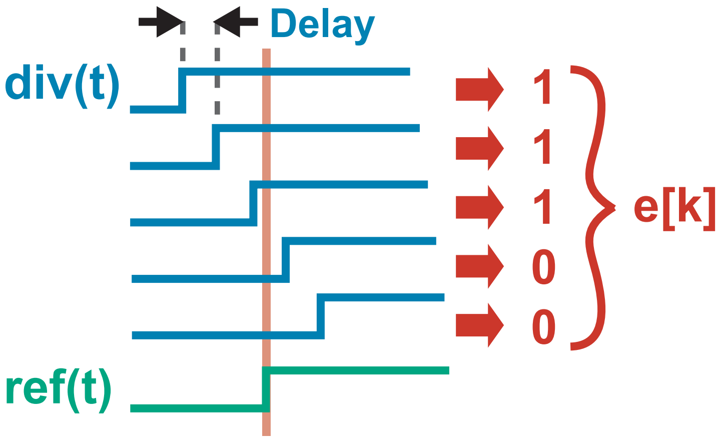
Want high PLL bandwidth?

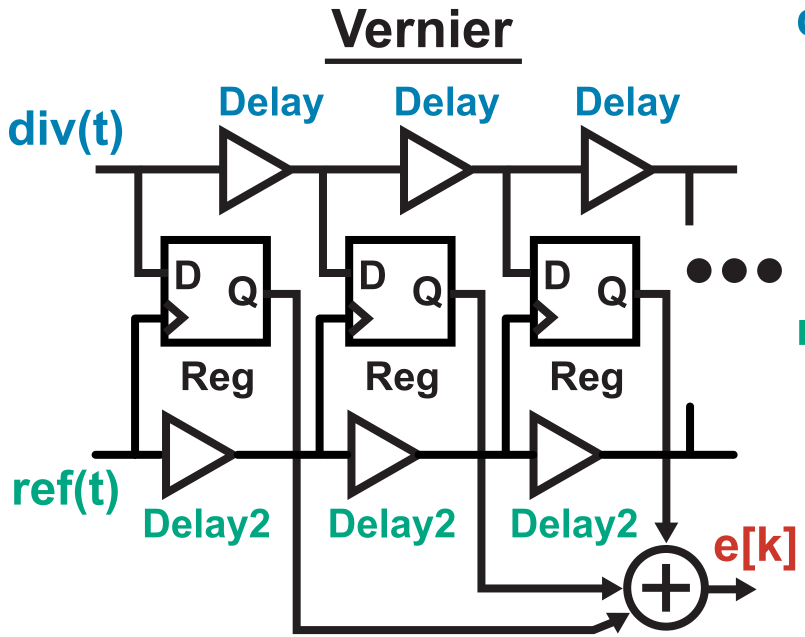
➡ Need low TDC Noise

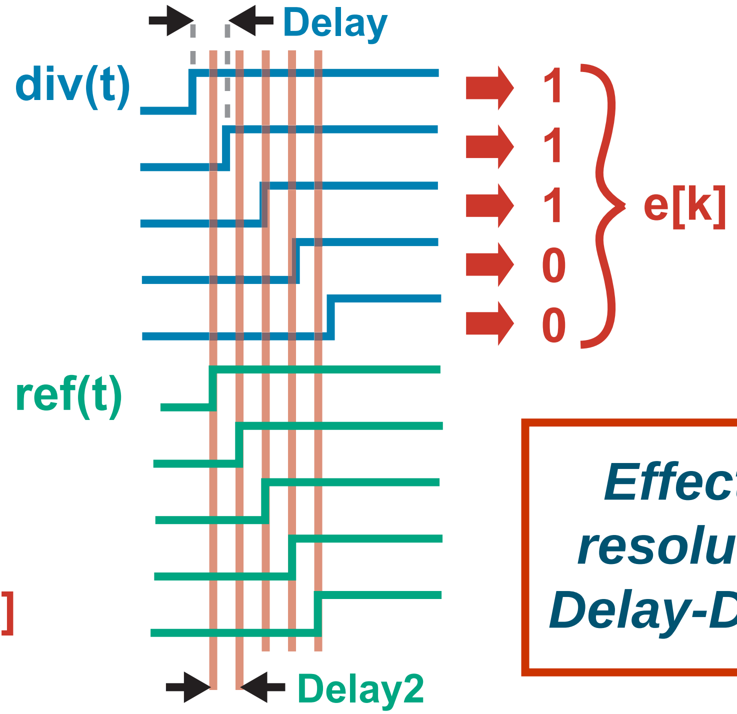


Improve Resolution with Vernier Delay Technique





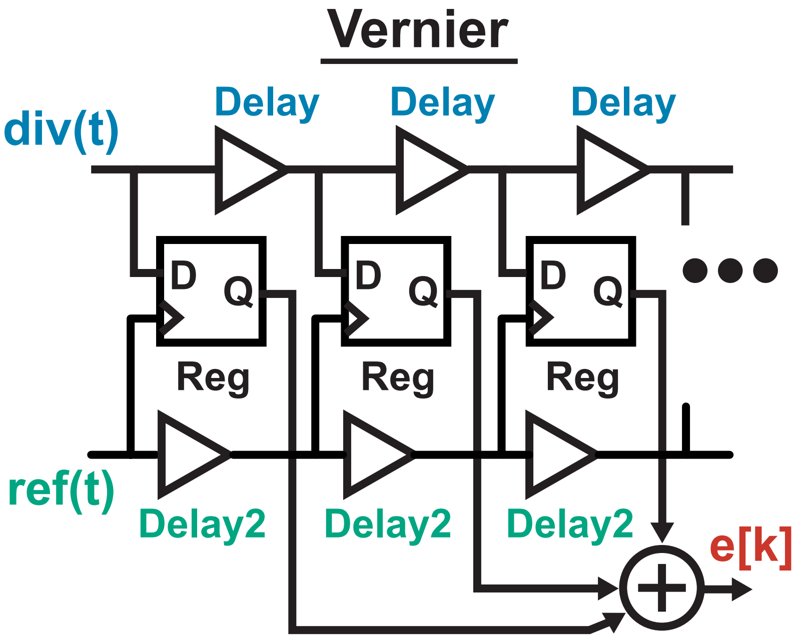


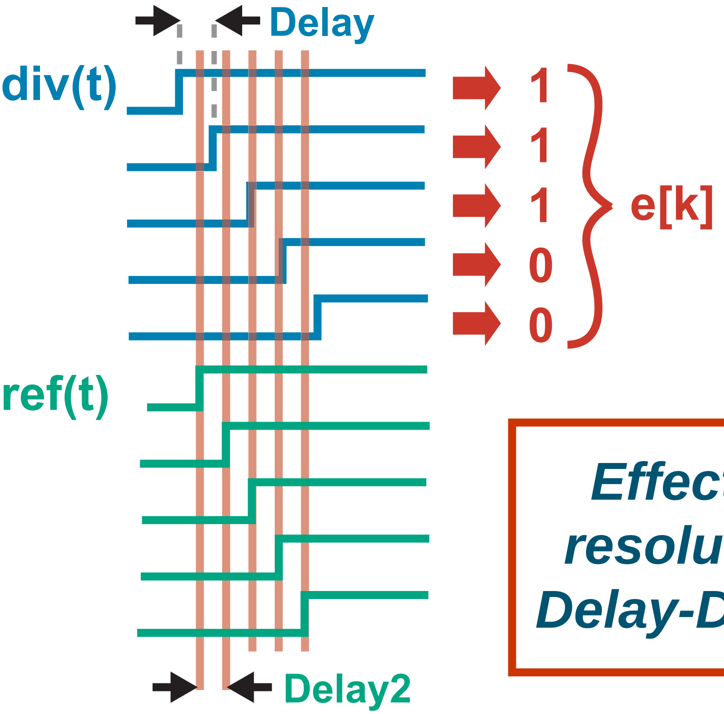


Effective resolution: Delay-Delay2

Issues with Vernier Approach

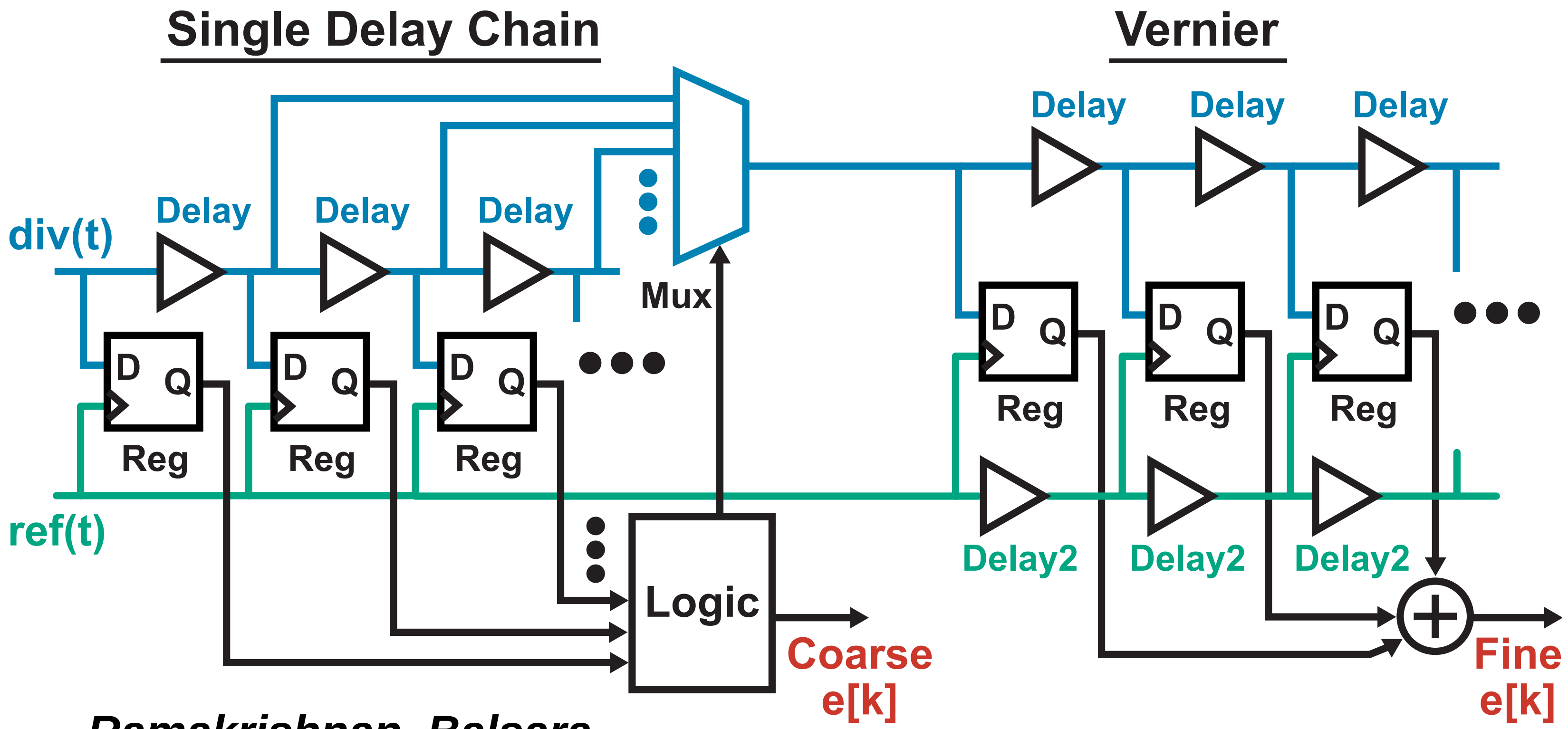
- Mismatch issues are more severe than the single delay chain TDC
  - Reduced delay is formed as *difference* of two delays
- Large measurement range requires large area
  - Initial PLL frequency acquisition may require a large range



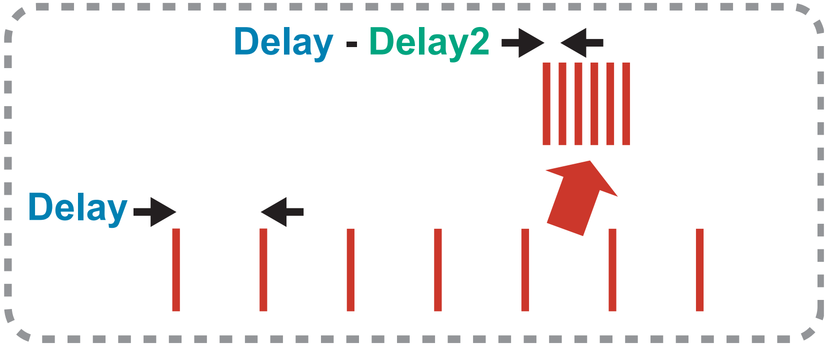


Effective resolution: Delay-Delay2

Two-Step TDC Architecture Allows Area Reduction

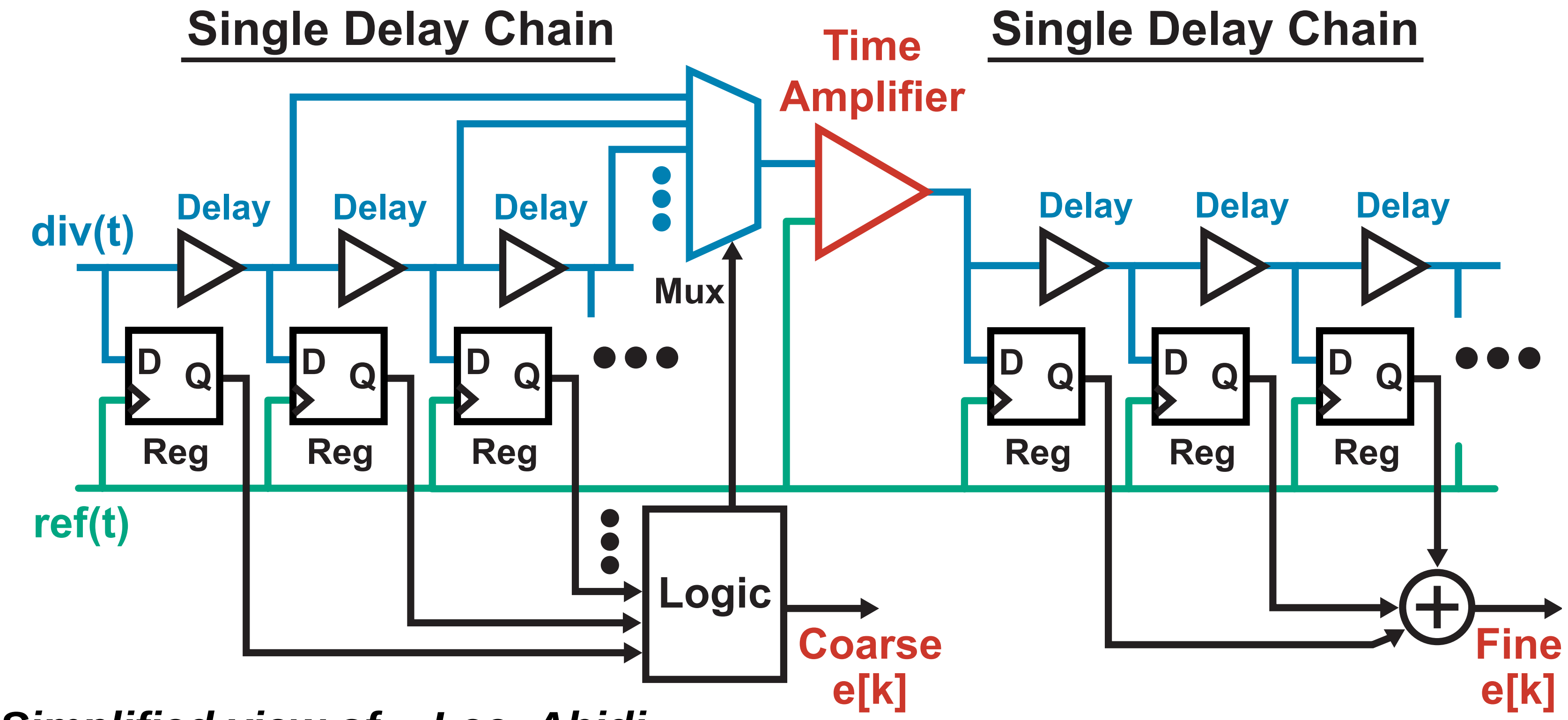


Ramakrishnan, Balsara
VLSID '06

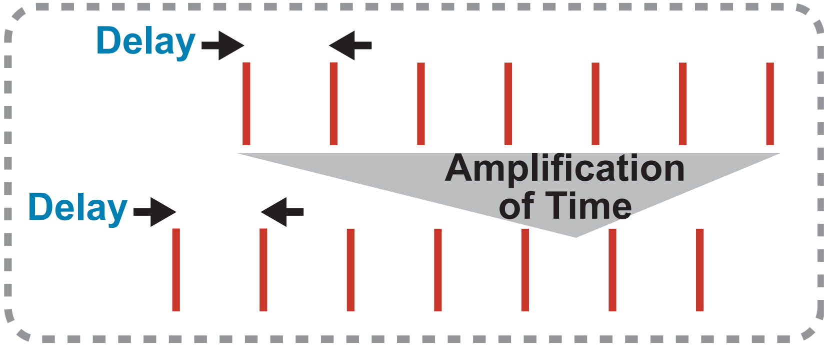


- Single delay chain provides coarse resolution
- (Folded) Vernier provides fine resolution

Two-Step TDC Using Time Amplification

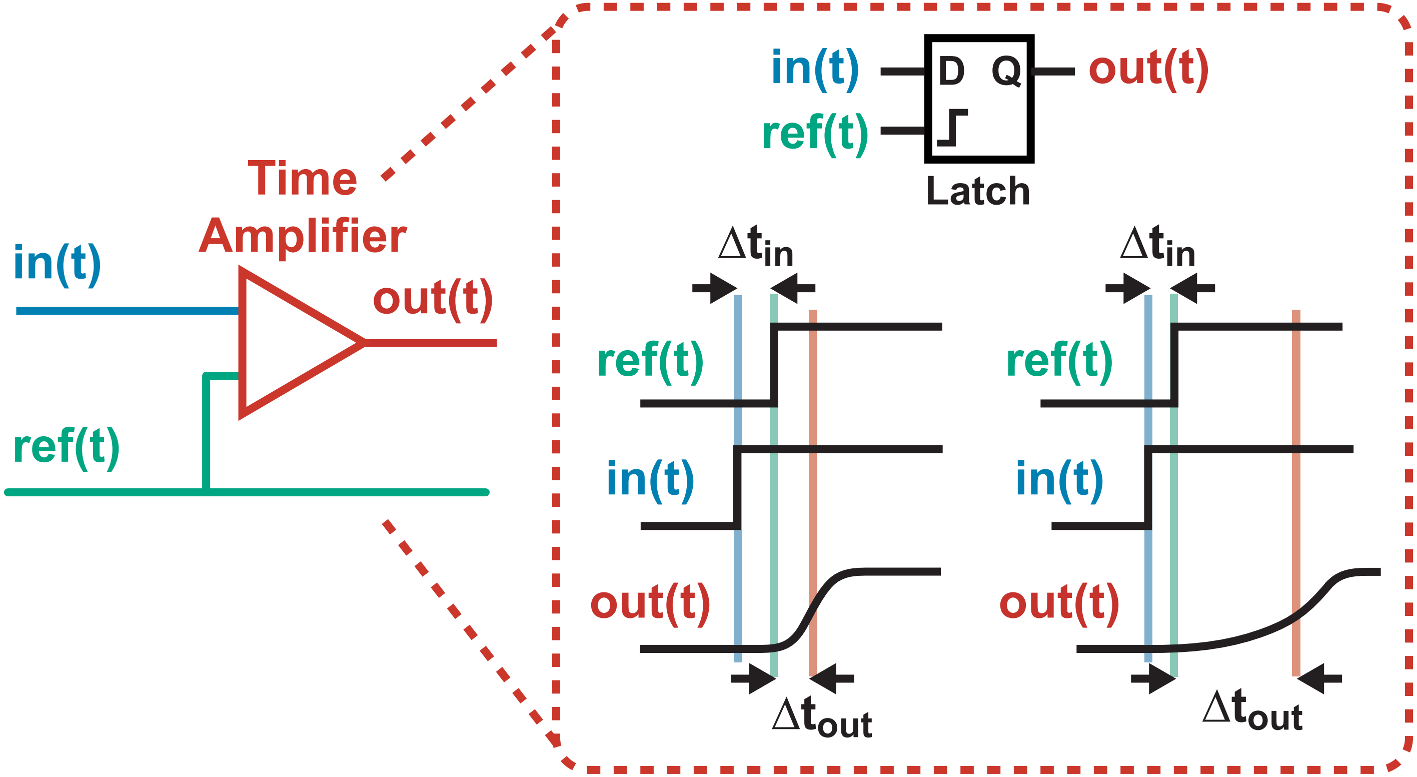


Simplified view of: Lee, Abidi VLSI 2007



- Single delay chain provides coarse and fine resolution
- Time amplification is used to improve resolution

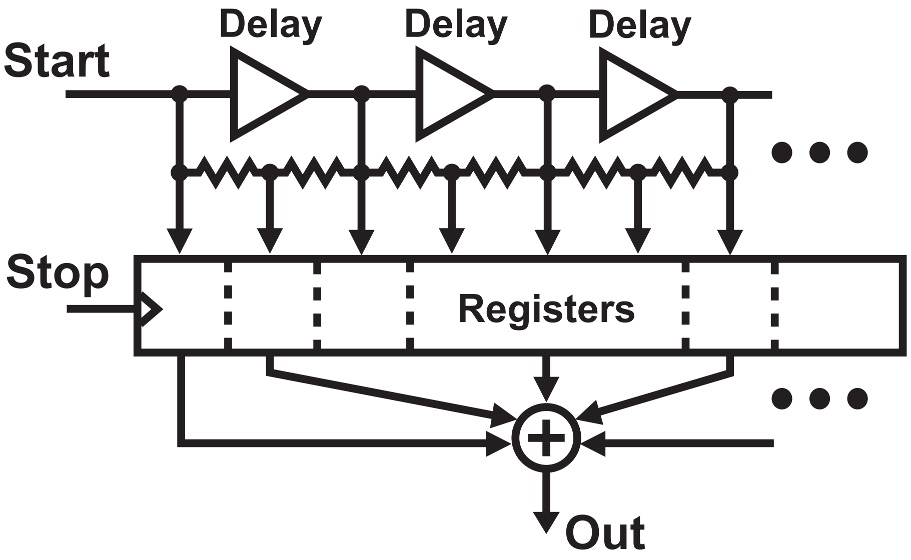
Leveraging Metastability to Create a Time Amplifier



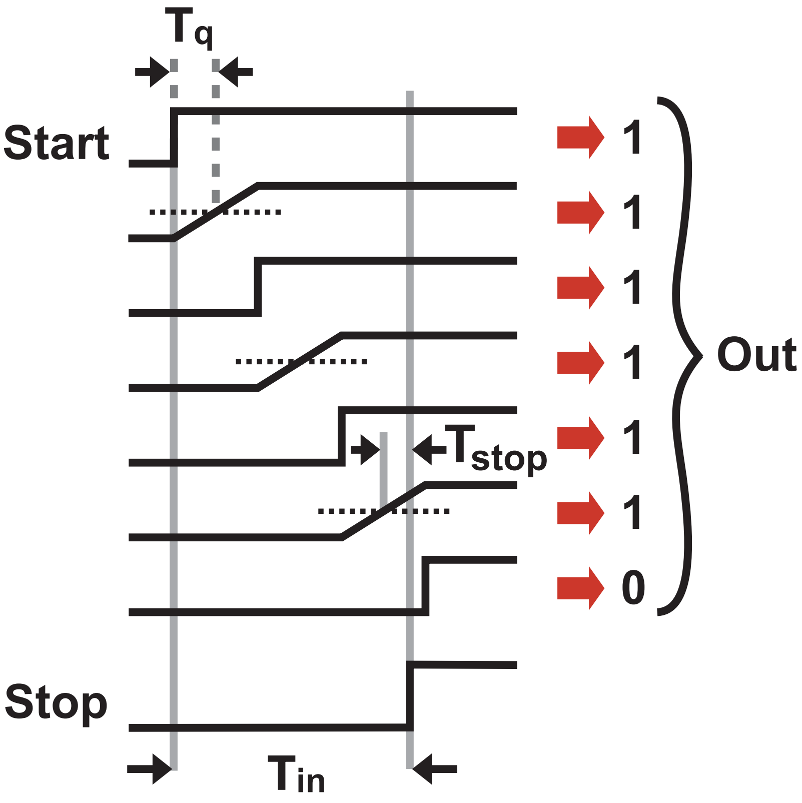
Simplified view of: Abas, et al., Electronic Letters, Nov 2002 (note that actual implementation uses SR latch)

- **Metastability leads to progressively slower output transitions as setup time on latch is encroached upon**
  - **Time difference at input is amplified at output**

Interpolating time-to-digital converter

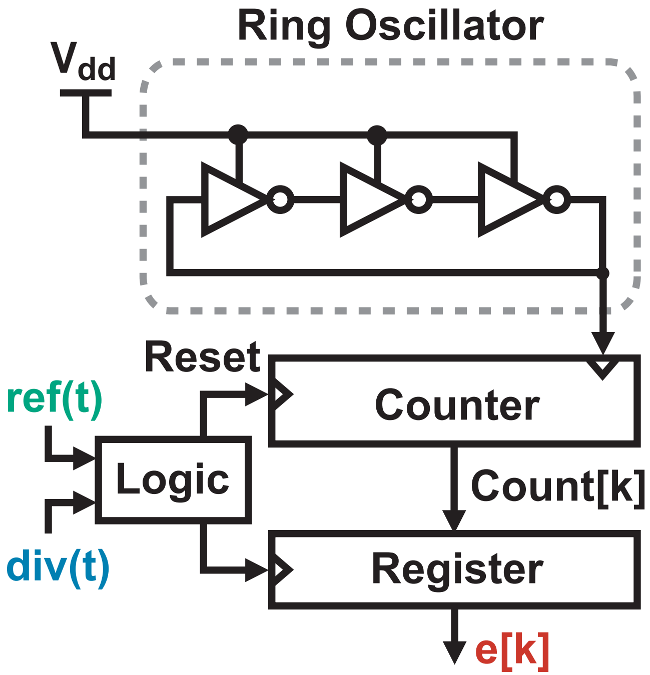


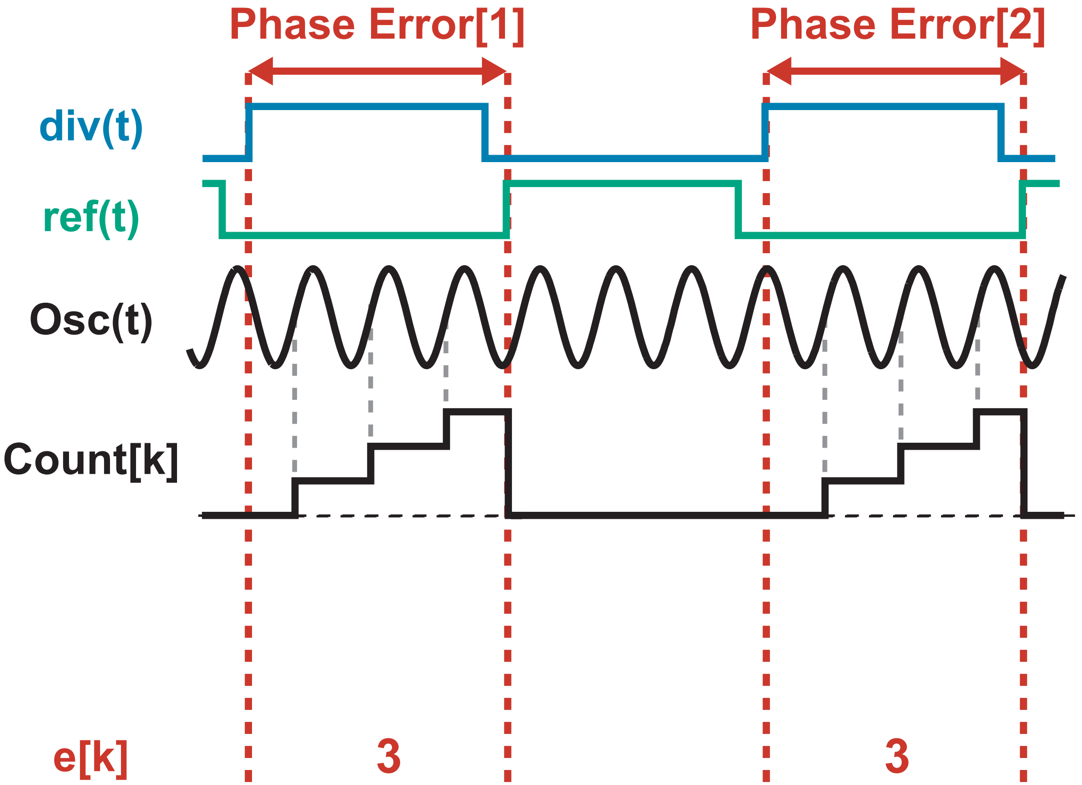
Henzler et al., ISSCC 2008



- Interpolate between edges to achieve fine resolution
- Cyclic approach can also be used for large range

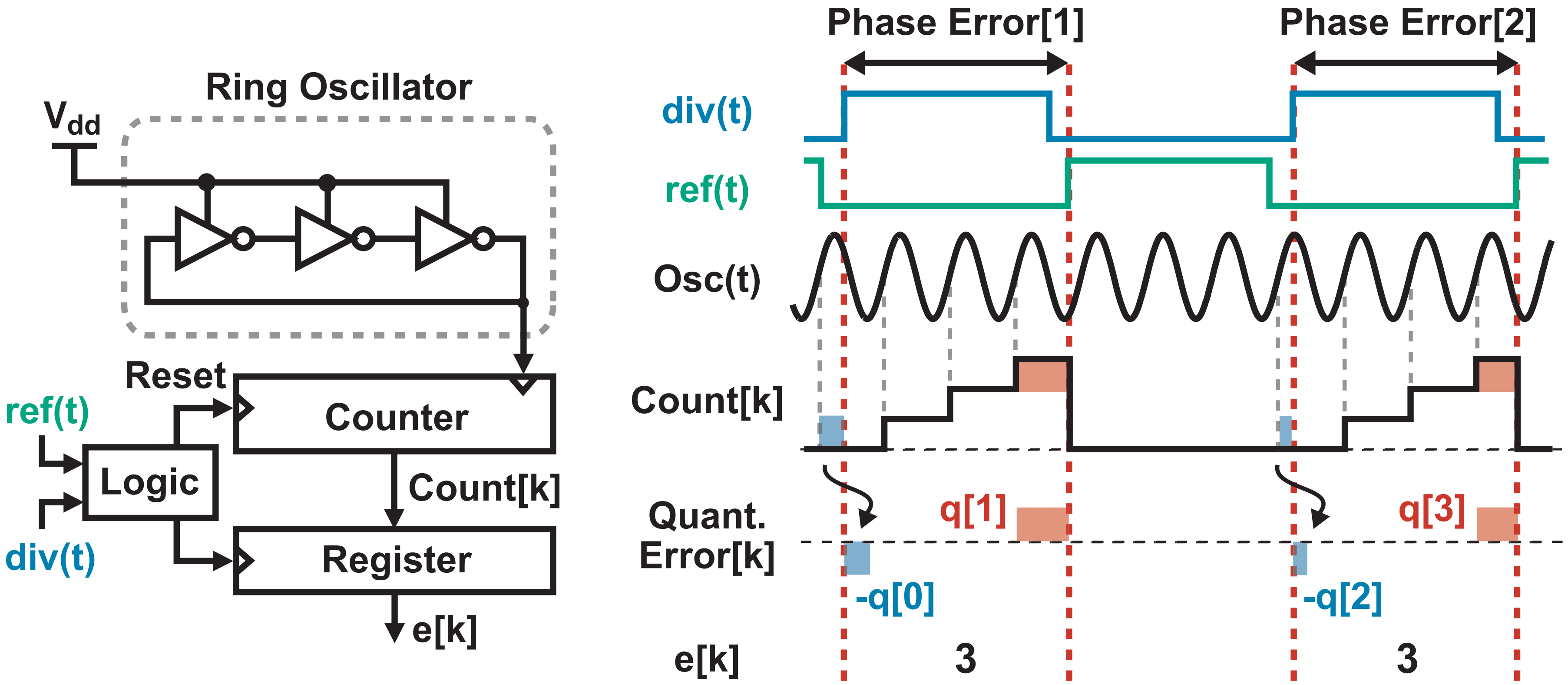
An Oscillator-Based TDC





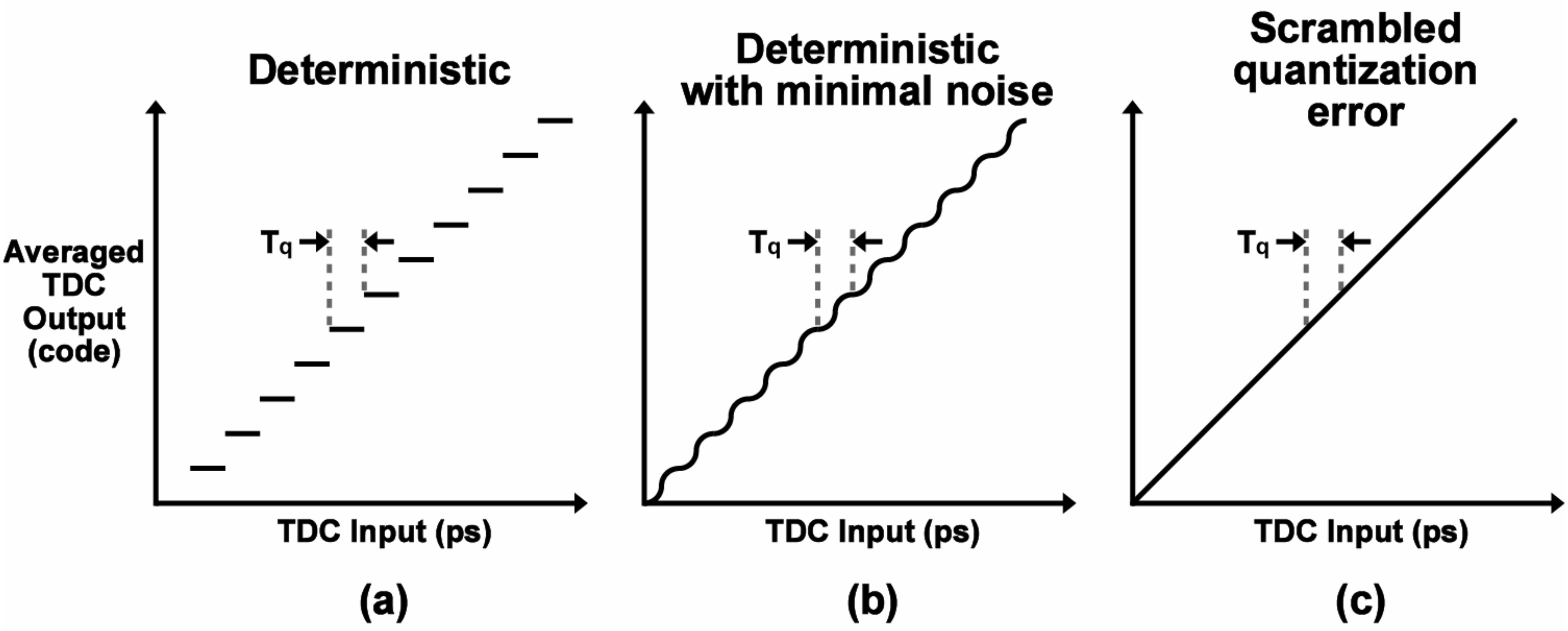
- Output *e[k]* corresponds to the number of oscillator edges that occur during the measurement time window
- Advantages
  - Extremely large range can be achieved with compact area
  - Quantization noise is scrambled across measurements

A Closer Look at Quantization Noise Scrambling



- Quantization error occurs at beginning and end of each measurement interval
- As a rough approximation, assume error is uncorrelated between measurements
  - Averaging of measurements improves effective resolution

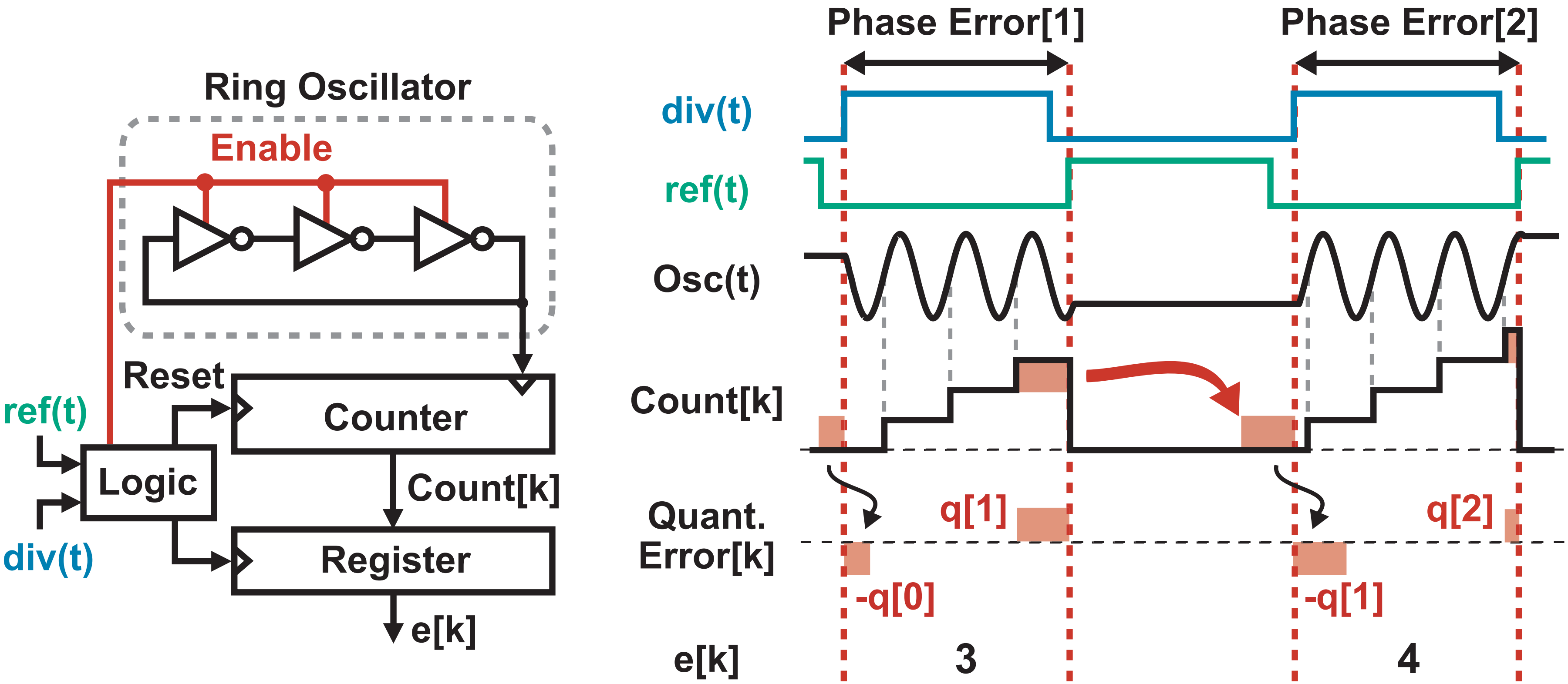
Deterministic quantizer error vs. scrambled error



- Deterministic TDC do not provide inherent scrambling
- For oversampling benefit, *TDC error must be scrambled!*
- Some systems provide input scrambling (ΔΣ fractional-N PLL), while some others do not (integer-N PLL)

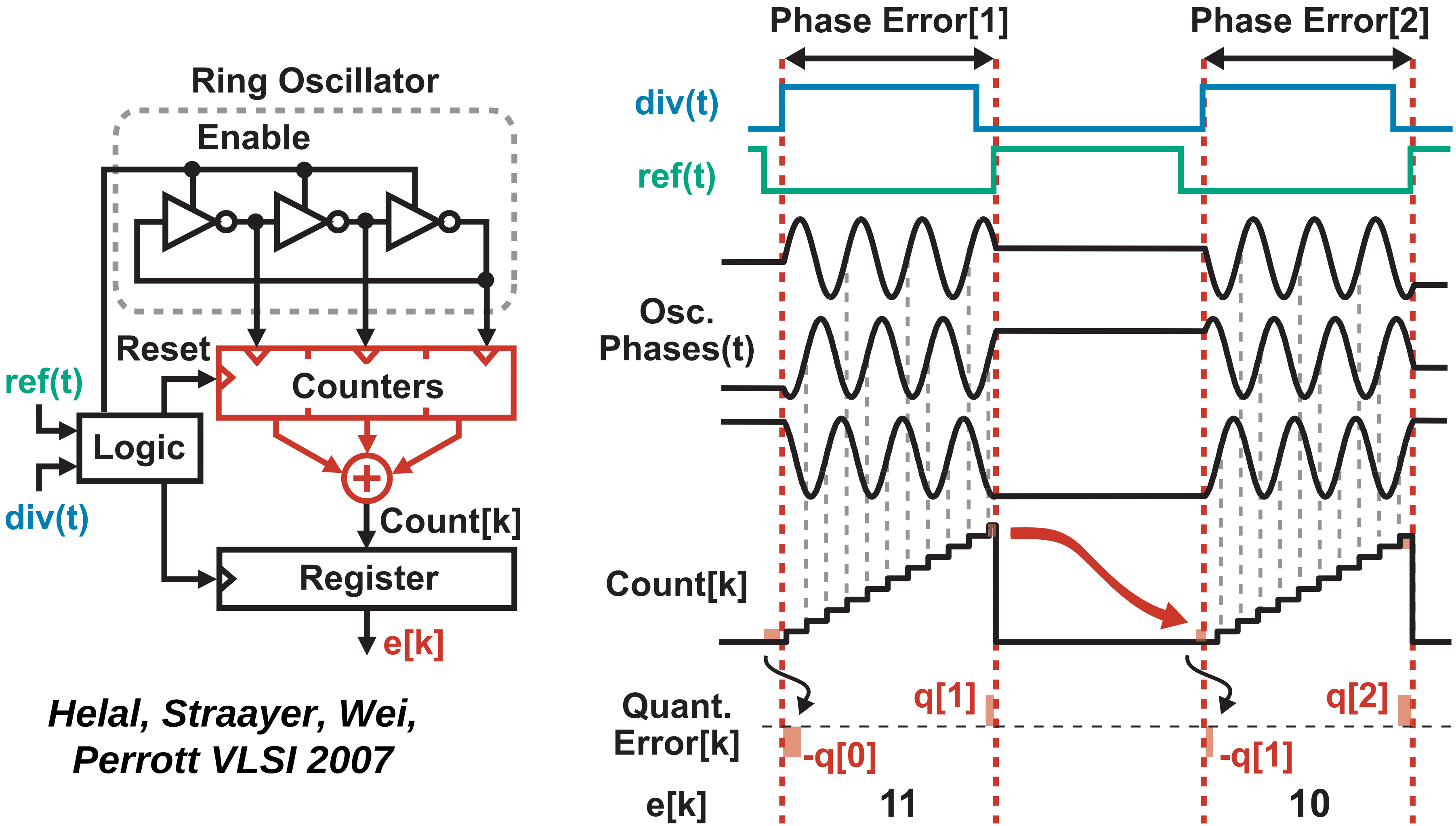
Proposed GRO TDC Structure

A Gated Ring Oscillator (GRO) TDC



- Enable ring oscillator only during measurement intervals
  - Hold the state of the oscillator between measurements
- Quantization error becomes first order noise shaped!
  - *e[k] = Phase Error[k] + q[k] – q[k-1]*
  - Averaging dramatically improves resolution!

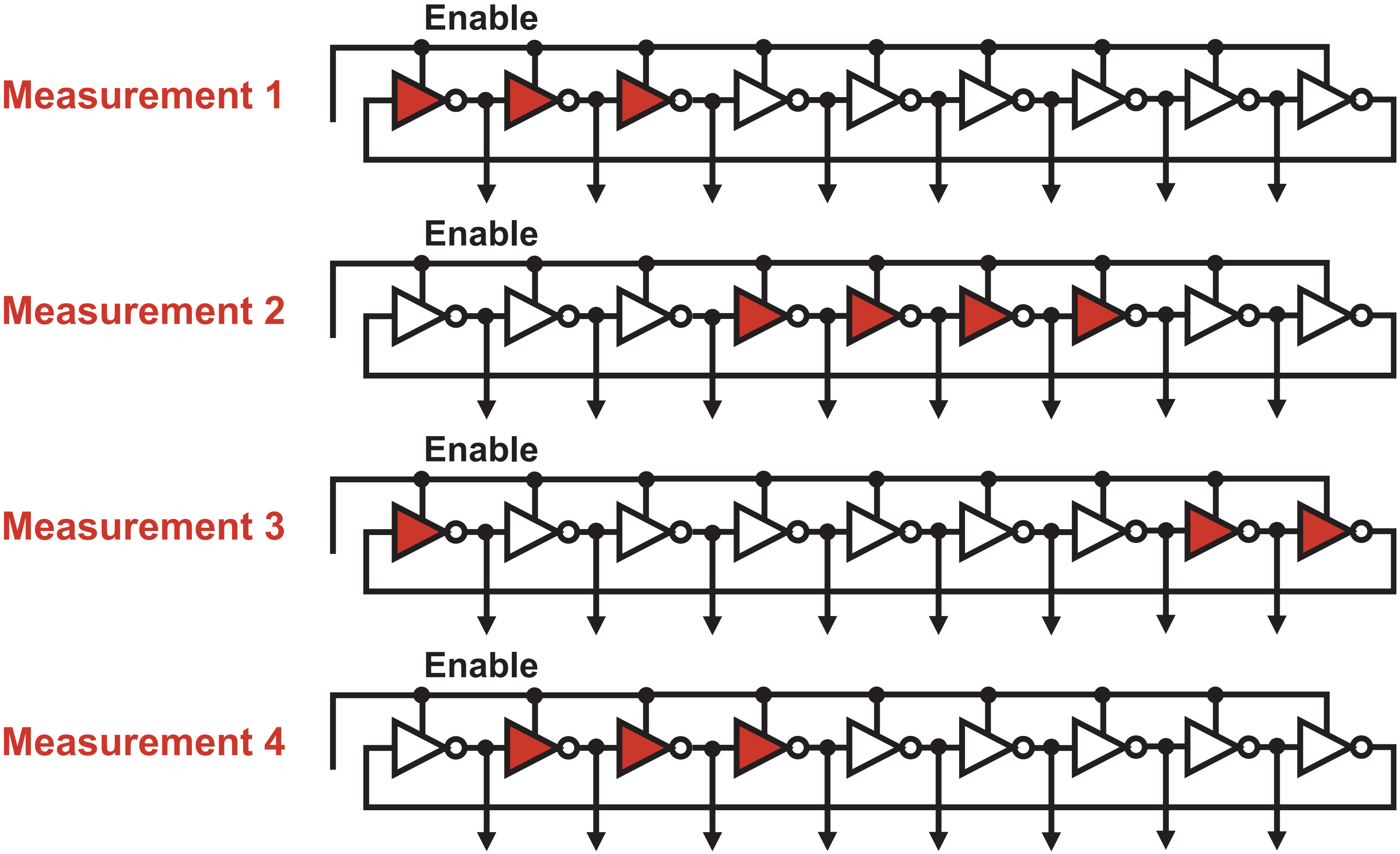
Improve Resolution By Using All Oscillator Phases



Helal, Straayer, Wei, Perrott VLSI 2007

- Raw resolution is set by inverter delay
- Effective resolution is dramatically improved by averaging

GRO TDC Also Shapes Delay Mismatch



Measurement 1

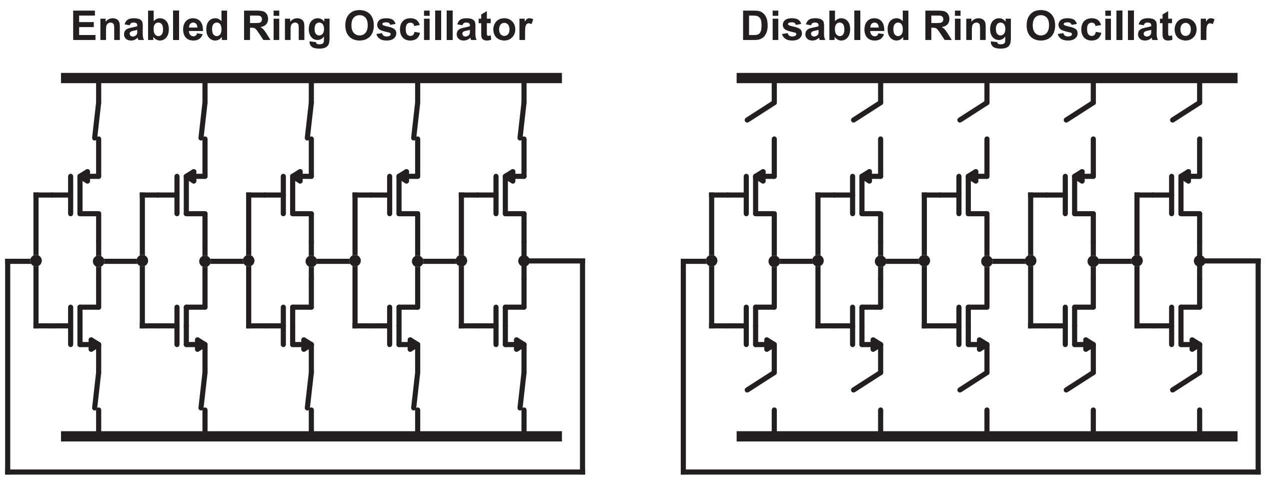
Measurement 2

Measurement 3

Measurement 4

- Barrel shifting occurs through delay elements across different measurements
  - Mismatch between delay elements is first order shaped!

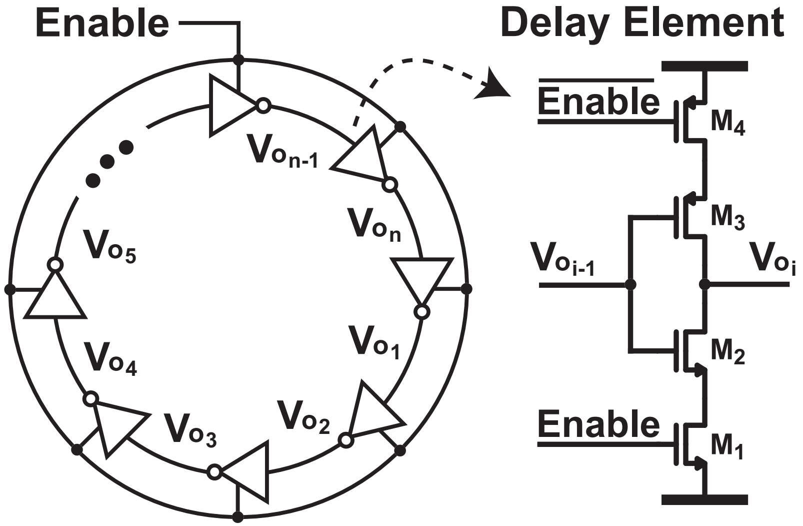
Simple gated ring oscillator inverter-based core



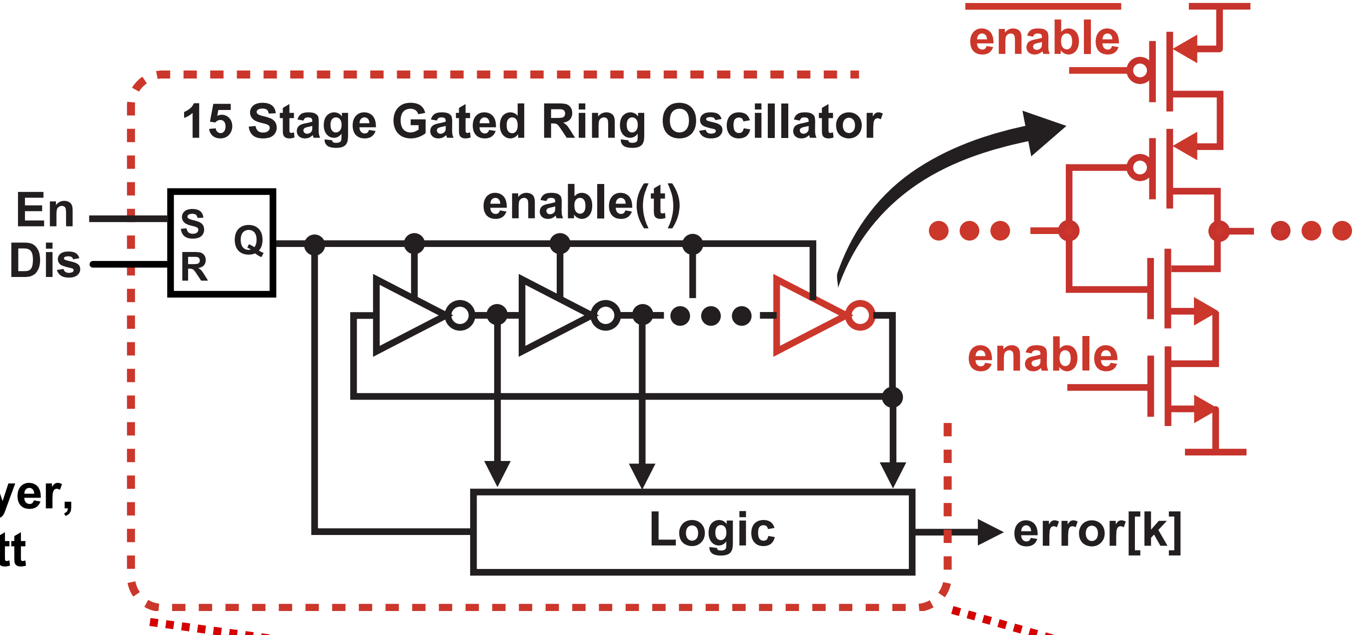
(a)

(b)

Gate the oscillator by switching the inverter cores to the power supply

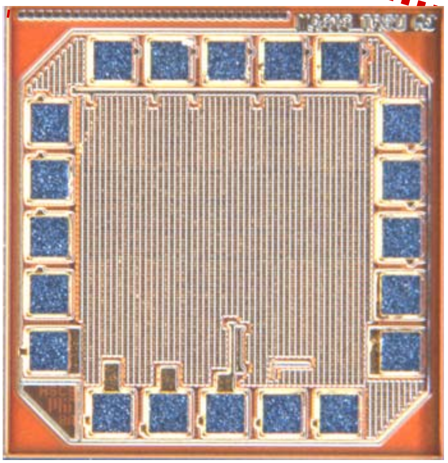


GRO Prototype

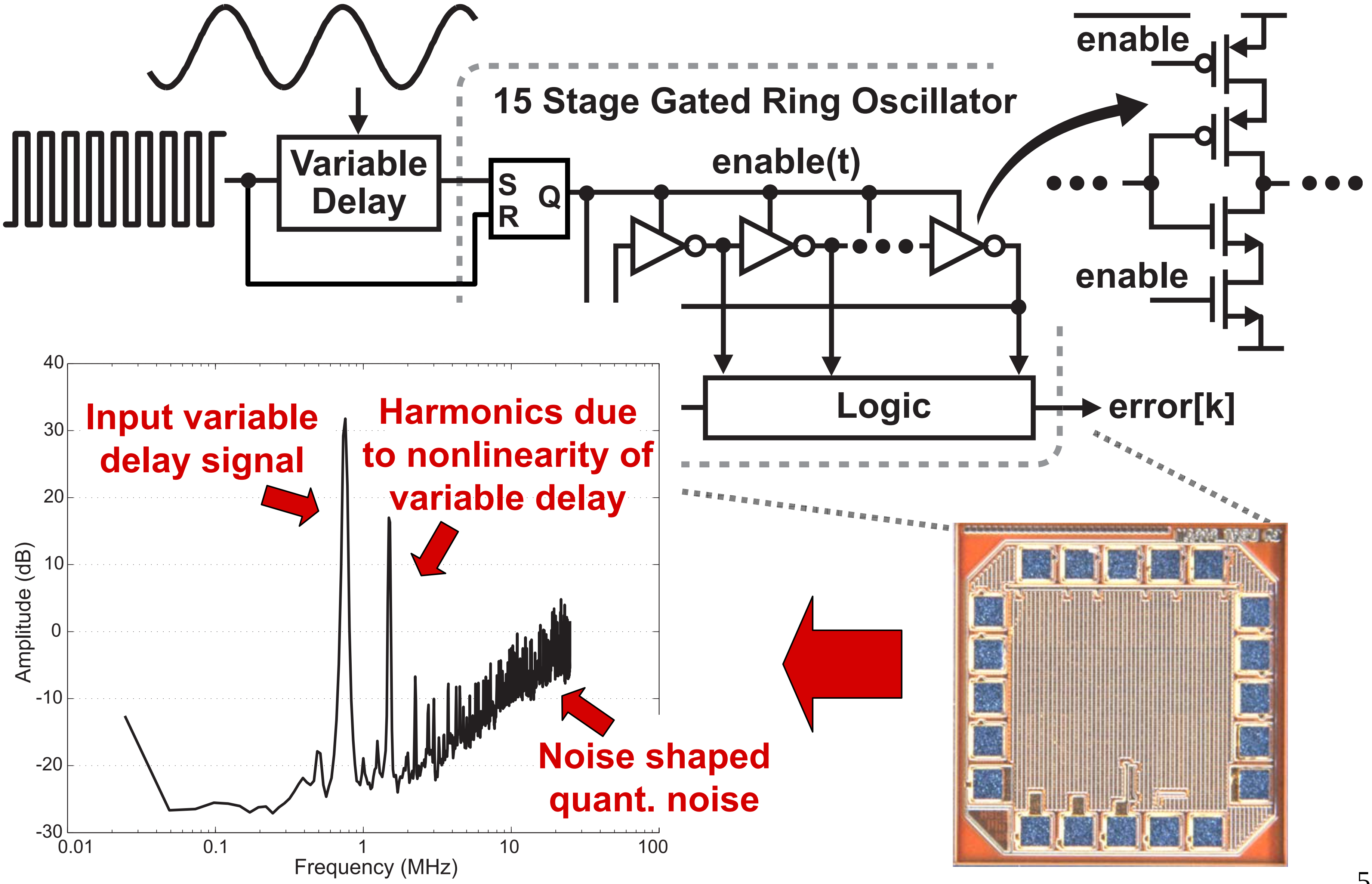


Straayer, Perrott

- GRO implemented as a custom 0.13 μm CMOS IC



Measured GRO Results Confirm Noise Shaping

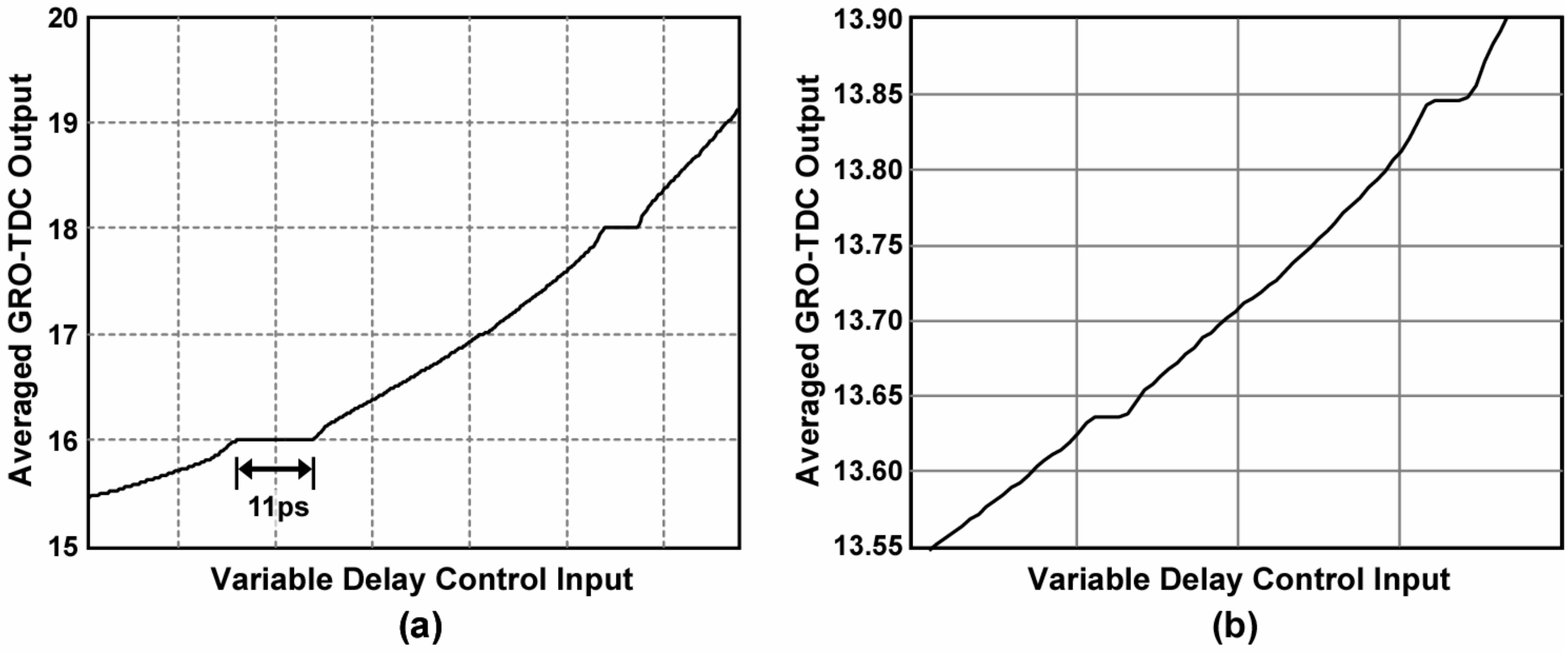


Input variable delay signal

Harmonics due to nonlinearity of variable delay

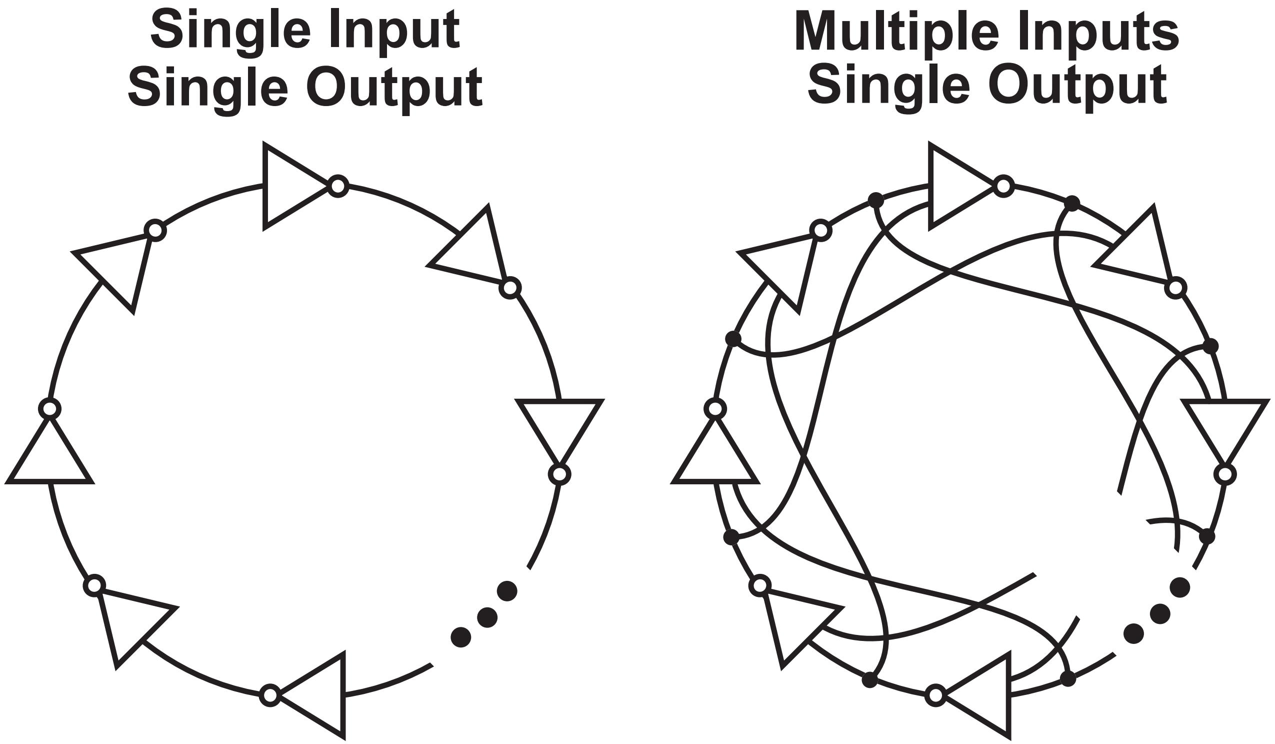
Noise shaped quant. noise

Measured deadzone behavior of inverter-based GRO



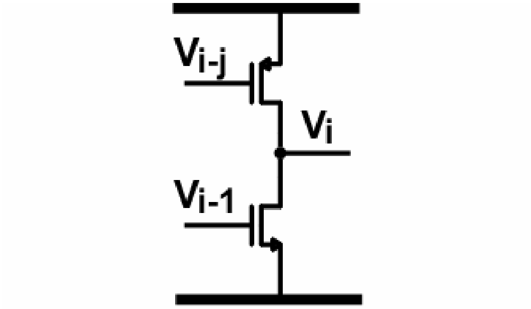
- **Deadzones were caused by errors in gating the oscillator**
- **GRO “injection locked” to an integer ratio of F_S**
- **Behavior occurred for almost all integer boundaries, and some fractional values as well**
- **Noise shaping benefit was limited by this gating error**

Next Generation GRO: Multi-path oscillator concept



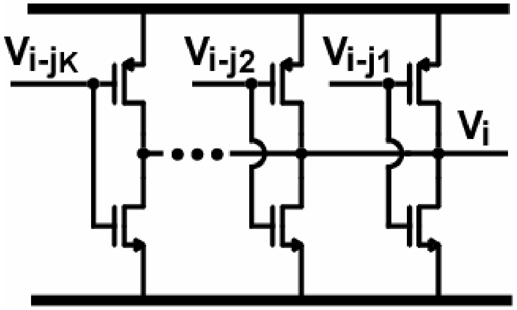
- Use multiple inputs for each delay element instead of one
- Allow each stage to optimally begin its transition based on information from the entire GRO phase state
- Key design issue is to ensure primary mode of oscillation

Multi-path inverter core



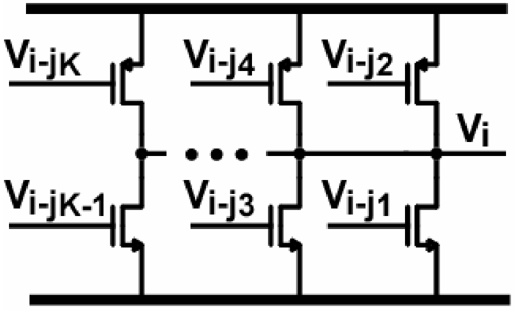
(a) Asymmetrically skewed inverter

Lee, Kim, Lee
JSSC 1997

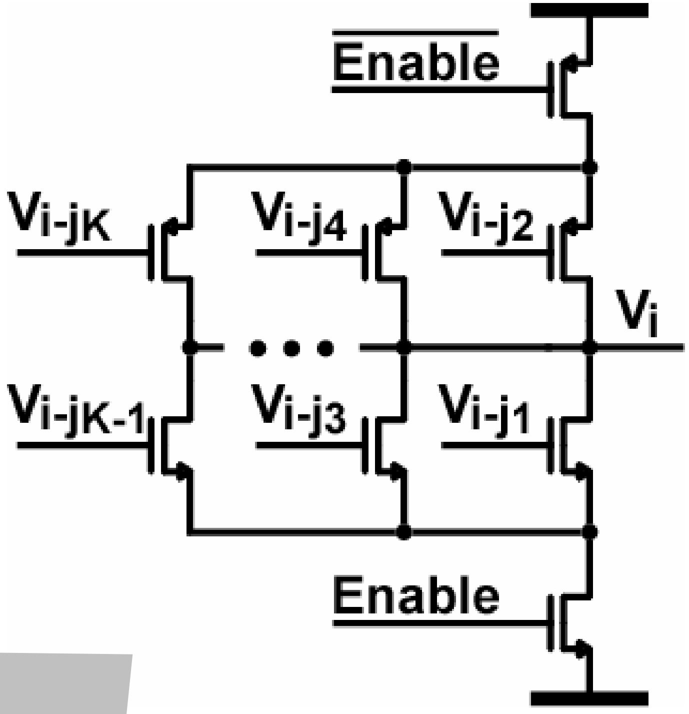


(b) Multiple skewed inverters

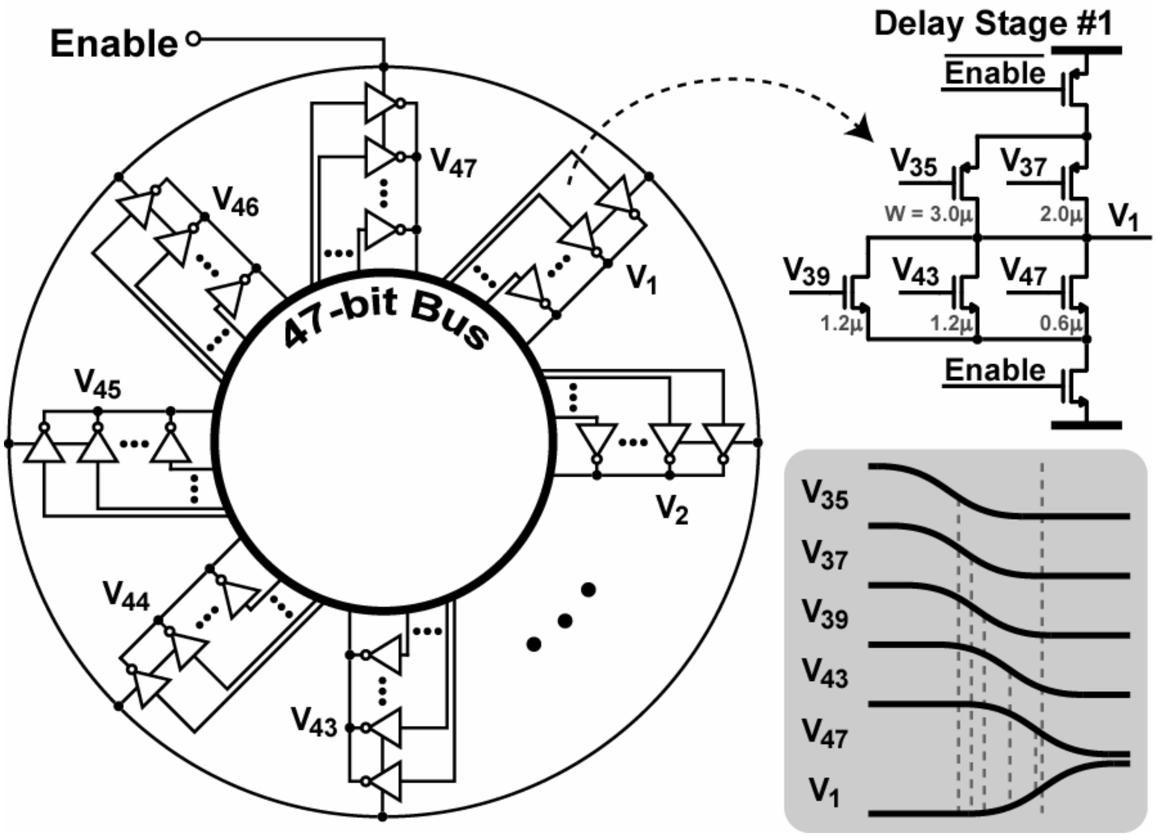
Mohan, et. al.,
CICC 2005



(c) Unrestricted connections



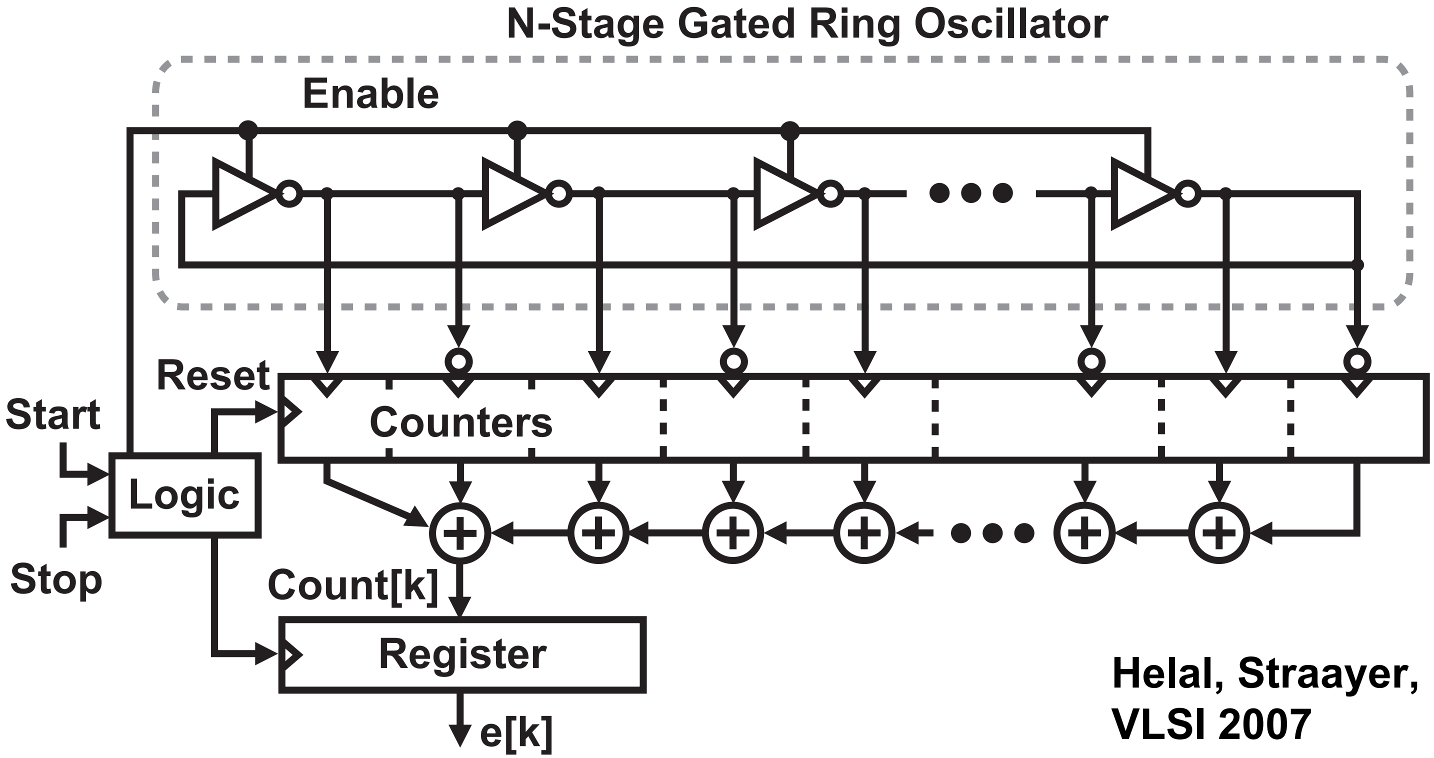
Proposed multi-path gated ring oscillator



Hsu, Straayer, Perrott
ISSCC 2008

- Oscillation frequency near 2GHz with 47 stages…
- Reduces effective delay per stage by a factor of 5-6!
- Represents a factor of 2-3 improvement compared to previous multi-path oscillators

A simple measurement approach…

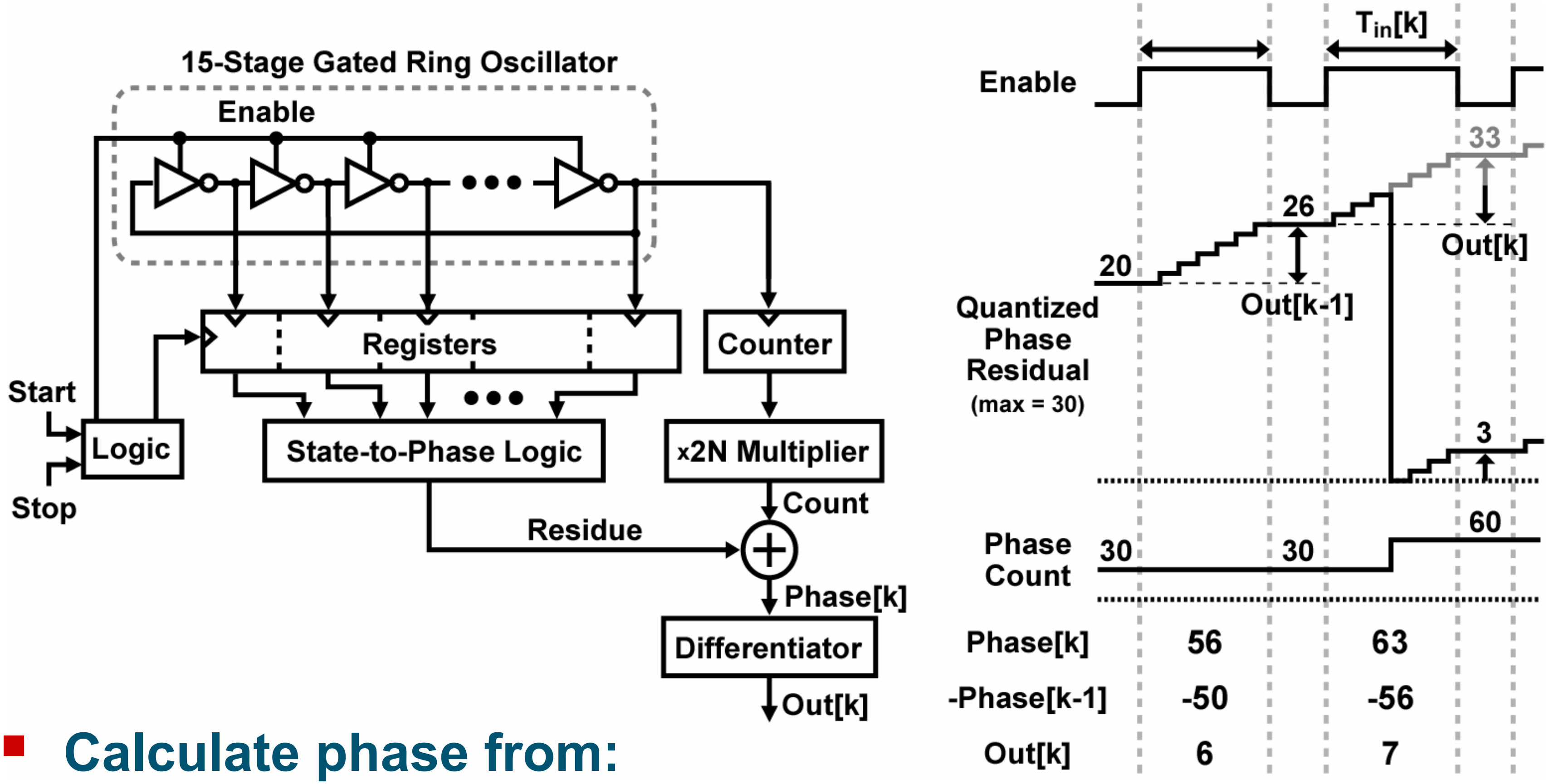


Helal, Straayer, Perrott
VLSI 2007

- 2 counters per stage * 47 stages = 94 counters each at 2GHz
- Power consumption for these counters is unreasonable

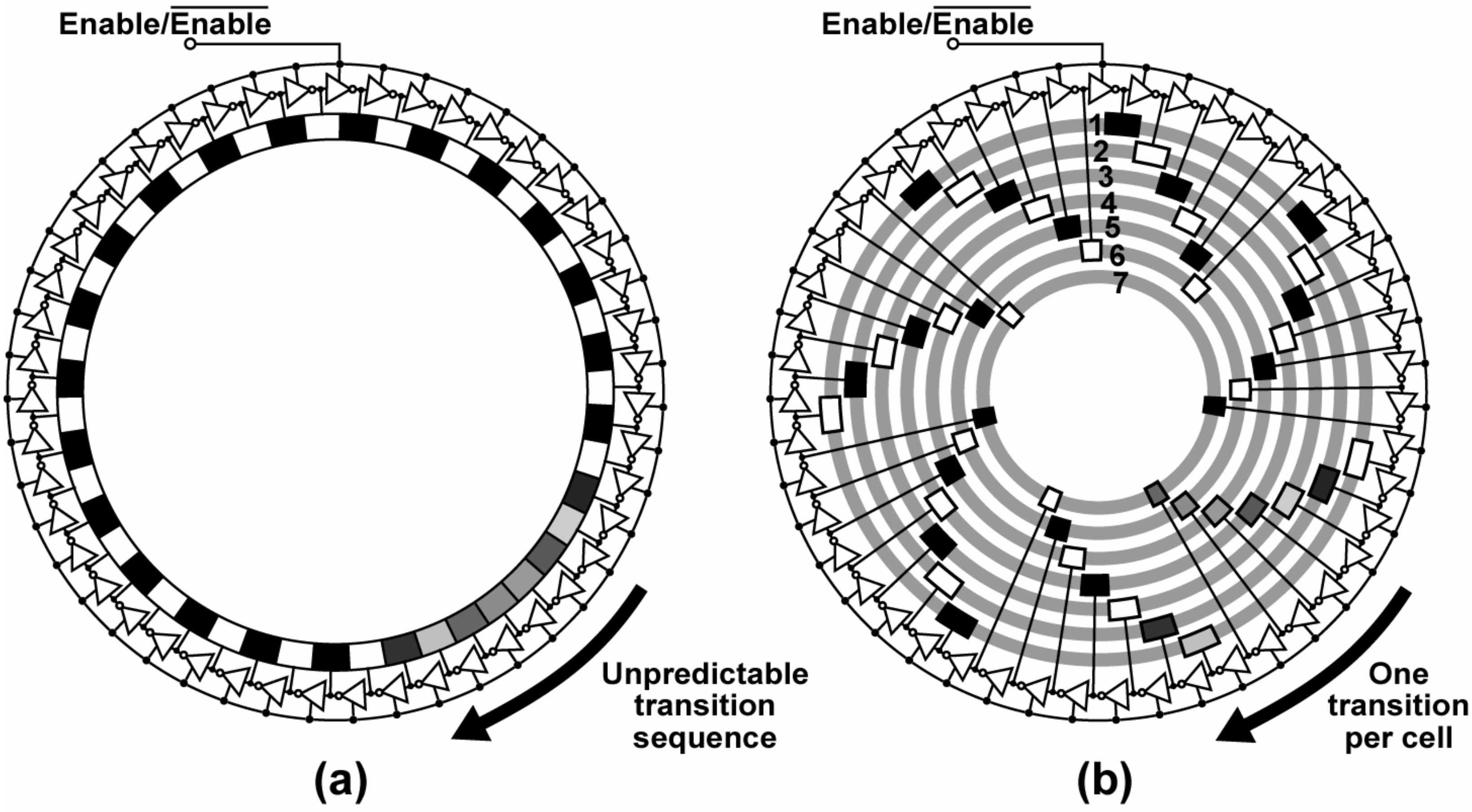
Need a more efficient way to measure the multi-path GRO

Count Edges by Sampling Phase



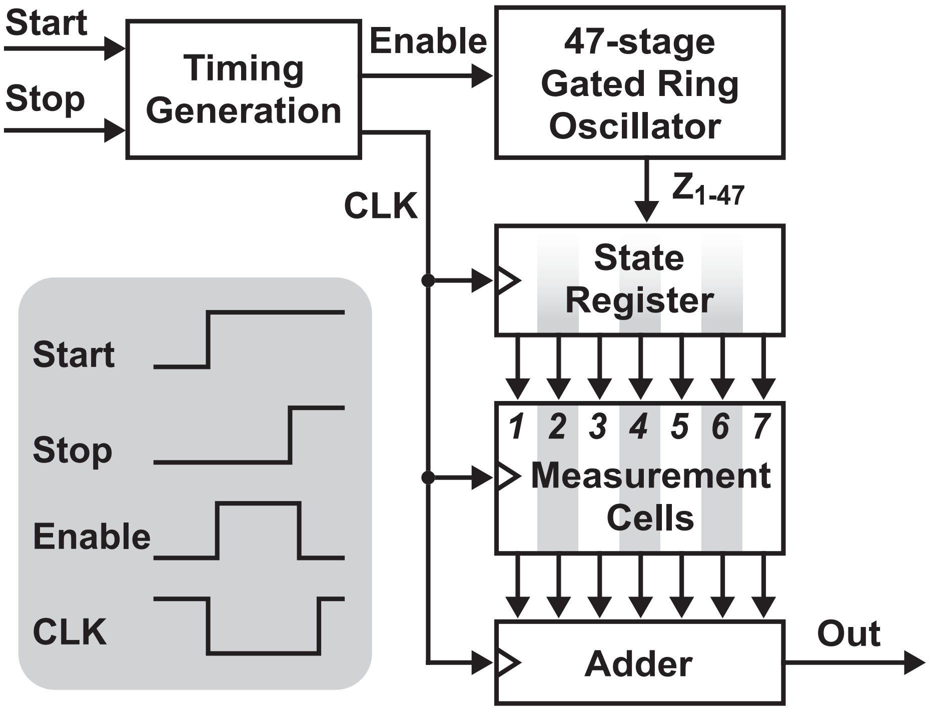
- Calculate phase from:
  - A single counter for coarse phase information (keeps track of phase wrapping)
  - GRO phase state for fine count information
- 1 counter and N registers → much more efficient

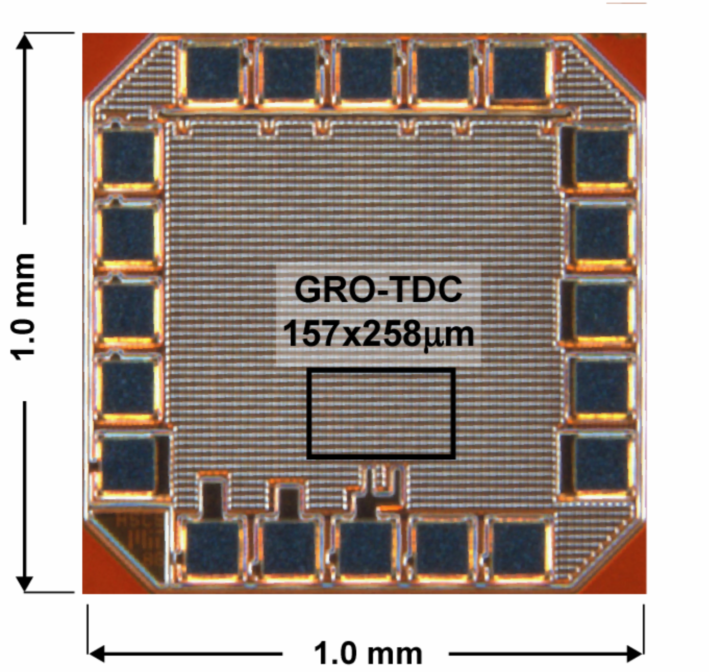
Proposed Multi-Path Measurement Structure


Enable/$\overline{\text{Enable}}$
Unpredictable transition sequence
(a)
Enable/$\overline{\text{Enable}}$
1
2
3
4
5
6
7
One transition per cell
(b)

- Multi-path structure leads to ambiguity in edge position
- Partition into 7 cells to avoid such ambiguity
  - Requires 7 counters rather than 1, but power still OK

Prototype 0.13μm CMOS multi-path GRO-TDC

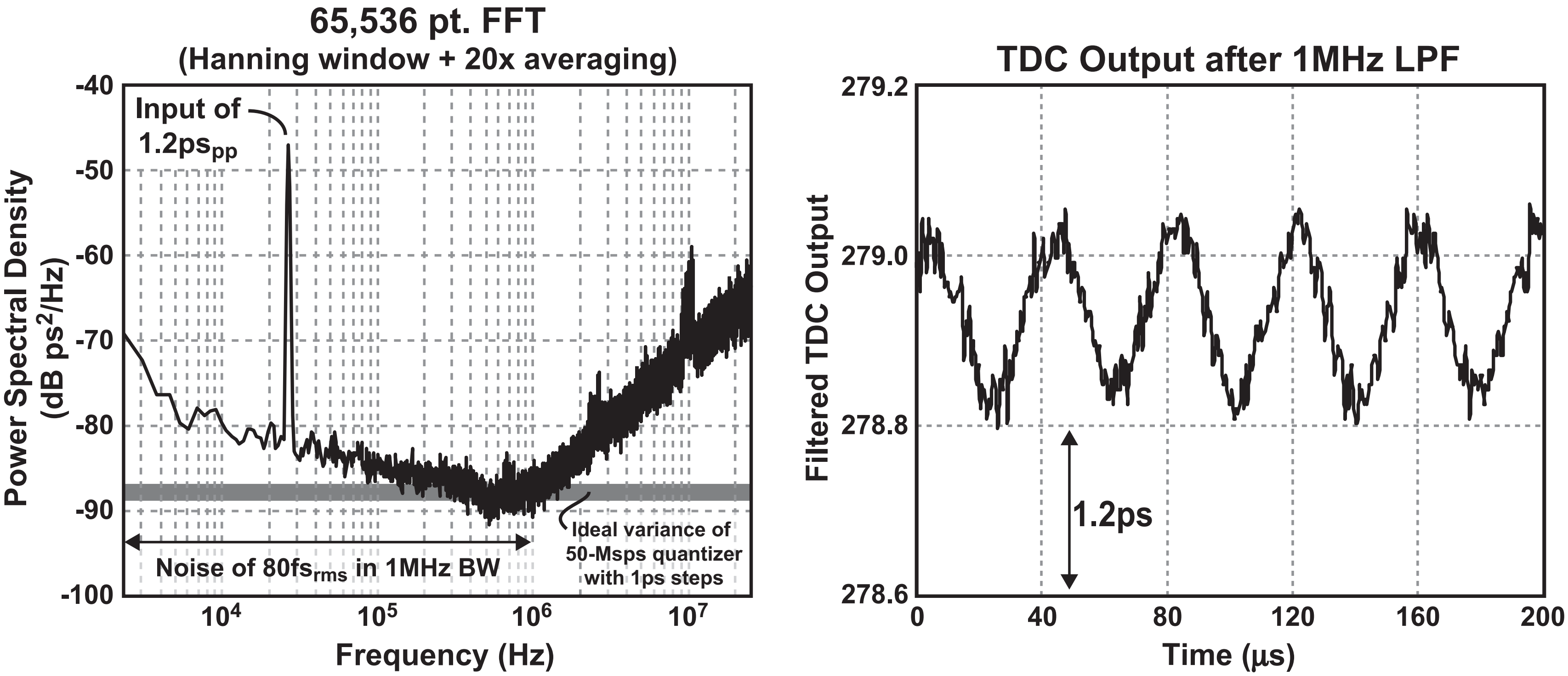




Straayer et al., VLSI 2008

- **Two implemented versions:**
  - **8-bit, 500Msps**
  - **11-bit, 100Msps version**
- **2-21mW power consumption depending on input duty cycle**

Measured noise-shaping of multi-path GRO

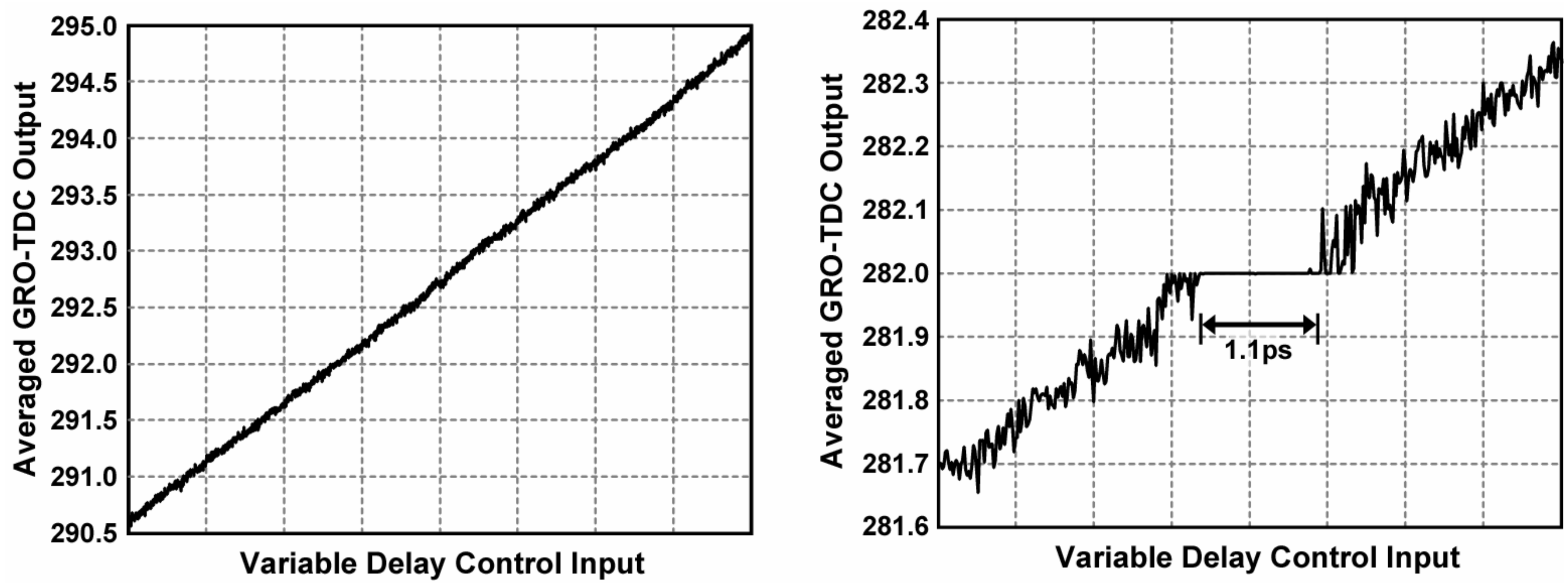


(a)

(b)

- Data collected at 50Msps
- More than 20dB of noise-shaping benefit
- 80fs$_{rms}$ integrated error from 2kHz-1MHz
- Floor primarily limited by 1/f noise (up to 0.5-1MHz)

Measured deadzone behavior for multi-path GRO



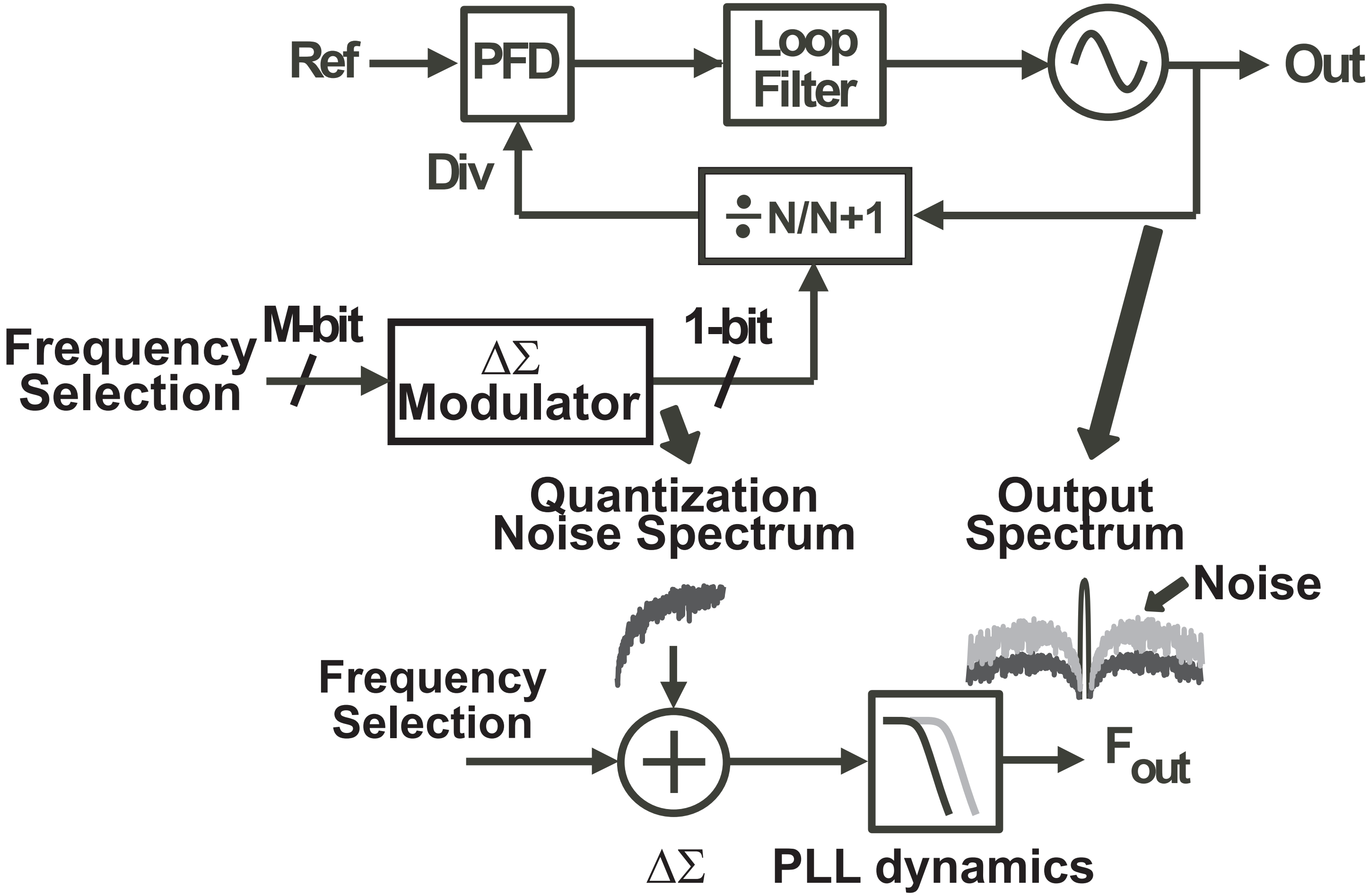
(a)

(b)

- Only deadzones for outputs that are multiples of 2N
  - 94, 188, 282, etc.
  - No deadzones for other even or odd integers, fractional output
- Size of deadzone is reduced by 10x

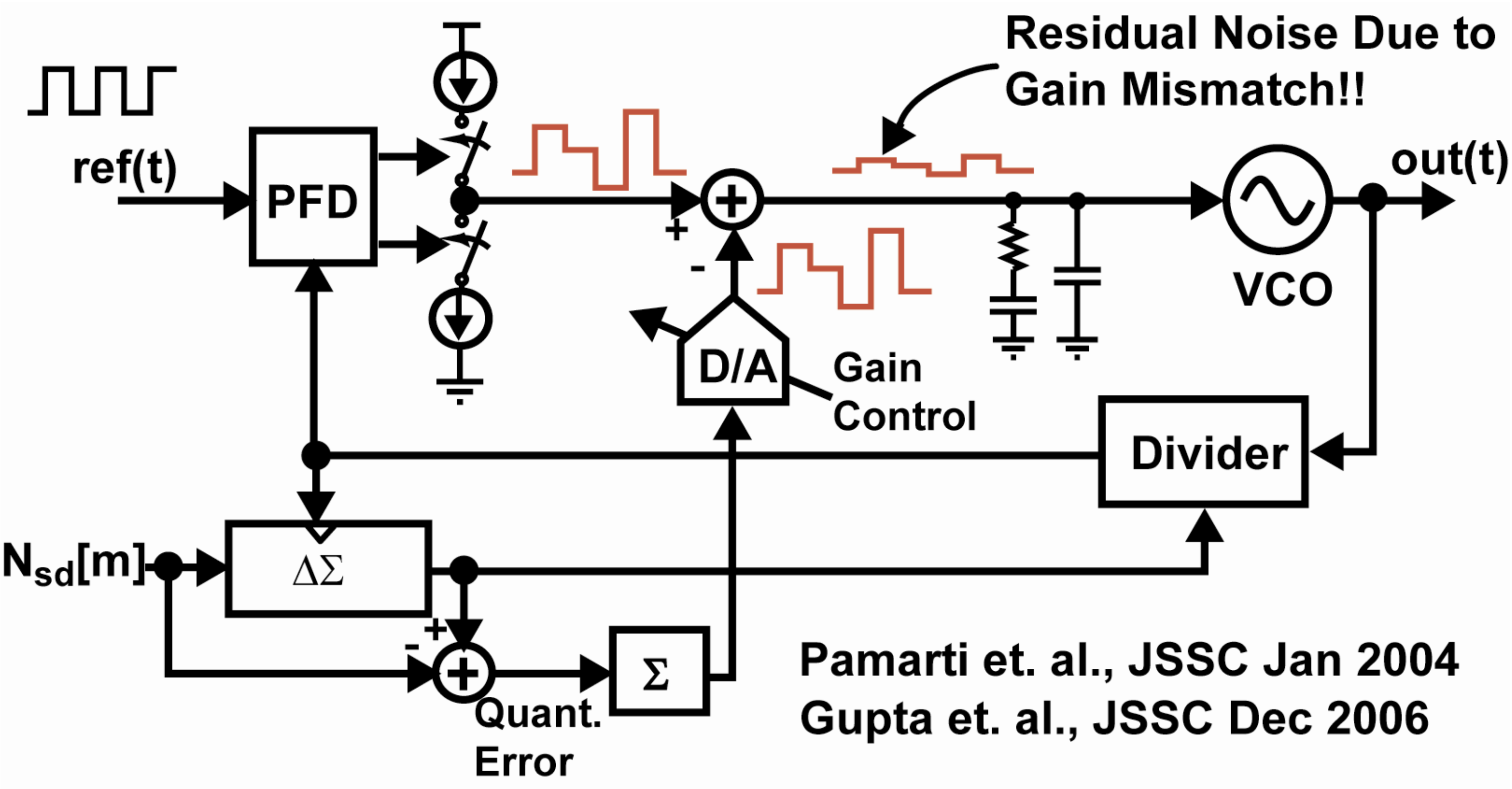
The Issue of Quantization Noise Due to Divider Dithering

The Nature of the Quantization Noise Problem



- Increasing PLL bandwidth increases impact of ΔΣ fractional-N noise
  - Cancellation offers a way out!

Previous Analog Quantization Noise Cancellation

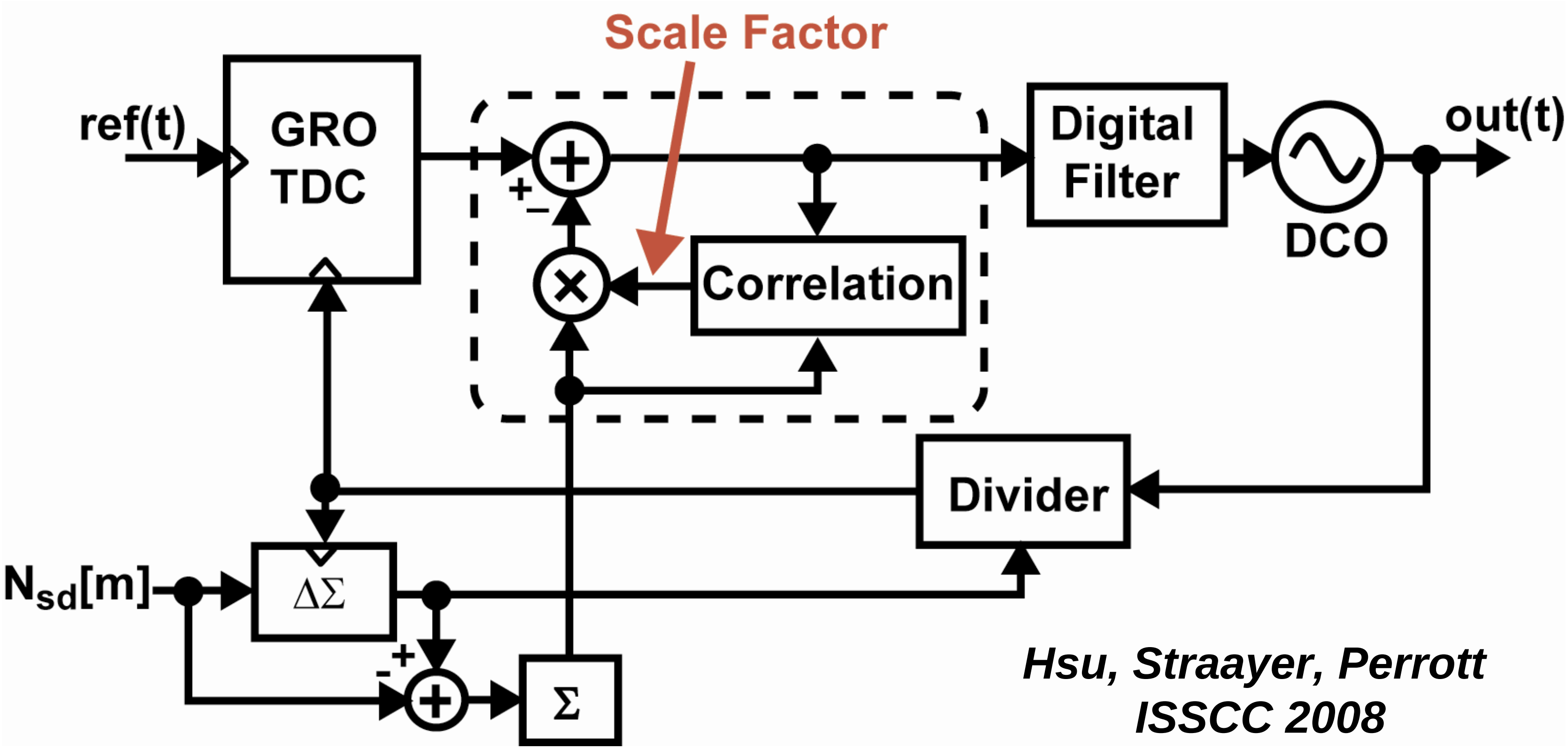


Pamarti et. al., JSSC Jan 2004
Gupta et. al., JSSC Dec 2006

- **Phase error due to ΔΣ is predicted by accumulating ΔΣ quantization error**
- **Gain matching between PFD and D/A must be precise**

Matching in *analog* domain limits performance

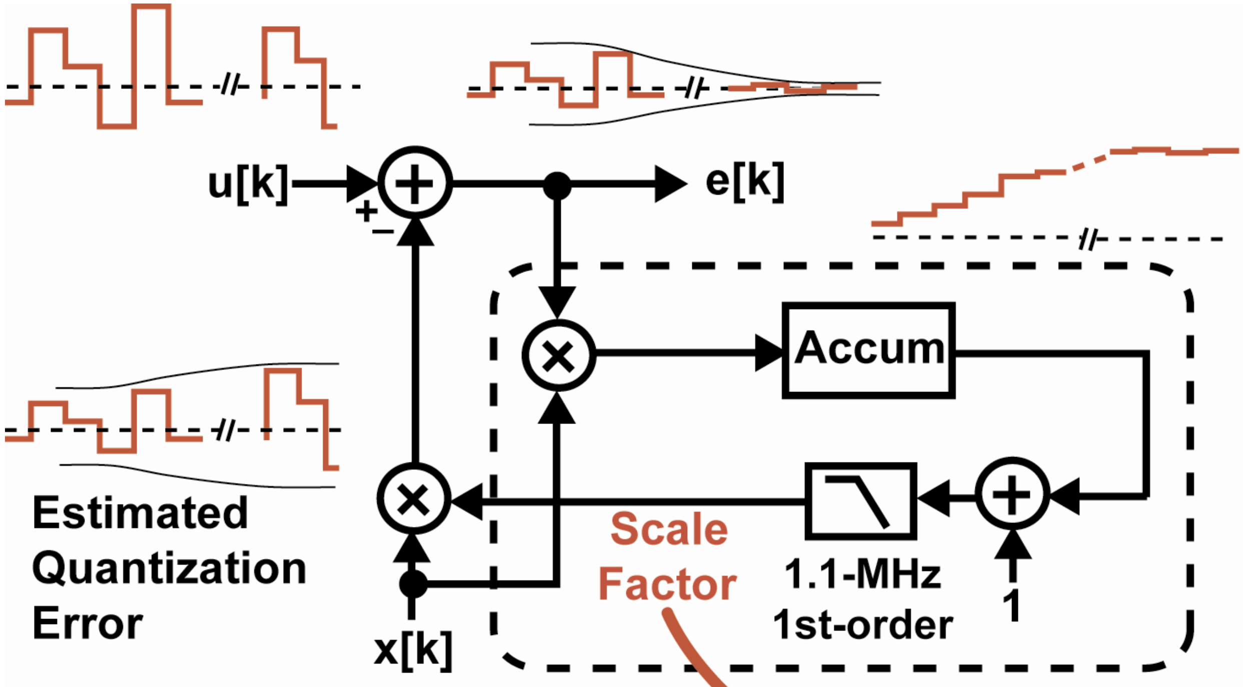
Proposed All-digital Quantization Noise Cancellation

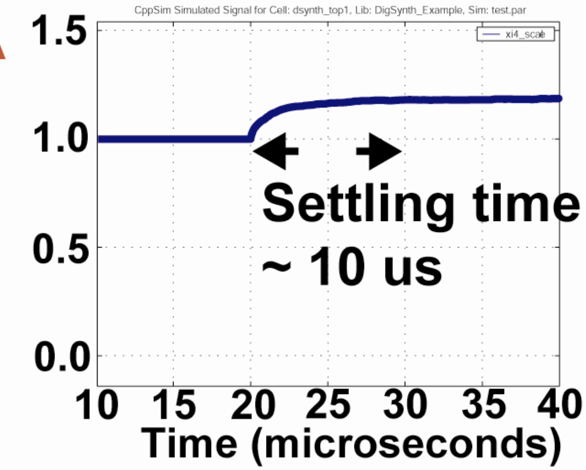


Hsu, Straayer, Perrott
ISSCC 2008

- Scale factor determined by simple digital correlation
- Analog non-idealities such as DC offset are completely eliminated

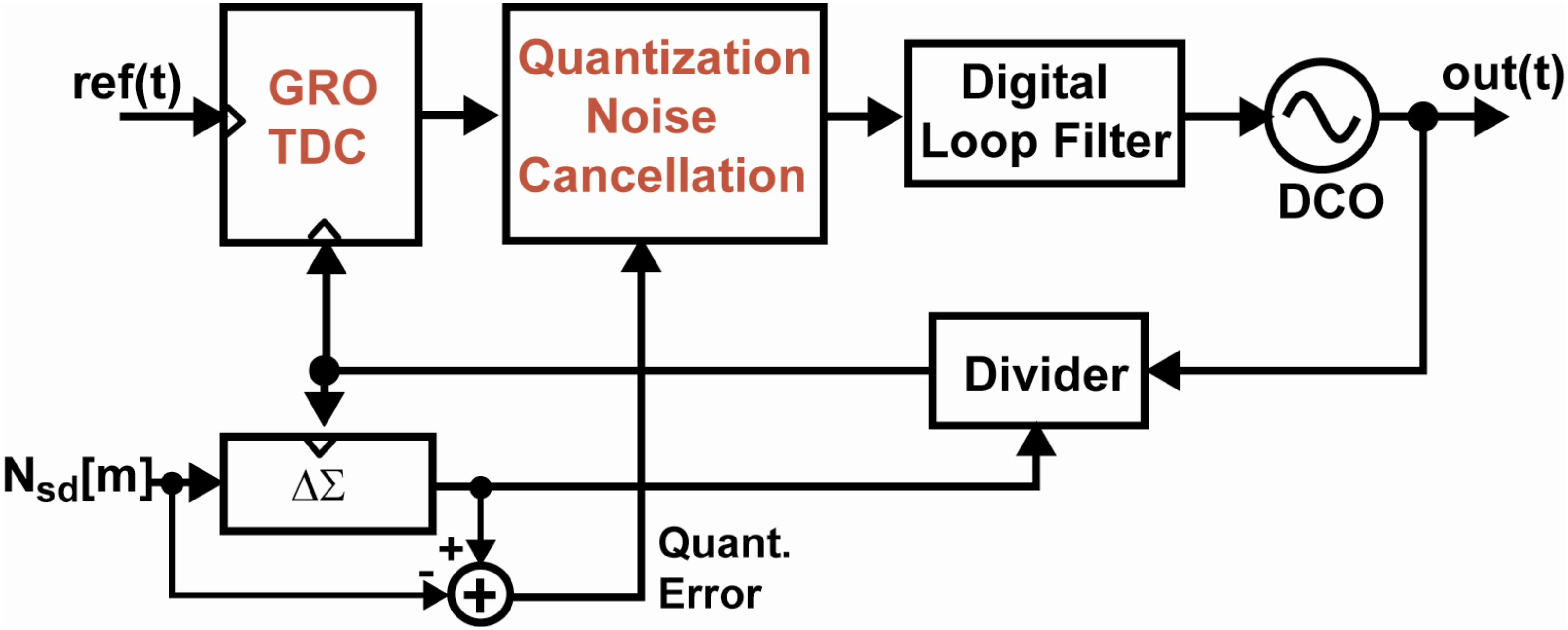
Details of Proposed Quantization Noise Cancellation





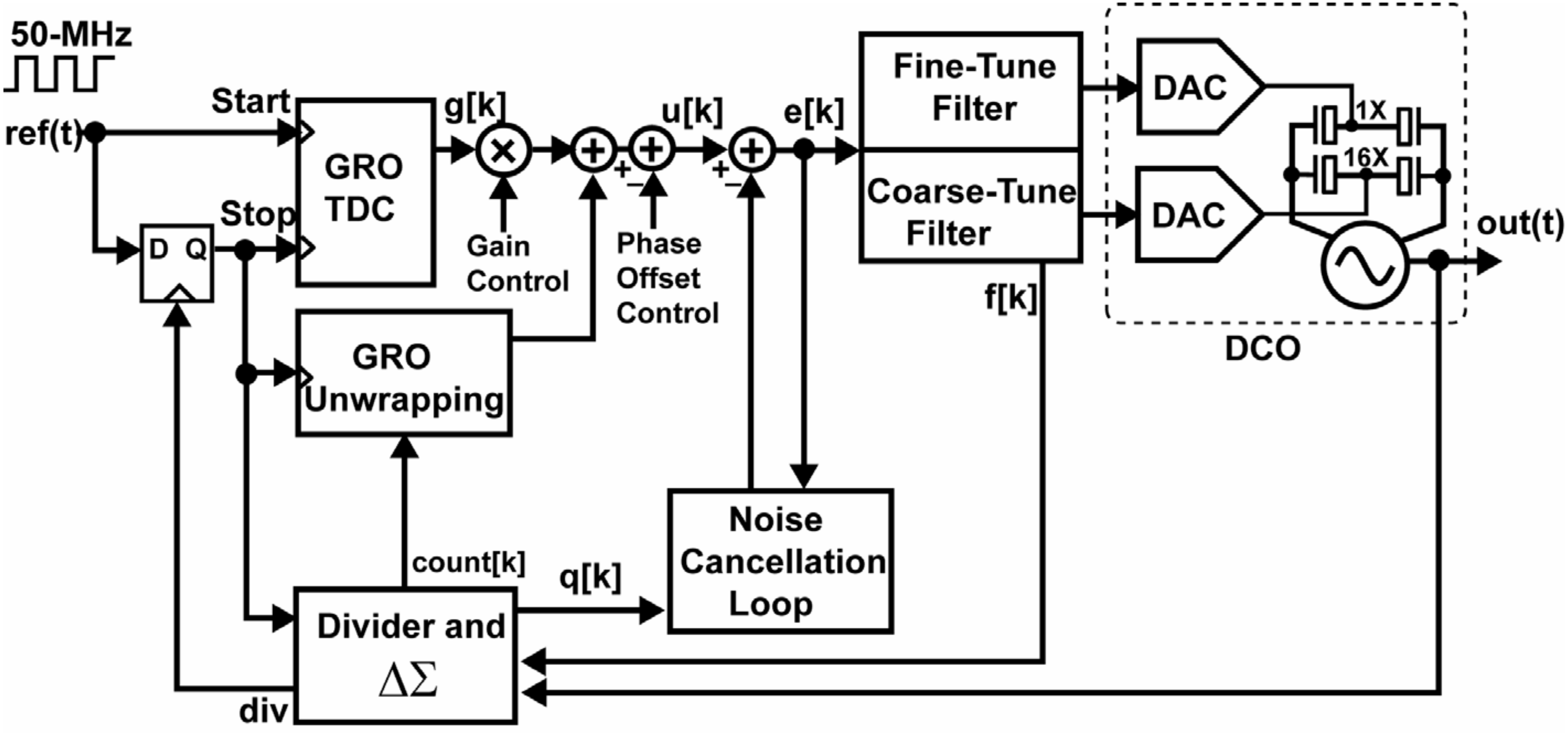
- Correlator out is accumulated and filtered to achieve scale factor
  - Settling time chosen to be around 10 us
- See *analog* version of this technique in *Swaminathan et.al., ISSCC 2007*

Proposed Digital Wide BW Synthesizer



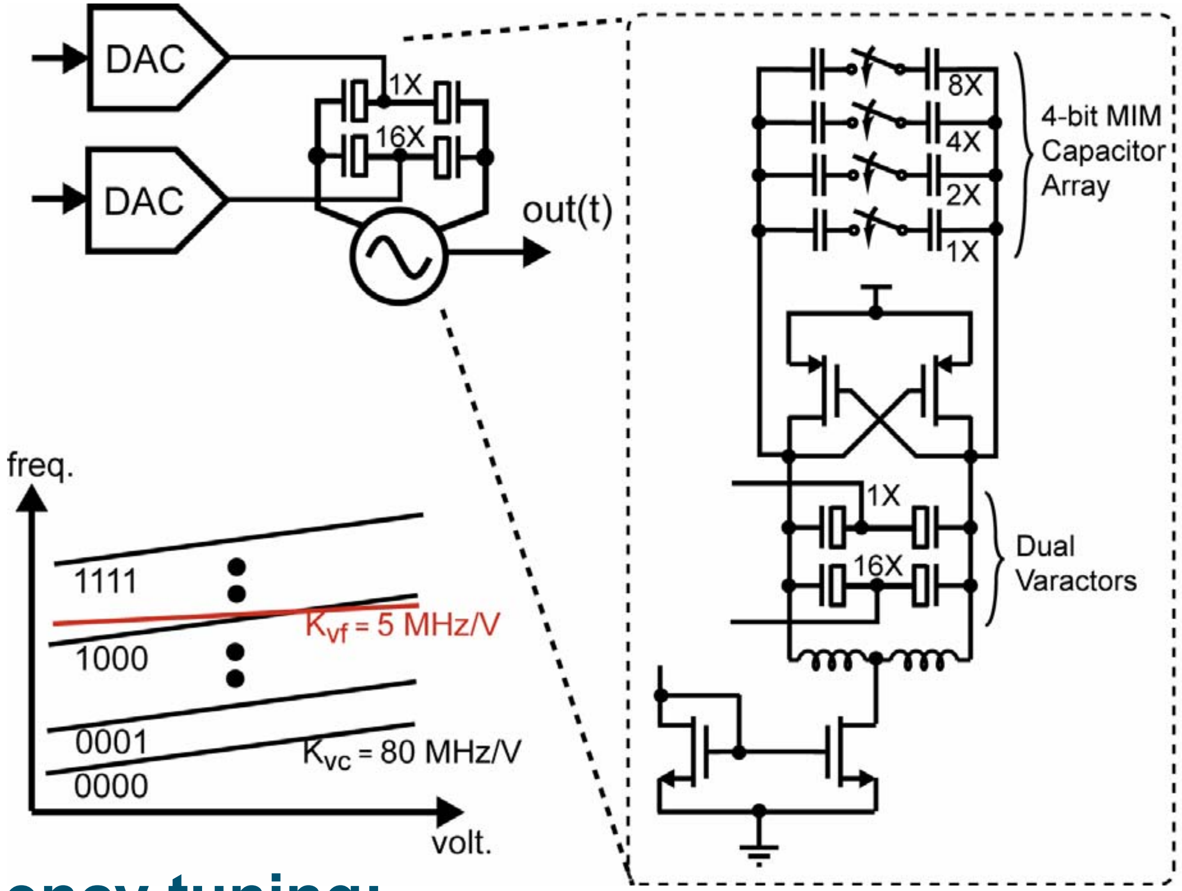
- *Gated-ring-oscillator (GRO) TDC* achieves low in-band noise
- *All-digital quantization noise cancellation* achieves low out-of-band noise
- Design goals:
  - 3.6-GHz carrier, 500-kHz bandwidth
  - <-100dBc/Hz in-band, <-150 dBc/Hz at 20 MHz offset

Overall Synthesizer Architecture



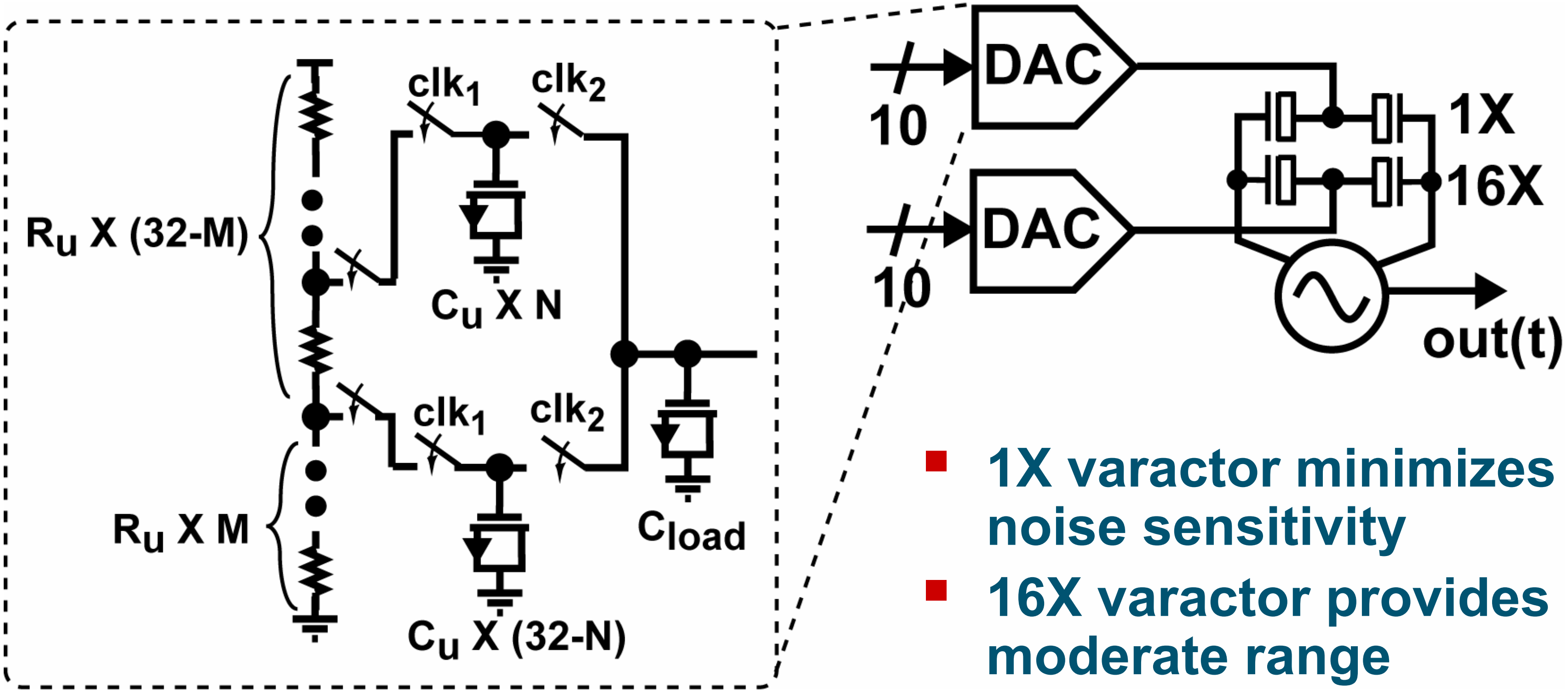
Note: Detailed behavioral simulation model available at http://www.cppsim.com

Dual-Port LC VCO



- **Frequency tuning:**
  - **Use a small 1X varactor to minimize noise sensitivity**
  - **Use another 16X varactor to provide moderate range**
  - **Use a four-bit capacitor array to achieve 3.3-4.1 GHz range**

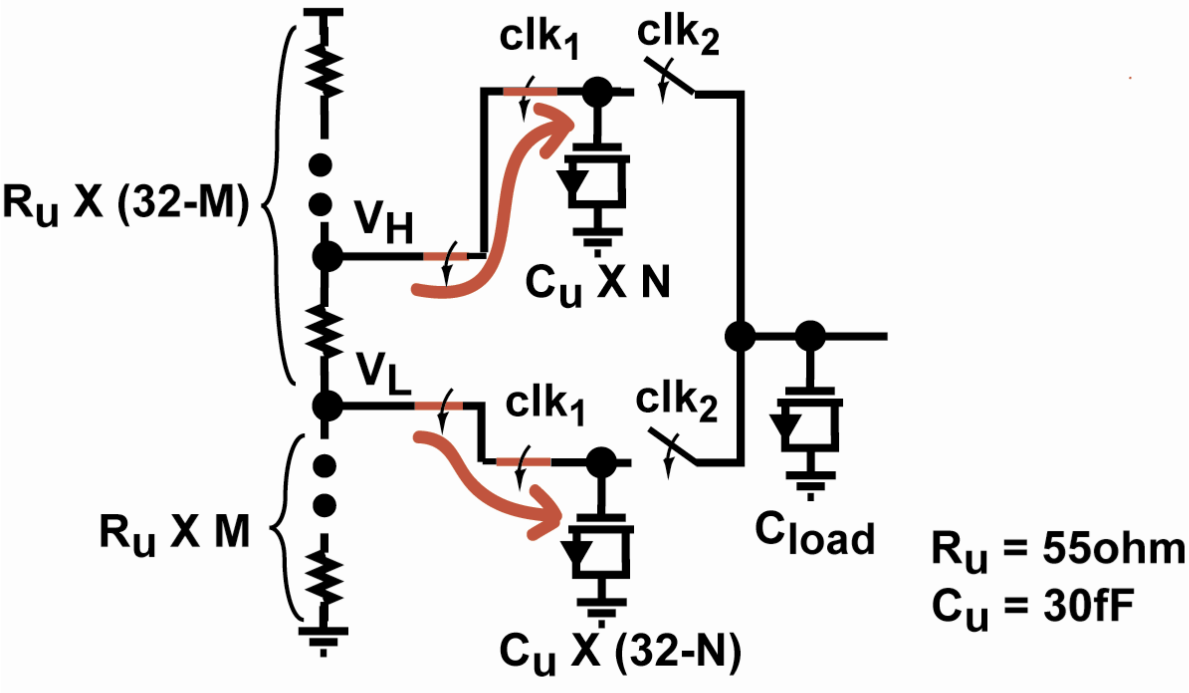
Digitally-Controlled Oscillator with Passive DAC



- 1X varactor minimizes noise sensitivity
- 16X varactor provides moderate range
- A four-bit capacitor array covers 3.3-4.1GHz

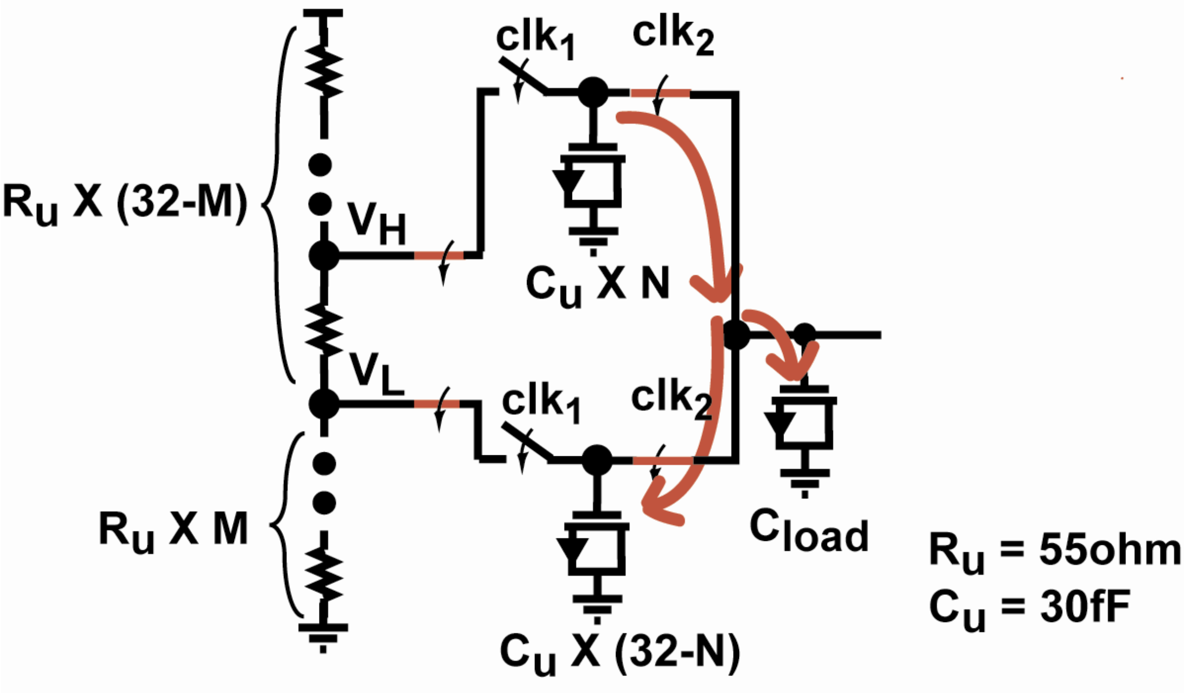
- Goals of 10-bit DAC
  - Monotonic
  - Minimal active circuitry and no transistor bias currents
  - Full-supply output range

Operation of 10-bit Passive DAC (Step 1)



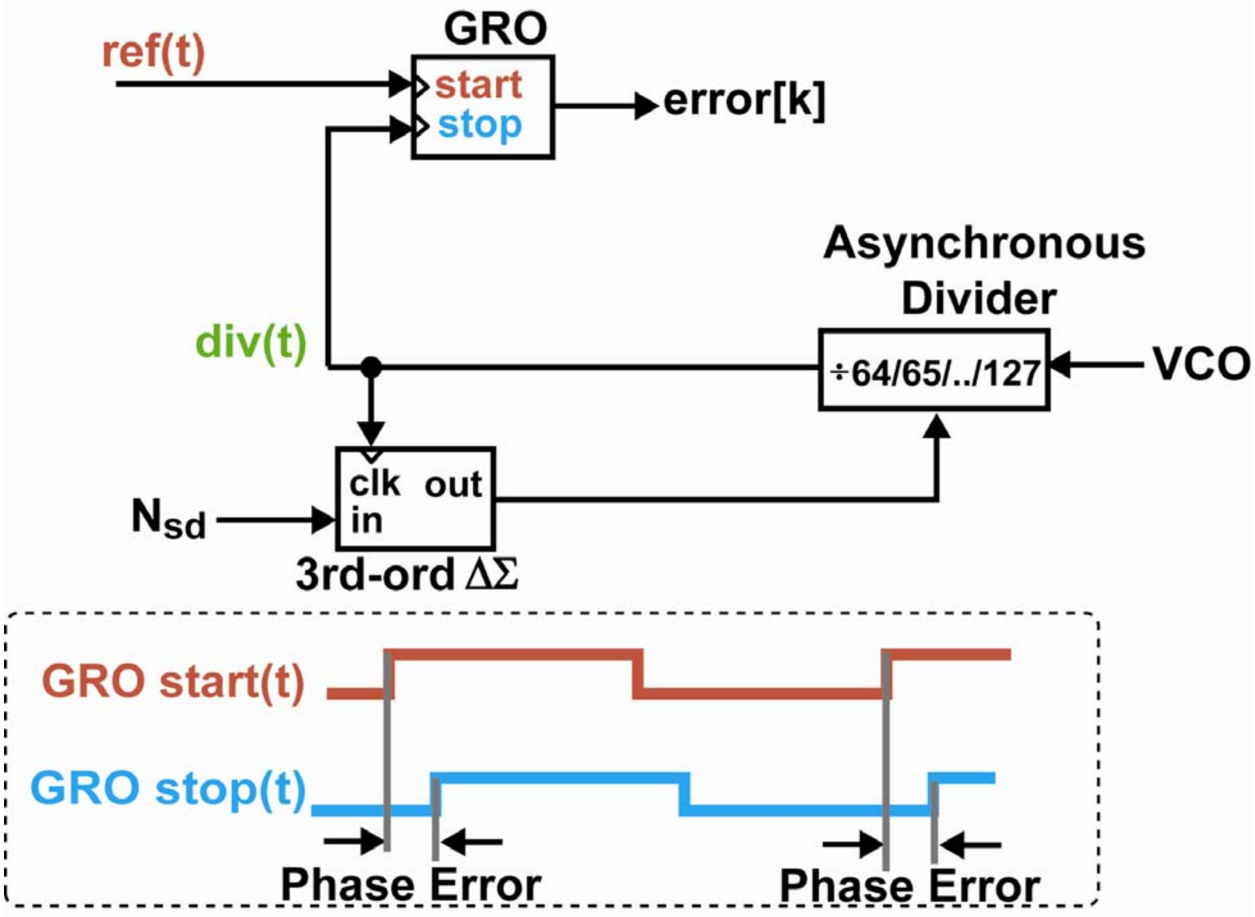
- 5-bit resistor ladder; 5-bit switch-capacitor array
- Step 1: *Capacitors Charged*
  - Resistor ladder forms V_L = M/32•V_{DD} and V_H = (M+1)/32•V_{DD}, where M ranges from 0 to 31
  - N unit capacitors charged to V_H, and (32-N) unit capacitors charged to V_L

Operation of 10-bit Passive DAC (Step 2)



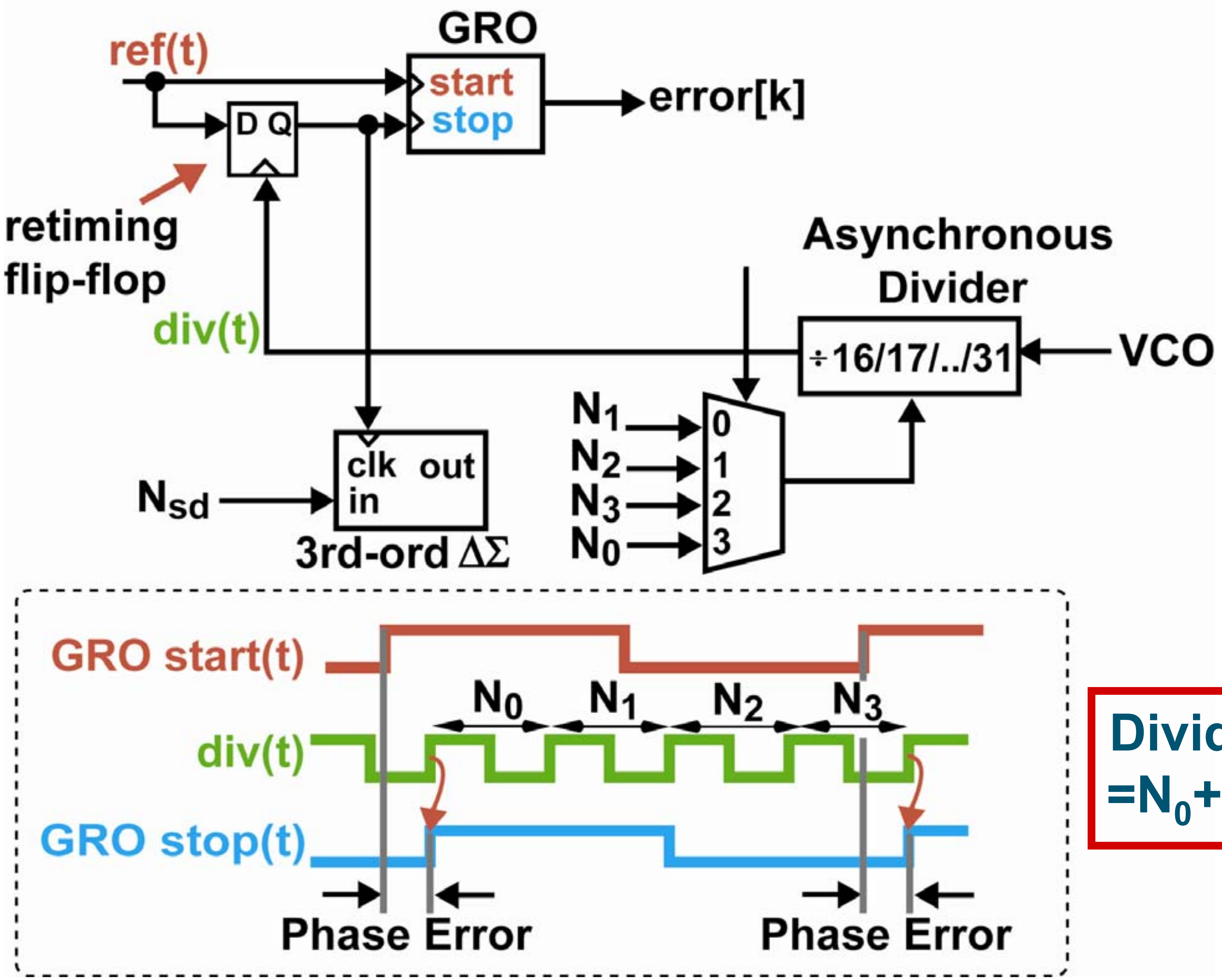
- **Step 2:** ***Disconnect Capacitors from Resistors, Then Connect Together***
  - **Achieves DAC output with first-order filtering**
  - **Bandwidth = 32• $C_u/(2\pi \cdot C_{load})$•50MHz**
    - Determined by capacitor ratio
    - Easily changed by using different C_{load}

Now Let's Examine Divider …



- **Issues:**
  - **GRO range must span entire reference period during initial lock-in**

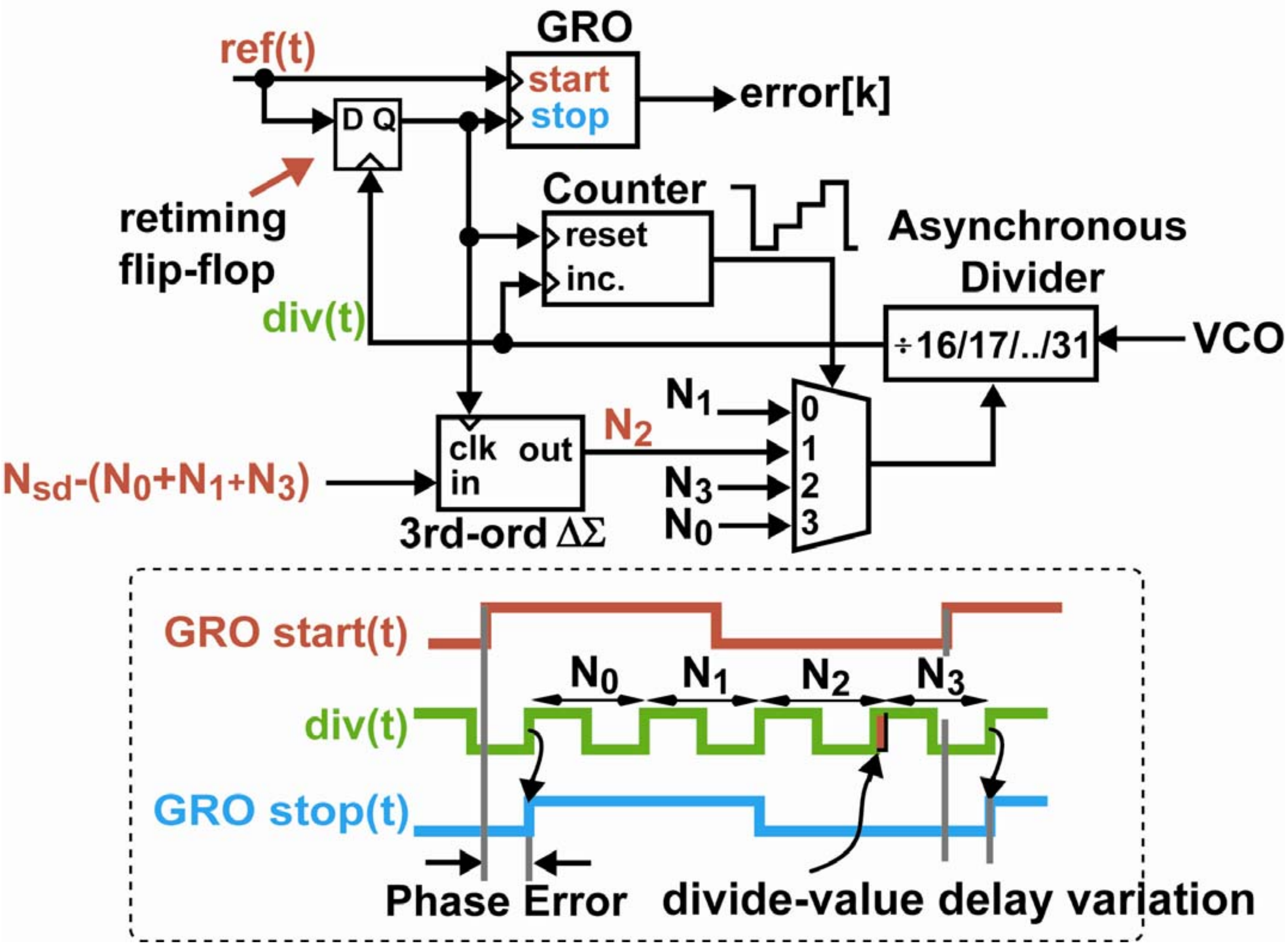
Proposed Divider Structure



Divide value $=N_0+N_1+N_2+N_3$

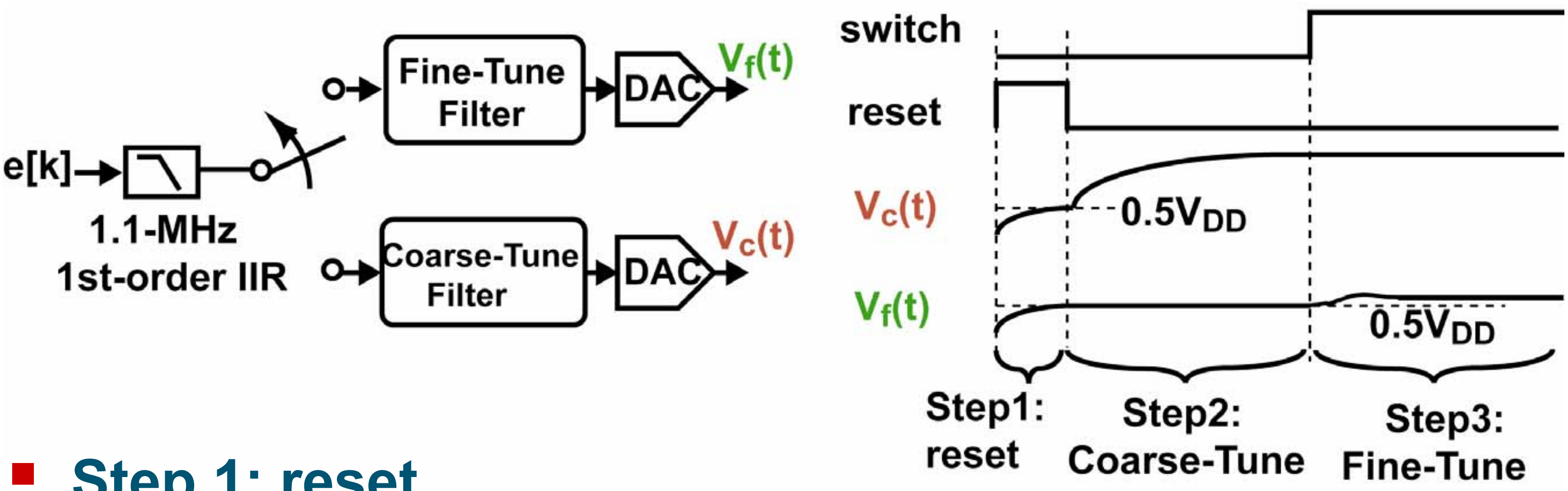
- **Resample reference with 4x division frequency**
  - **Lowers GRO range to one fourth of the reference period**

Proposed Divider Structure (cont'd)



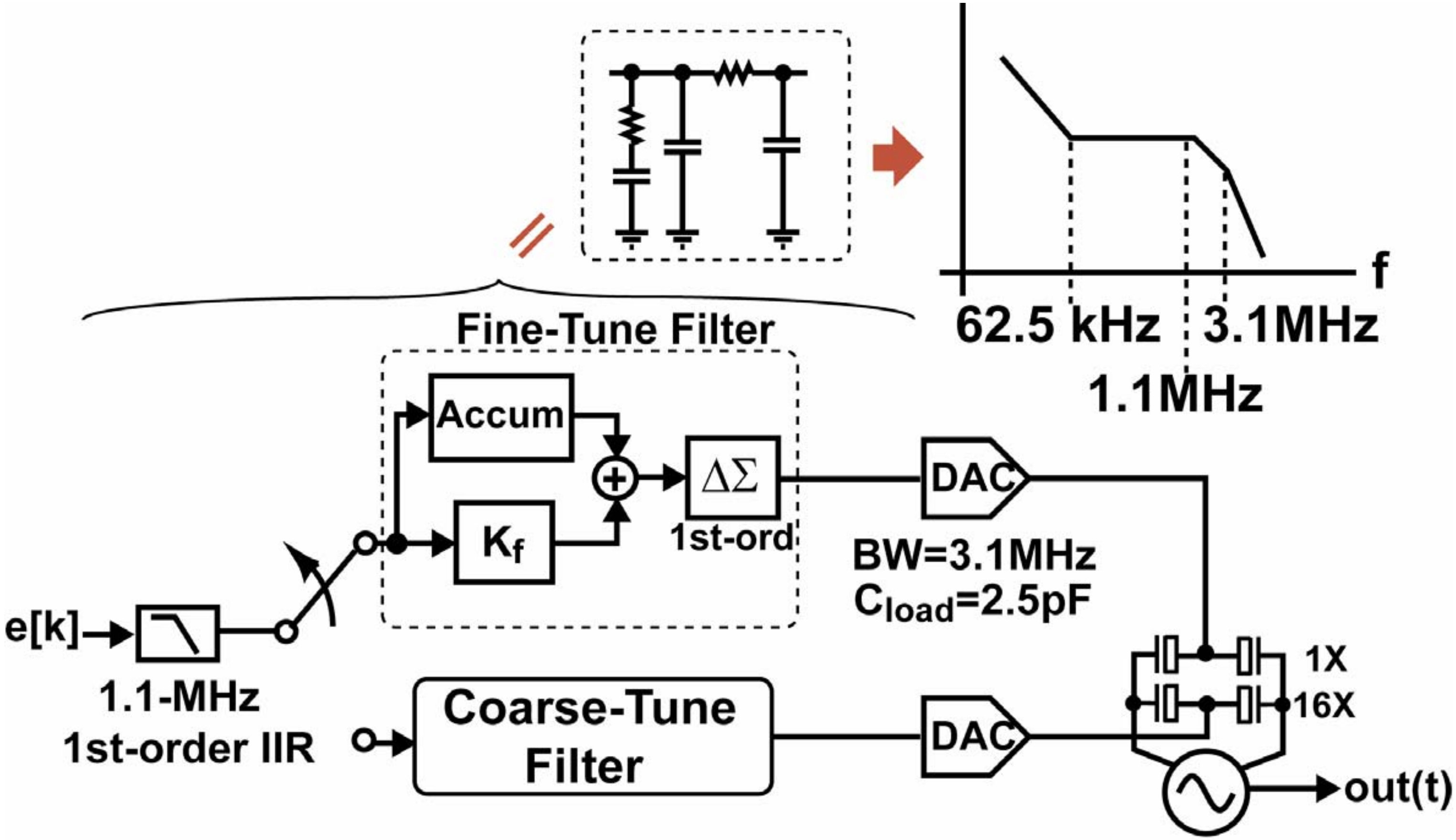
- **Place ΔΣ dithered edge away from GRO edge**
  - **Prevents extra jitter due to divide-value dependent delay**

Dual-Path Loop Filter



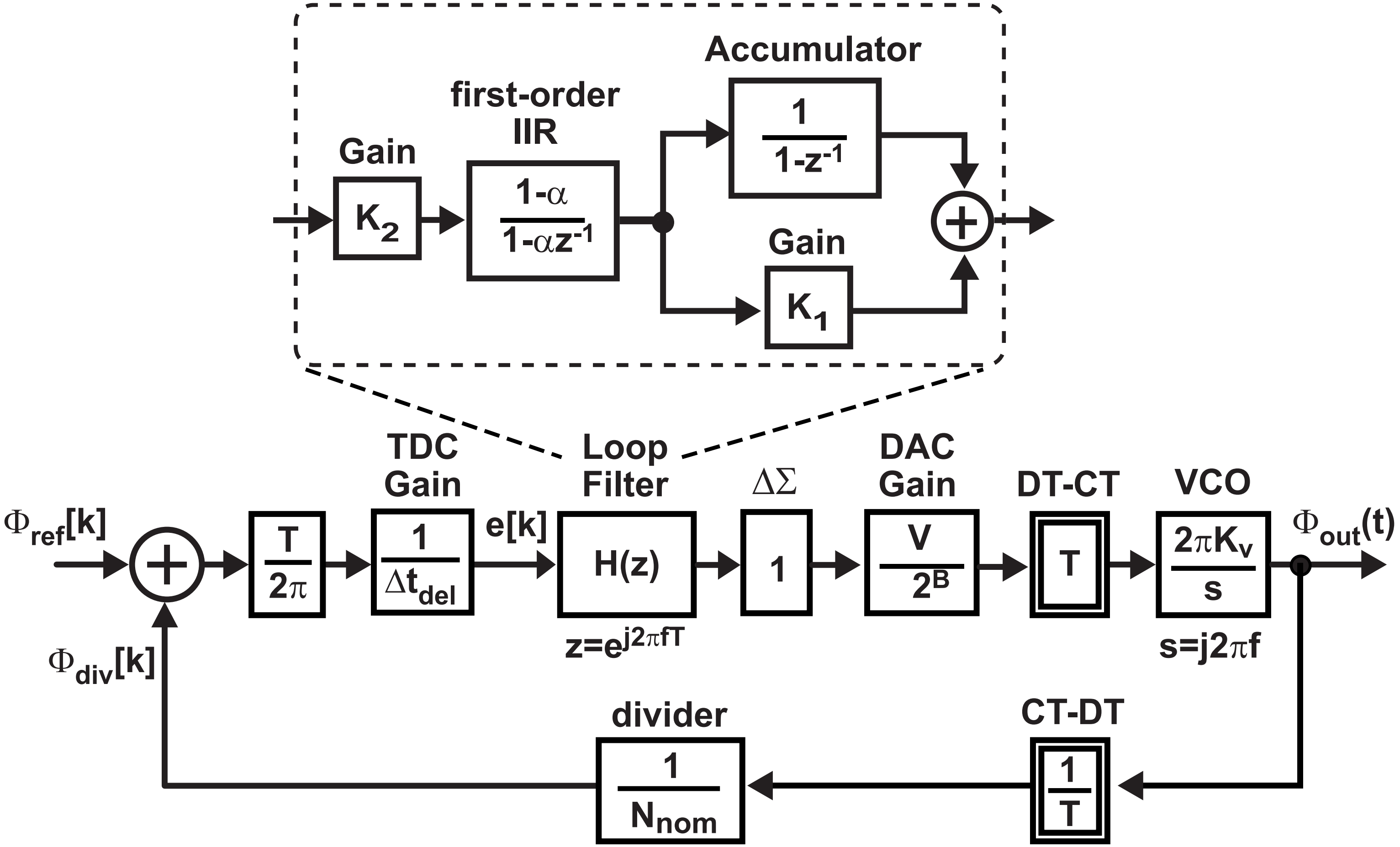
- Step 1: reset
- Step 2: frequency acquisition
  - $V_c(t)$ varies
  - $V_f(t)$ is held at midpoint
- Step 3: steady-state lock conditions
  - $V_c(t)$ is frozen to take quantization noise away
  - ΔΣ quantization noise cancellation is enabled

Fine-Path Loop Filter



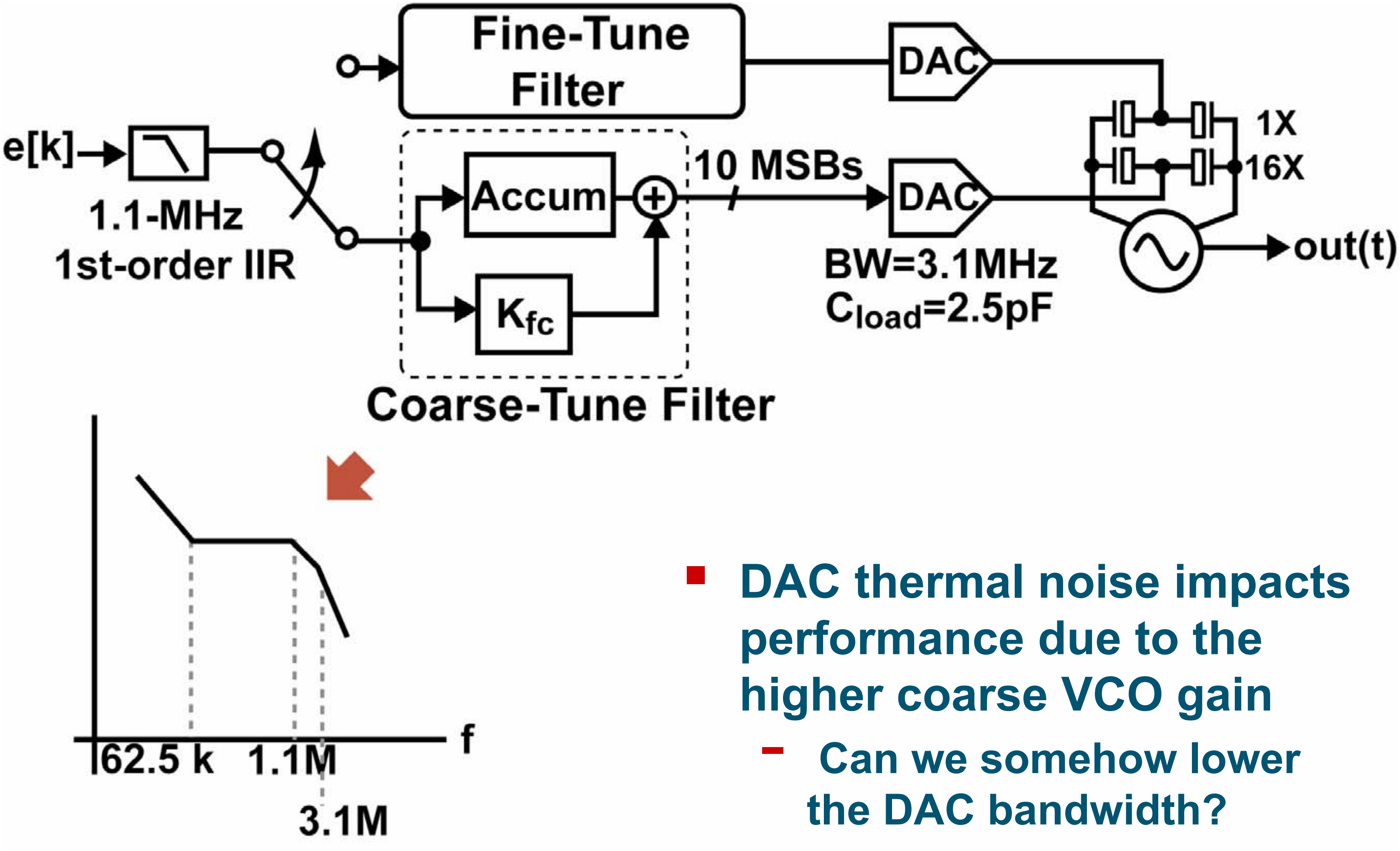
- Equivalent to an analog lead-lag filter
  - Set zero (62.5kHz) and first pole (1.1MHz) digitally
  - Set second pole (3.1MHz) by capacitor ratio
- First-order ΔΣ reduces in-band quantization noise

Linearized Model of PLL Under Fine-Tune Operation



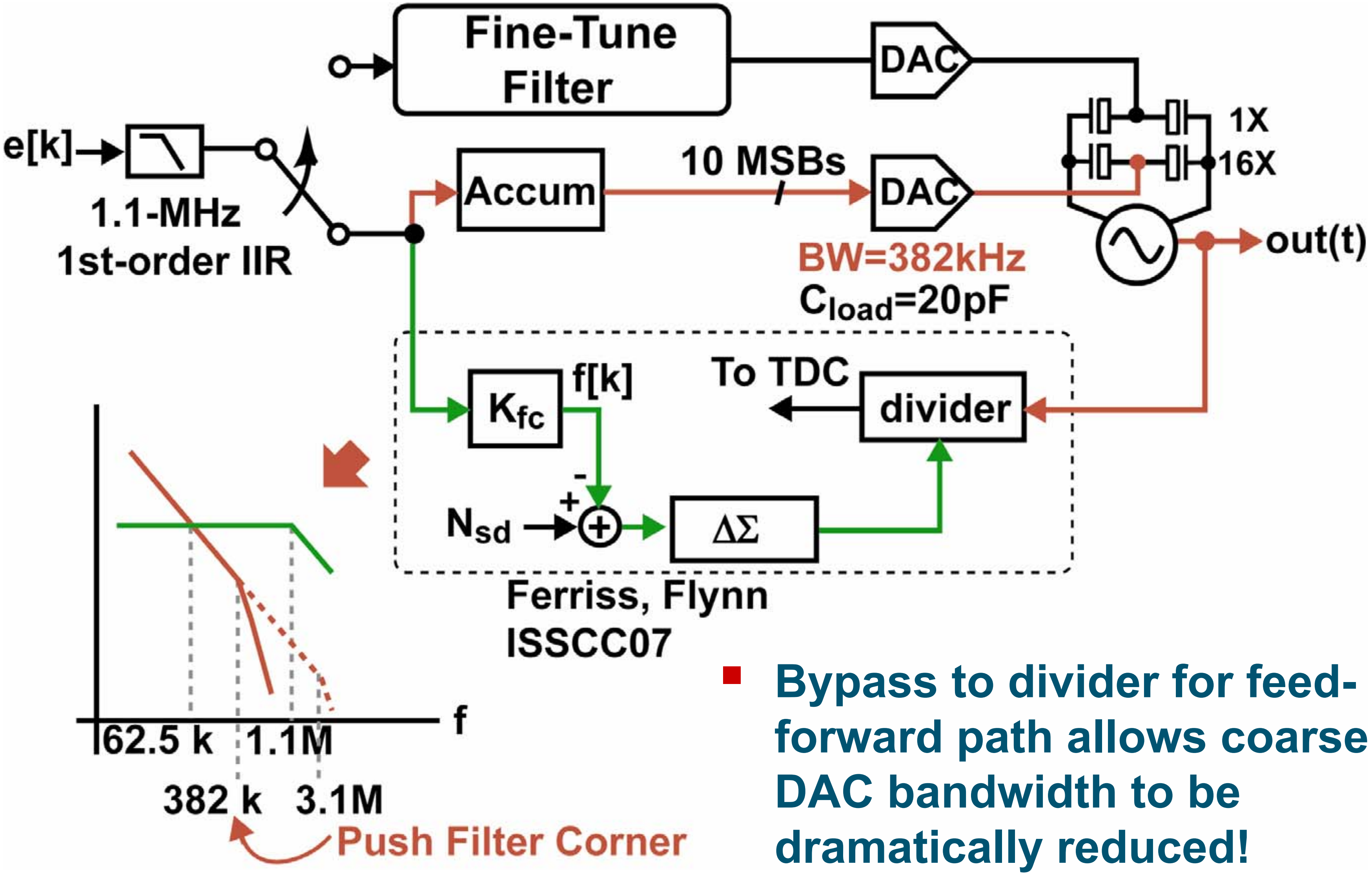
- **Standard lead-lag filter topology but implemented in digital domain**
  - **Consists of accumulator plus feedforward path**

Same Technique Poses Problems for Coarse-Tune



- DAC thermal noise impacts performance due to the higher coarse VCO gain
  - Can we somehow lower the DAC bandwidth?

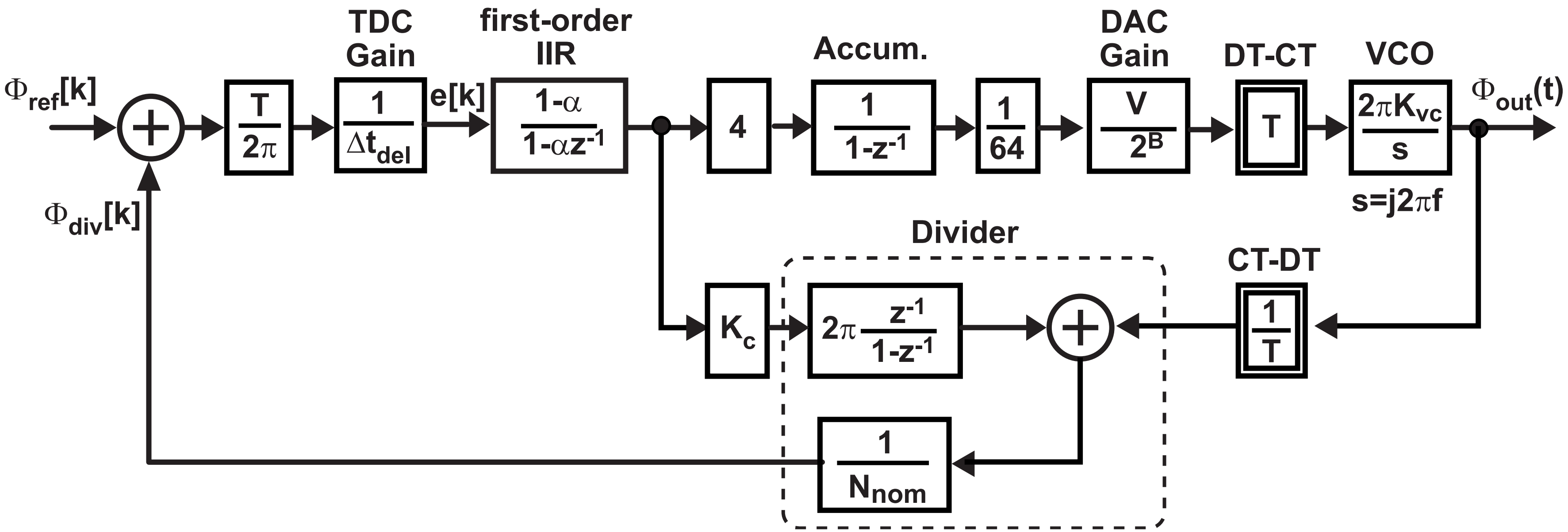
Fix: Leverage the Divider as a Signal Path



Ferriss, Flynn ISSCC07

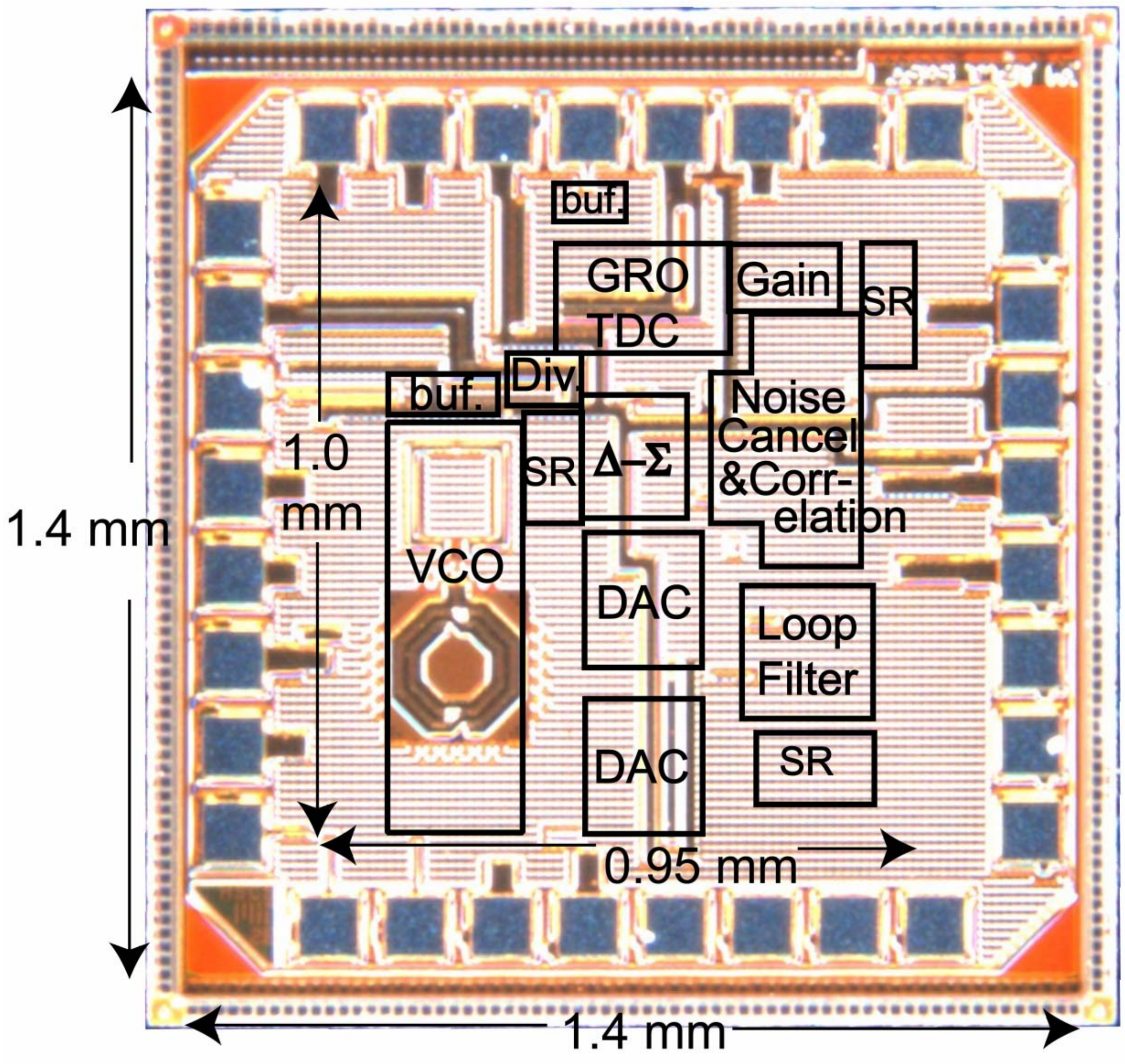
- Bypass to divider for feed-forward path allows coarse DAC bandwidth to be dramatically reduced!

Linearized Model of PLL Under Coarse-Tune Operation



- **Routing of signal path into Sigma-Delta controlling the divider yields a feedforward path**
  - **Adds to accumulator path as both signals pass back through the divider**
  - **Allows reduction of coarse DAC bandwidth**
    - Noise impact of coarse DAC on VCO is substantially lowered

Die Photo of Prototype

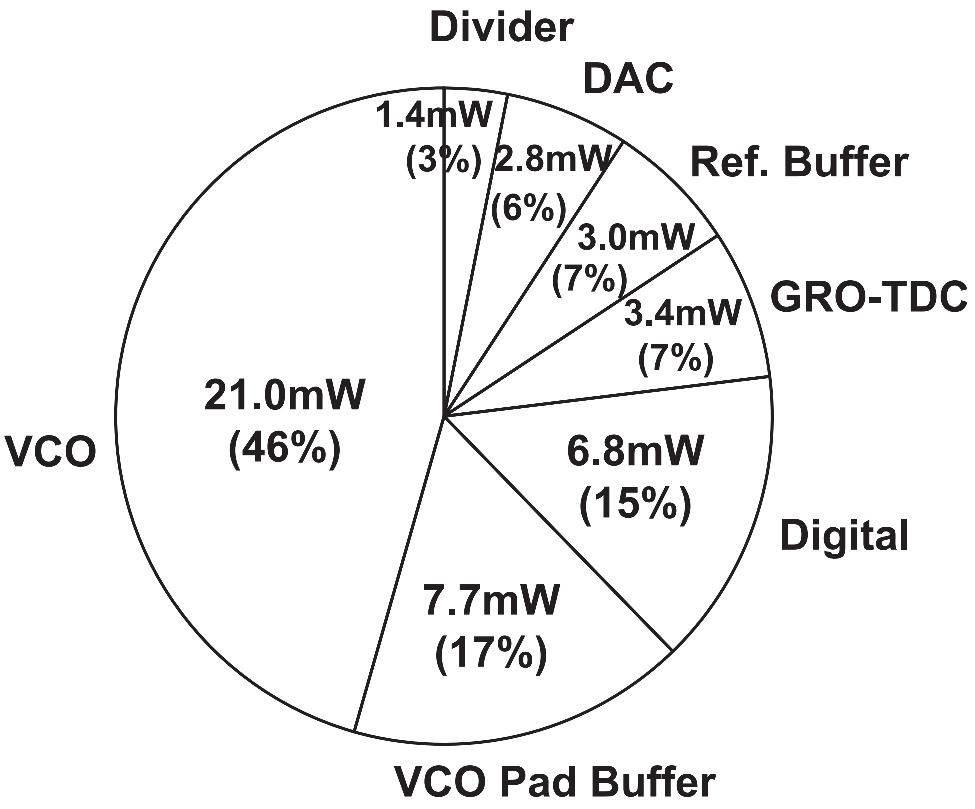


- 0.13-µm CMOS
- Active area: 0.95 mm^2
- Chip area: 1.96 mm^2
- V_{DD}: 1.5V
- Current:
  - 26mA (Core)
  - 7mA (VCO output buffer at 1.1V)

GRO-TDC:

- 2.3mA
- 157X252 um^2

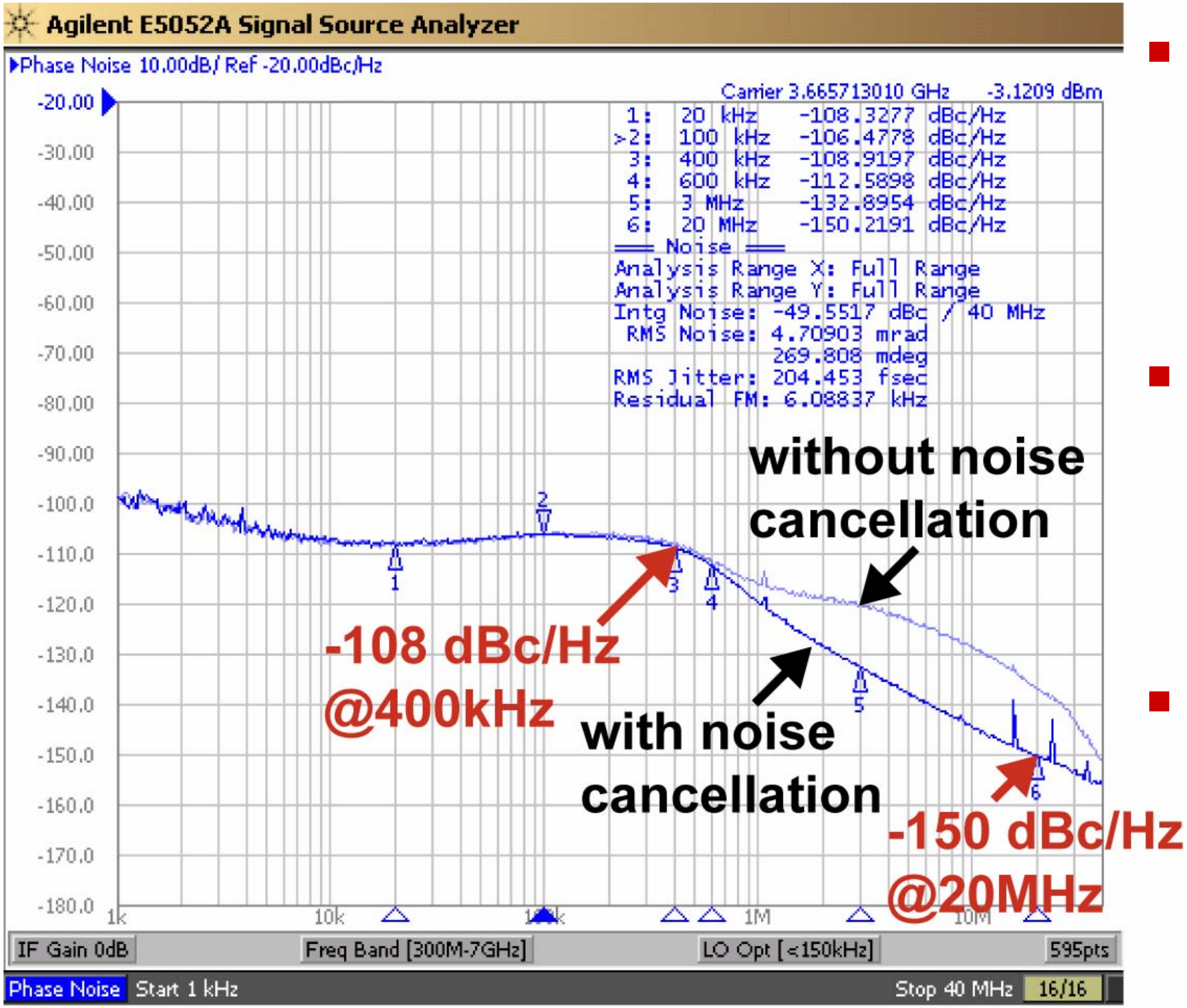
Power Distribution of Prototype IC



Total Power: 46.1mW

- Notice GRO and digital quantization noise cancellation have only minor impact on power (and area)

Measured Phase Noise at 3.67GHz



```
Agilent E5052A Signal Source Analyzer
▸Phase Noise 10.00dB/ Ref -20.00dBc/Hz
                         Carrier 3.665713010 GHz    -3.1209 dBm
 1:  20  kHz    -108.3277 dBc/Hz
>2:  100 kHz    -106.4778 dBc/Hz
 3:  400 kHz    -108.9197 dBc/Hz
 4:  600 kHz    -112.5898 dBc/Hz
 5:   3  MHz    -132.8954 dBc/Hz
 6:  20  MHz    -150.2191 dBc/Hz
══ Noise ══
Analysis Range X: Full Range
Analysis Range Y: Full Range
Intg Noise: -49.5517 dBc / 40 MHz
 RMS Noise: 4.70903 mrad
            269.808 mdeg
RMS Jitter: 204.453 fsec
Residual FM: 6.08837 kHz
```

IF Gain 0dB | Freq Band [300M-7GHz] | LO Opt [<150kHz] | 595pts

Phase Noise | Start 1 kHz | Stop 40 MHz | 16/16

without noise cancellation

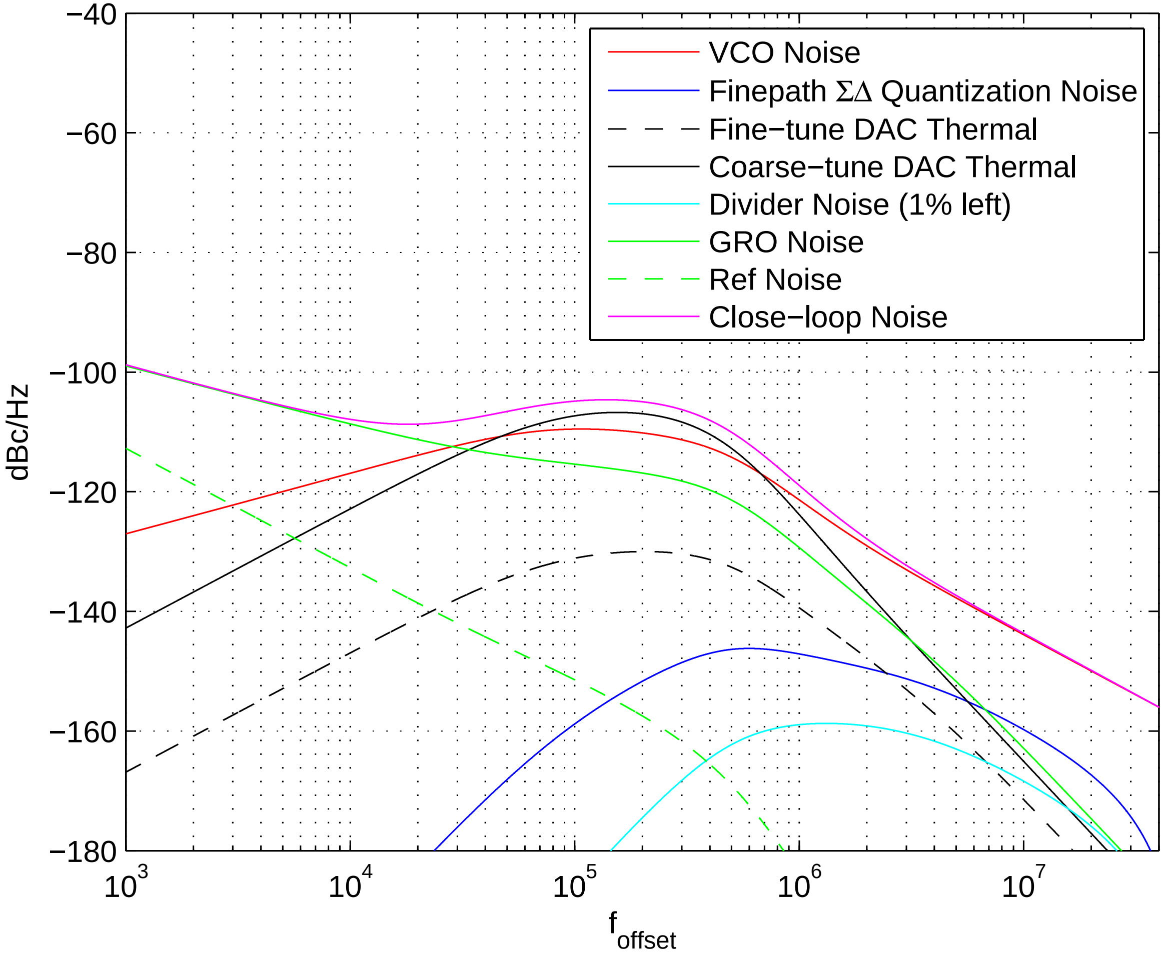
with noise cancellation

-108 dBc/Hz @400kHz

-150 dBc/Hz @20MHz

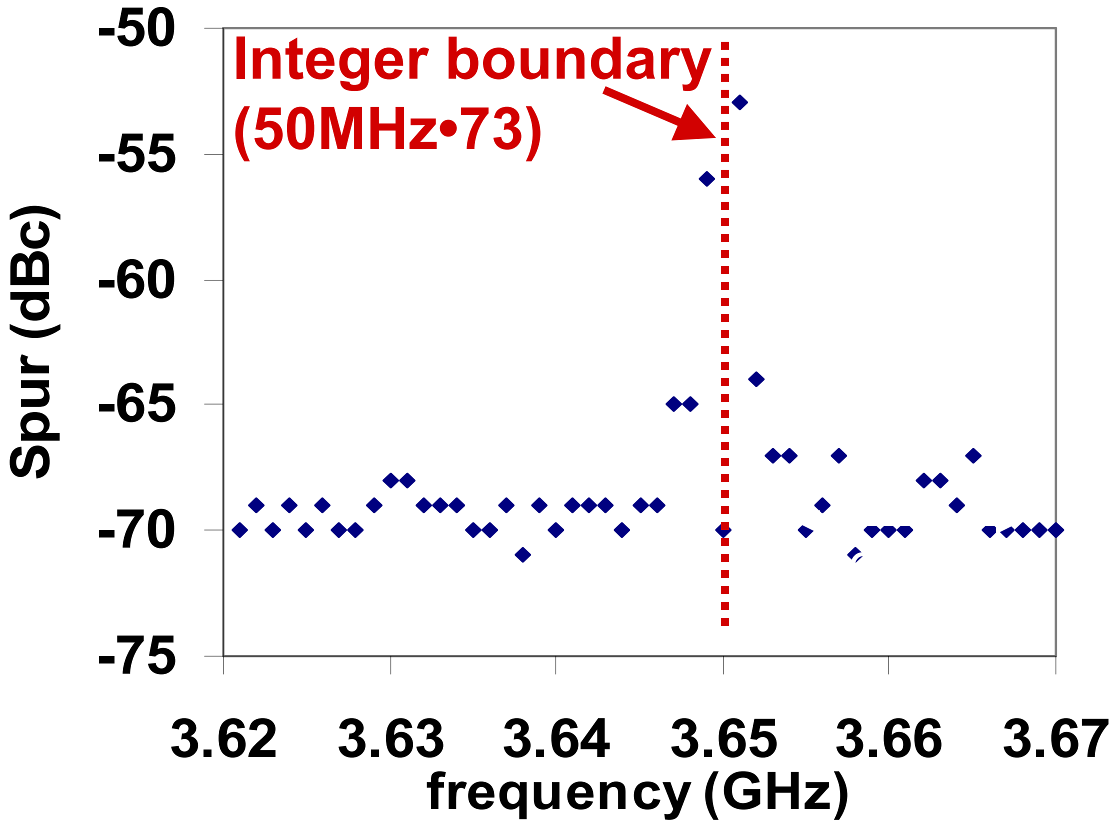
- Suppresses quantization noise by more than 15 dB
- Achieves 204 fs (0.27 degree) integrated noise (jitter)
- Reference spur: -65dBc

Calculation of Phase Noise Components



- **See wideband digital synthesizer tutorial available at http://www.cppsim.com**

Measured Worst Spurs over Fifty Channels



- Tested from 3.620 GHz to 3.670 GHz at intervals of 1 MHz
  - Worst spurs observed close to integer-N boundary (multiples of 50 MHz)
- -42dBc worst spur observed at 400kHz offset from boundary

Conclusions

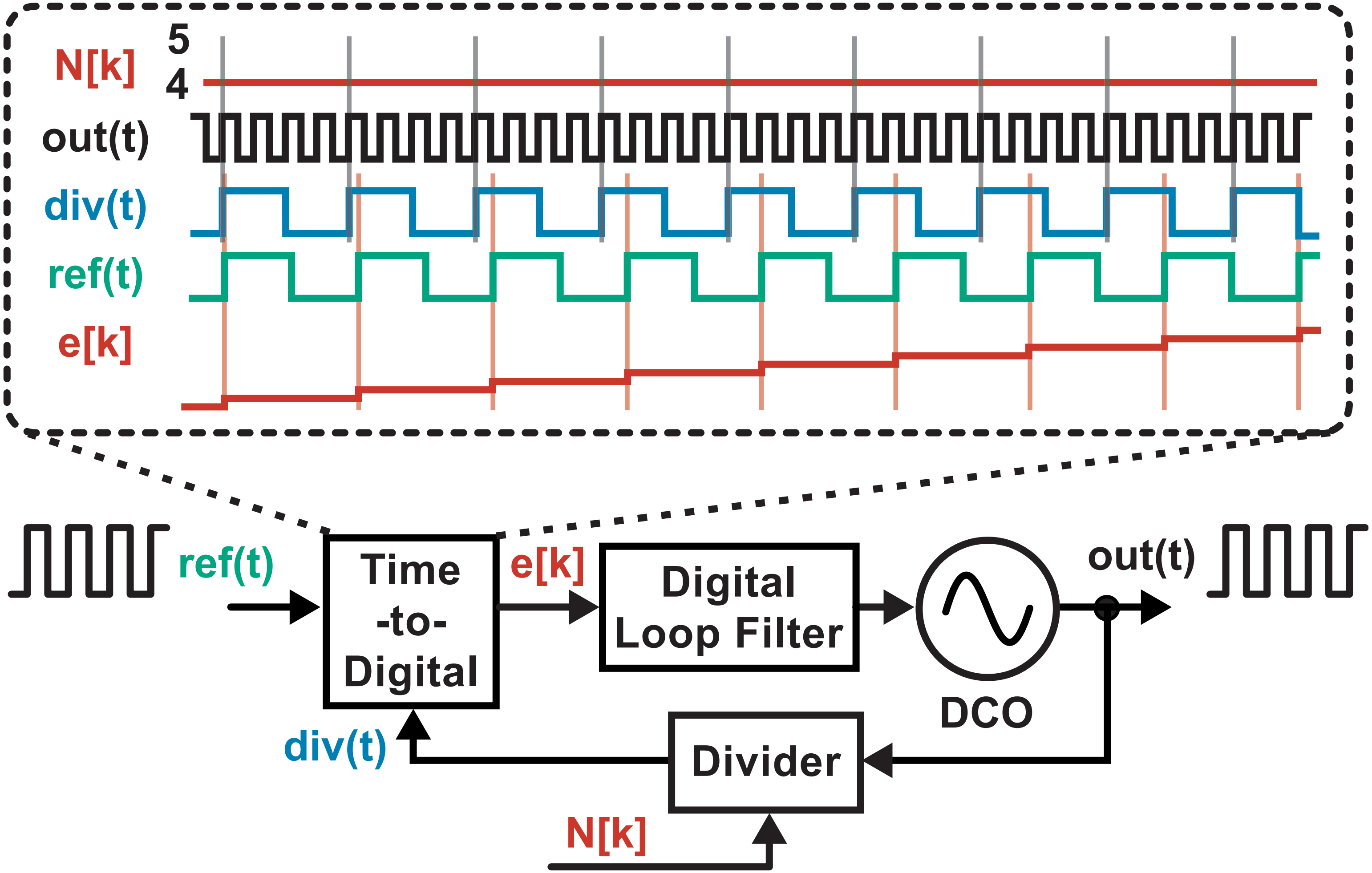
- **Digital Phase-Locked Loops look extremely promising for future applications**
  - **Very amenable to future CMOS processes**
  - **Excellent performance can be achieved**
- **Analysis of digital PLLs is similar to analog PLLs**
  - **PLL bandwidth is often chosen for best noise performance**
    - TDC (or Ref) noise dominates at low frequency offsets
    - DCO noise dominates at high frequency offsets
- **Behavioral simulation tools such as CppSim allow architectural investigation and validation of calculations**
- **TDC structures are an exciting research area**
  - **Ideas from A-to-D conversion can be applied**

Innovation of future digital PLLs will involve joint circuit/algorithm development

Supplemental Slides

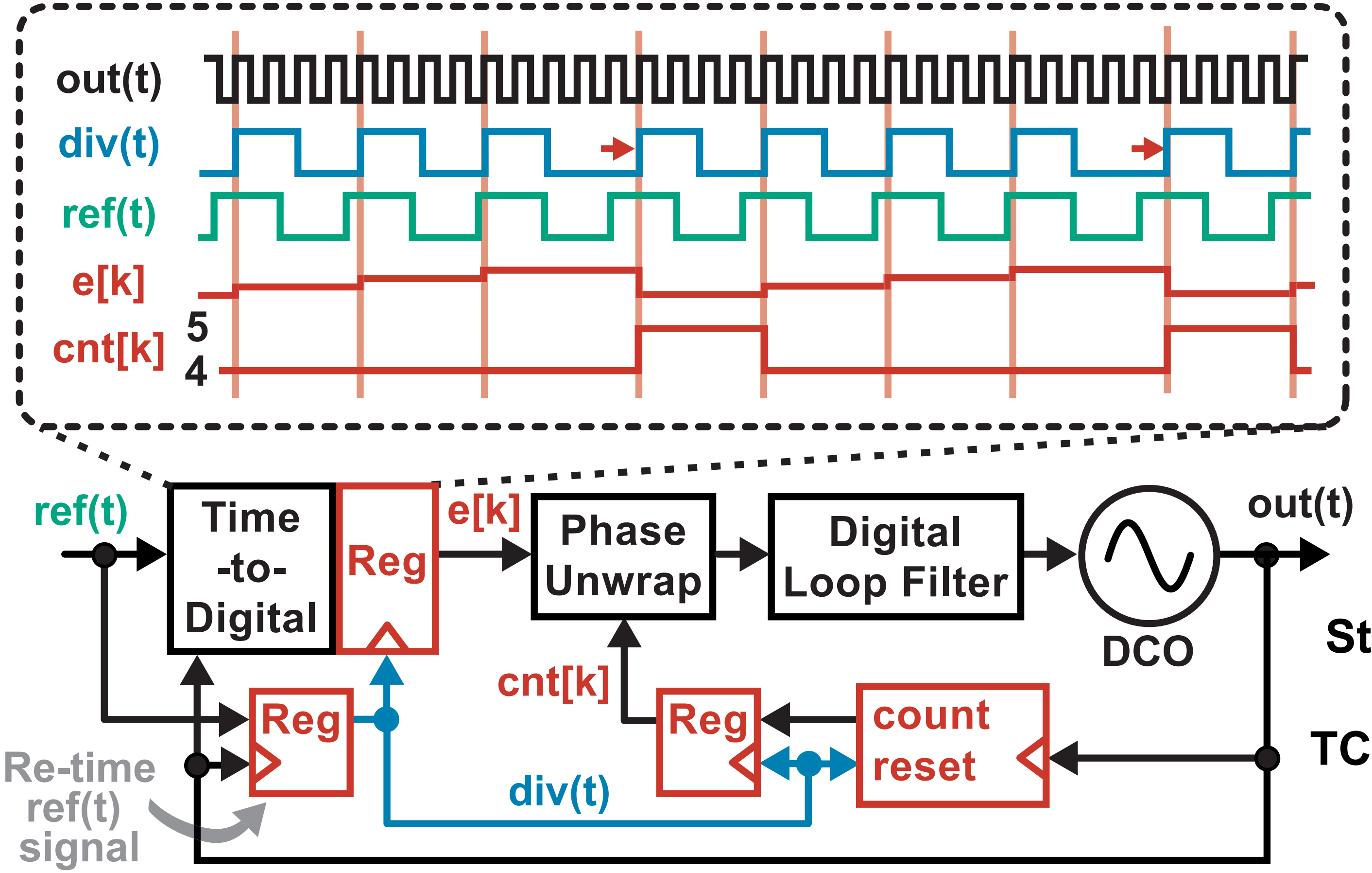
Section 1: Digital Fractional-N Frequency Synthesizers

A First Glance at Fractional-N Signals (F_{out} = 4.25F_{ref})



- Constant *divide value* of *N* = 4 leads to frequency error
  - Phase error accumulates in unbounded manner

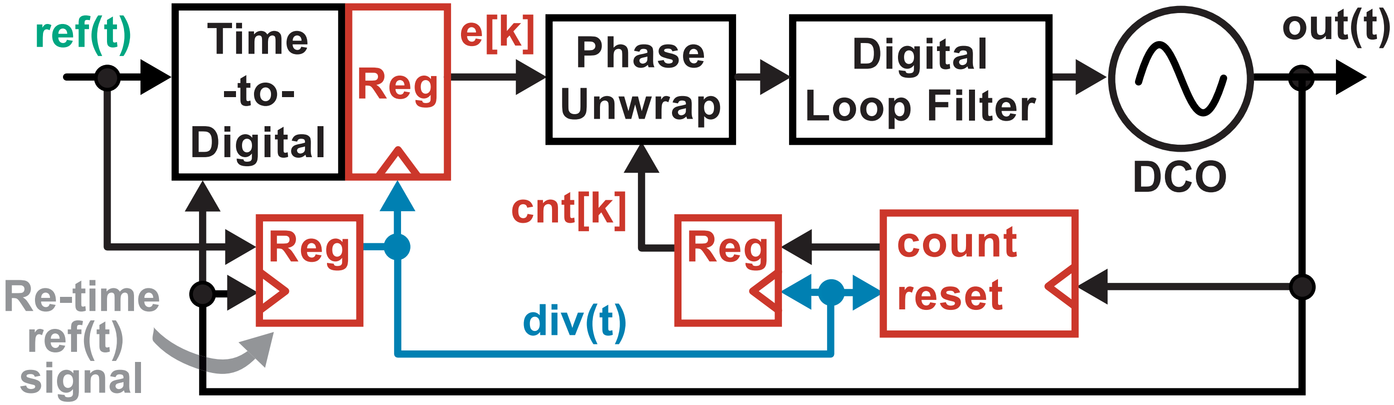
TI Approach to Fractional Division



Staszewski et. al., TCAS II, Nov 2003

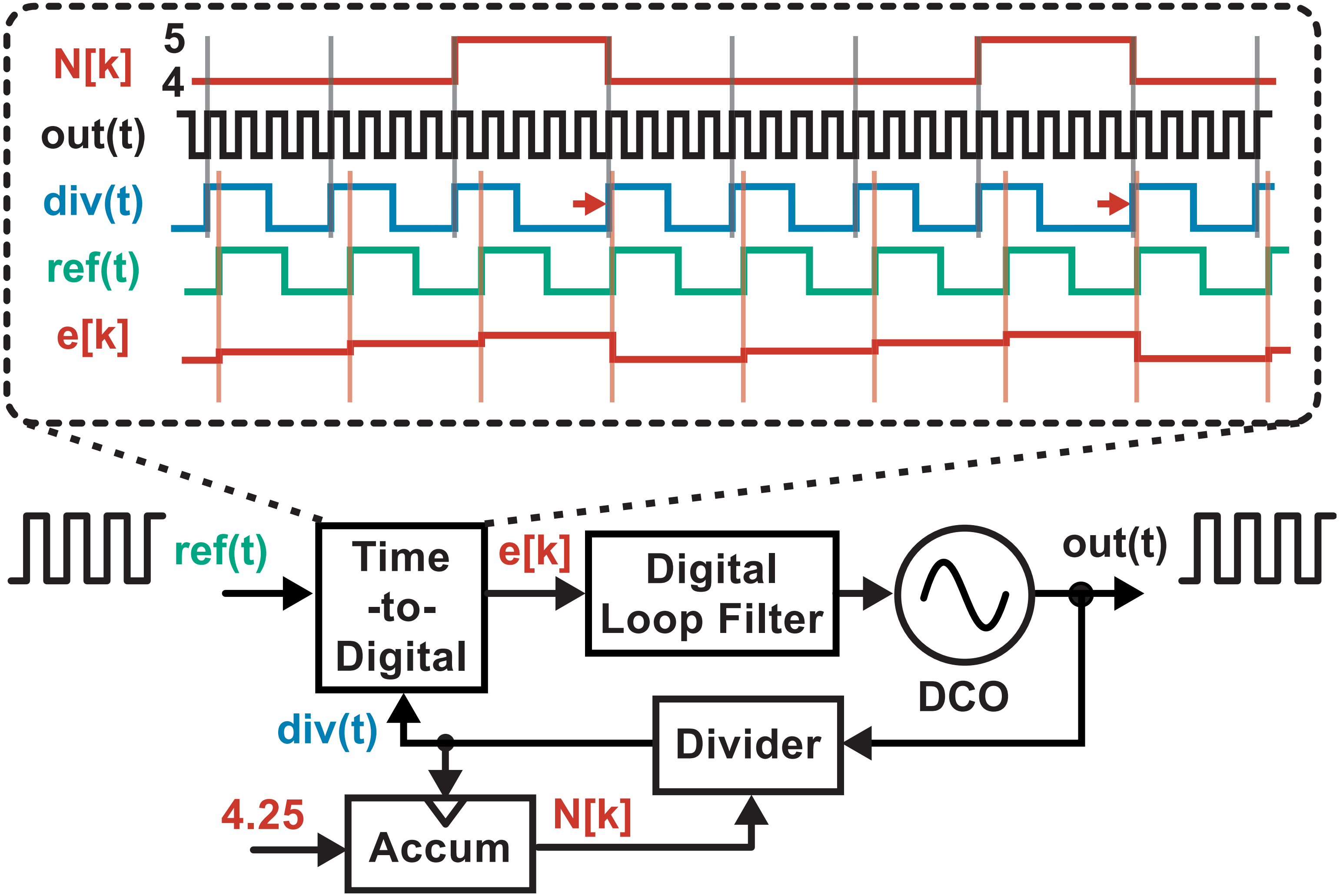
- Wrap *e[k]* by feeding delay chain in TDC with *out(t)*
- Counter provides information of *when* wrapping occurs

Key Issues



- Counter, re-timing register, and delay stages of TDC must operate at very high speeds
  - Power consumption can be an issue
- Calibration of TDC scale factor required to achieve proper unwrapping of *e[k]*
  - Can be achieved continuously with relative ease
    - See Staszewski et. al, JSSC, Dec 2005

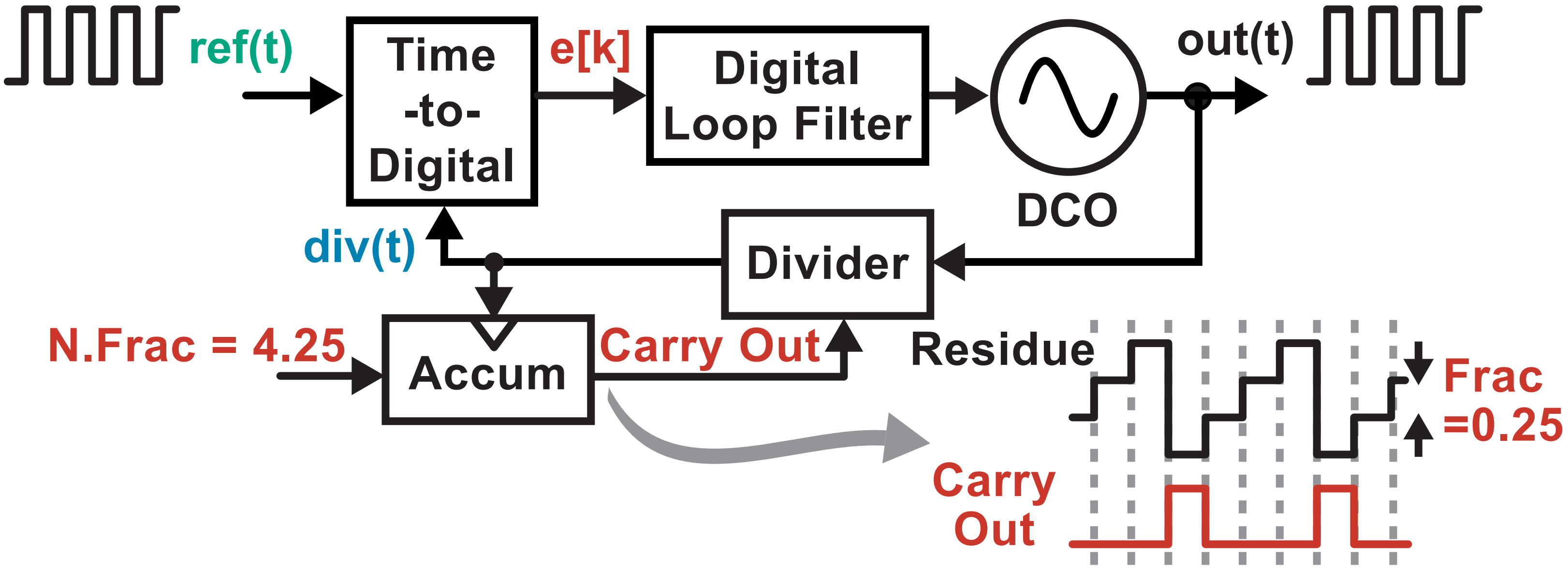
Fractional-N Synthesizer Approach (F_{out} = 4.25F_{ref})



- **Accumulator guides the “swallowing” of VCO cycles**
  - **Average divide value of *N* = 4.25 is achieved in this case**

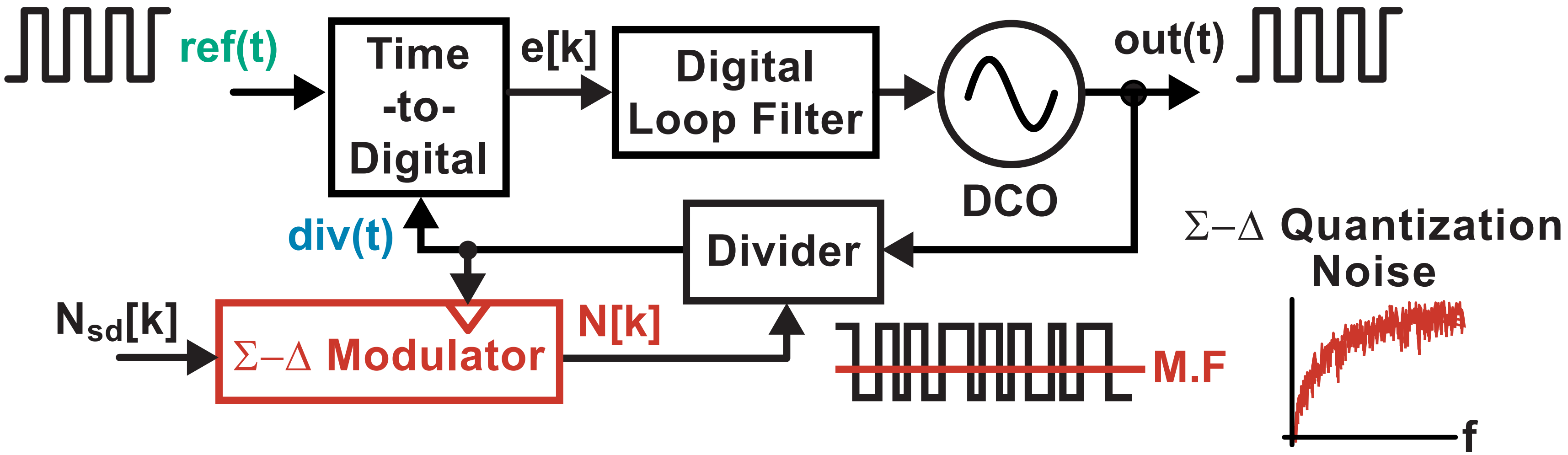
The Accumulator as a Phase "Observer"

- Accumulator residue corresponds to an estimate of the instantaneous phase error of the PLL
  - Fractional value (i.e., 0.25) yields the slope of the residue
- Carry out signal is asserted when the phase error deviation (i.e. residue) exceeds one VCO cycle
  - Carry out signal accurately predicts when a VCO cycle should be "swallowed"

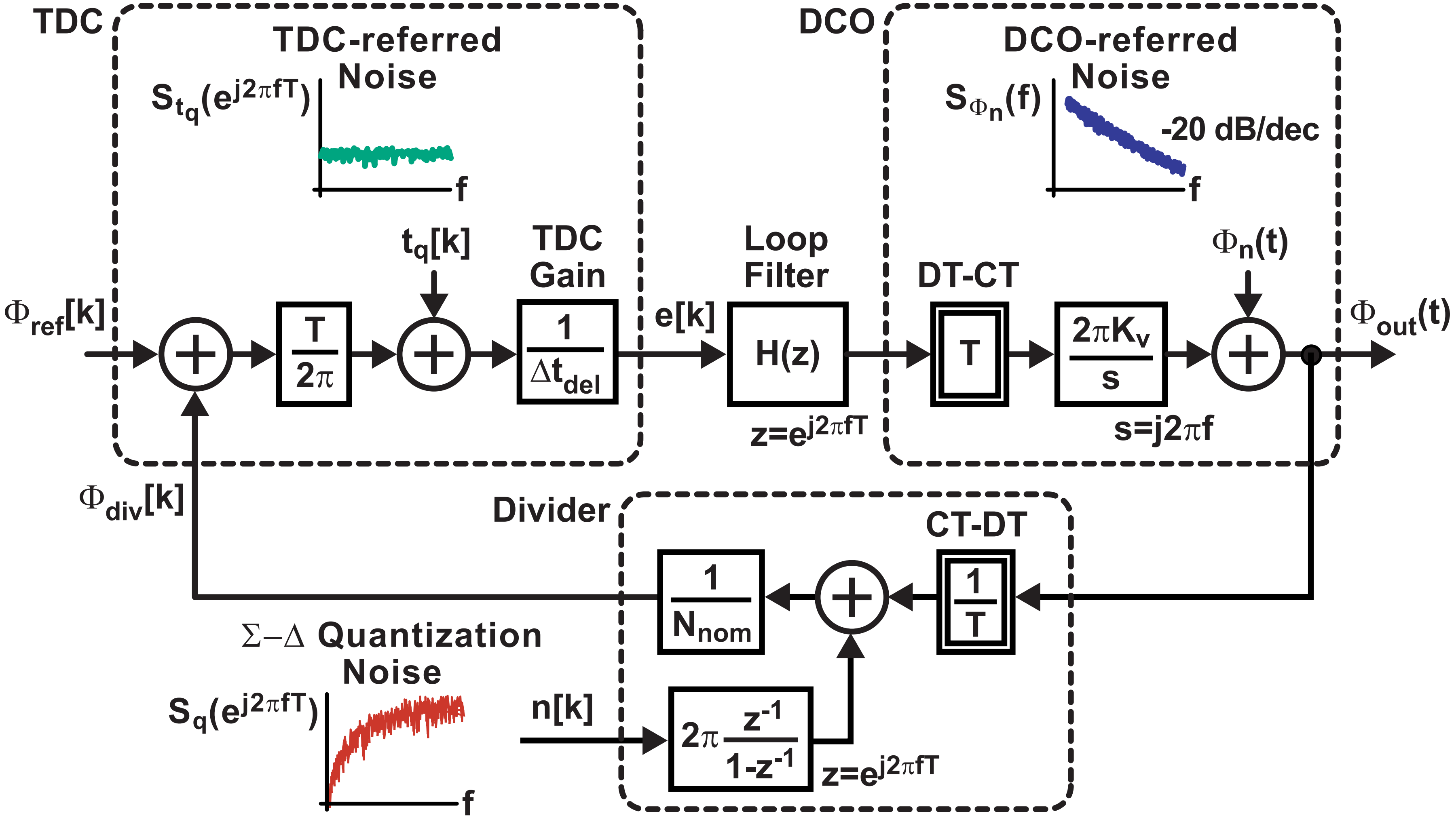


Improve Dithering Using Sigma-Delta Modulation

- Provides improved noise performance over accumulator-based divide value dithering
  - Dramatic reduction of spurious noise
  - Noise shaping for improved in-band noise
  - Maintains bounded phase error signal
- Digital Σ–Δ fractional-N synthesizer architecture is directly analogous to analog Σ–Δ fractional-N synth.

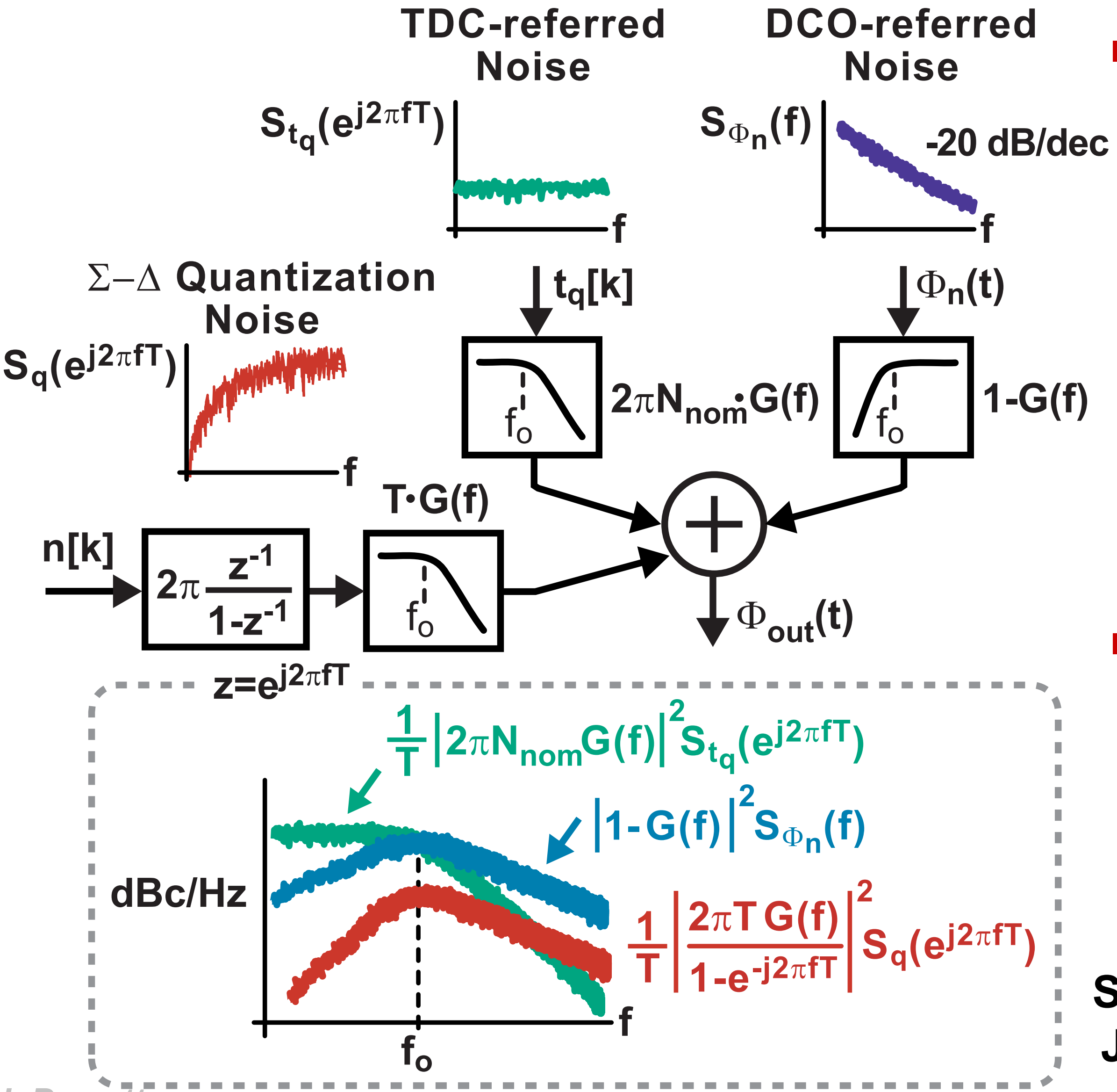


Model of Digital Σ–Δ Fractional-N PLL



- **Divider model is expanded to include the impact of divide value variations**

Transfer Function View of Digital Σ–Δ Fractional-N PLL

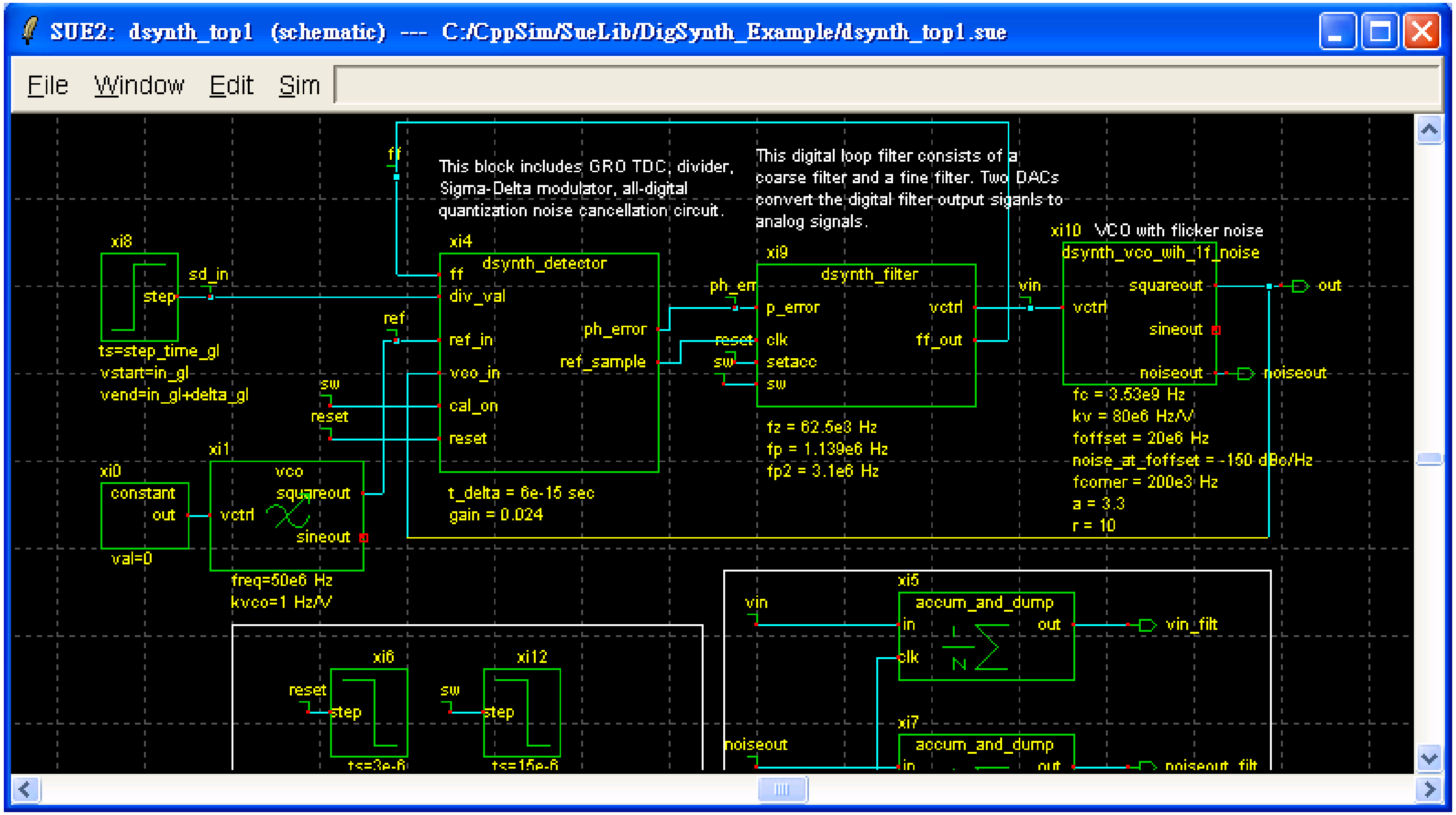


TDC-referred Noise
DCO-referred Noise
$S_{t_q}(e^{j2\pi fT})$
f
$S_{\Phi_n}(f)$
-20 dB/dec
f
Σ–Δ Quantization Noise
$S_q(e^{j2\pi fT})$
f
$t_q[k]$
$\Phi_n(t)$
f_o
$2\pi N_{nom} \cdot G(f)$
f_o
1-G(f)
T·G(f)
n[k]
$2\pi \frac{z^{-1}}{1-z^{-1}}$
f_o
$\Phi_{out}(t)$
$z=e^{j2\pi fT}$
$\frac{1}{T}\left|2\pi N_{nom} G(f)\right|^2 S_{t_q}(e^{j2\pi fT})$
$\left|1-G(f)\right|^2 S_{\Phi_n}(f)$
dBc/Hz
$\frac{1}{T}\left|\frac{2\pi T\, G(f)}{1-e^{-j2\pi fT}}\right|^2 S_q(e^{j2\pi fT})$
f
f_o

- Σ–Δ quantization noise now impacts the overall PLL phase noise
  - High PLL bandwidth will increase its impact
- Digital PLL implementation simplifies quantization noise cancellation

See: Hsu, Straayer, Perrott JSSC Dec 2008 for details

For More Information on Digital Fractional-N PLLs



SUE2: dsynth_top1 (schematic) --- C:/CppSim/SueLib/DigSynth_Example/dsynth_top1.sue

This block includes GRO TDC, divider, Sigma-Delta modulator, all-digital quantization noise cancellation circuit.

This digital loop filter consists of a coarse filter and a fine filter. Two DACs convert the digital filter output siganls to analog signals.

xi10 VCO with flicker noise

ts=step_time_gl
vstart=in_gl
vend=in_gl+delta_gl

val=0

freq=50e6 Hz
kvco=1 Hz/V

t_delta = 6e-15 sec
gain = 0.024

fz = 62.5e3 Hz
fp = 1.139e6 Hz
fp2 = 3.1e6 Hz

fc = 3.53e9 Hz
kv = 80e6 Hz/V
foffset = 20e6 Hz
noise_at_foffset = -150 dBc/Hz
fcorner = 200e3 Hz
a = 3.3
r = 10

ts=3e-6
ts=15e-6

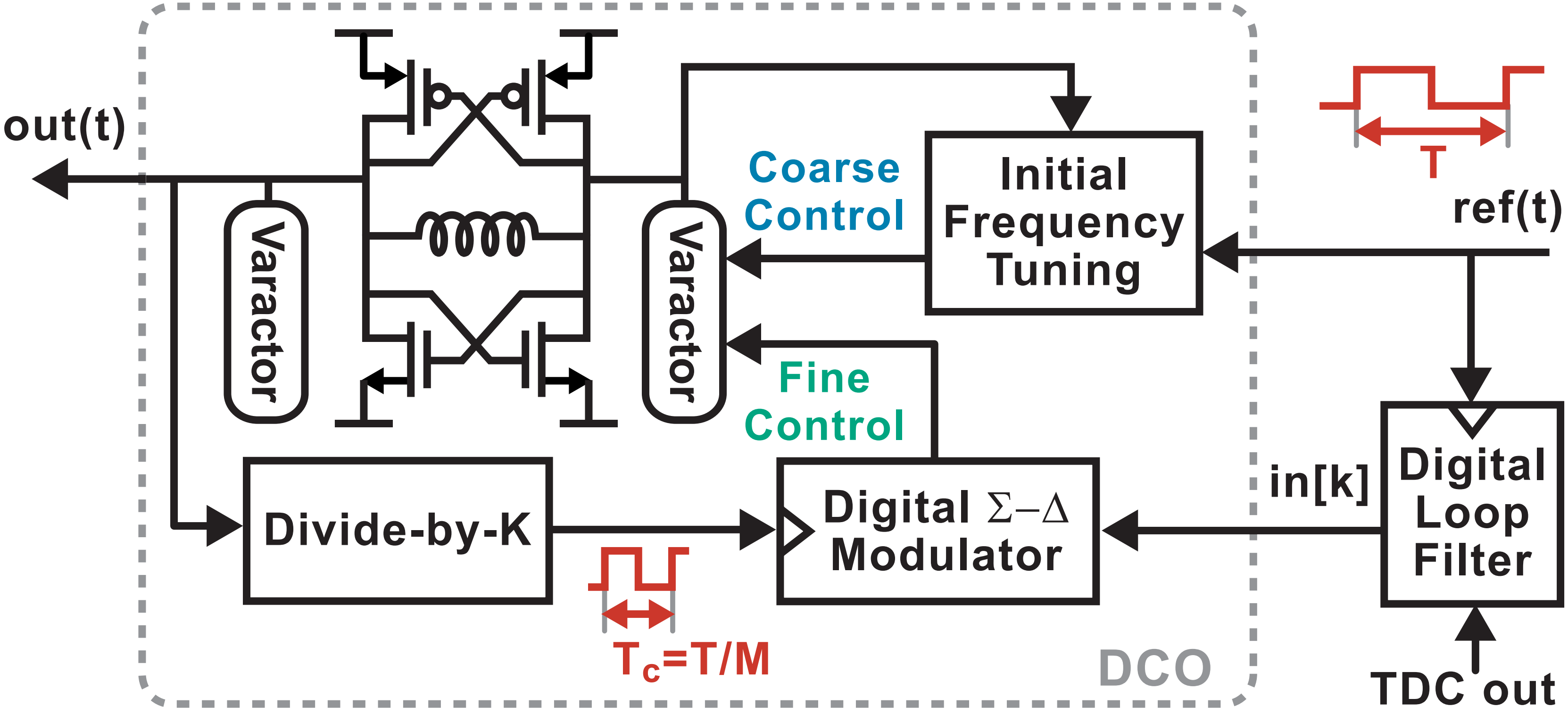
- **Check out the CppSim tutorial:**
  - **Design of a Low-Noise Wide-BW 3.6GHz Digital Σ–Δ Fractional-N Frequency Synthesizer Using the PLL Design Assistant and CppSim**

www.cppsim.com

Supplemental Slides

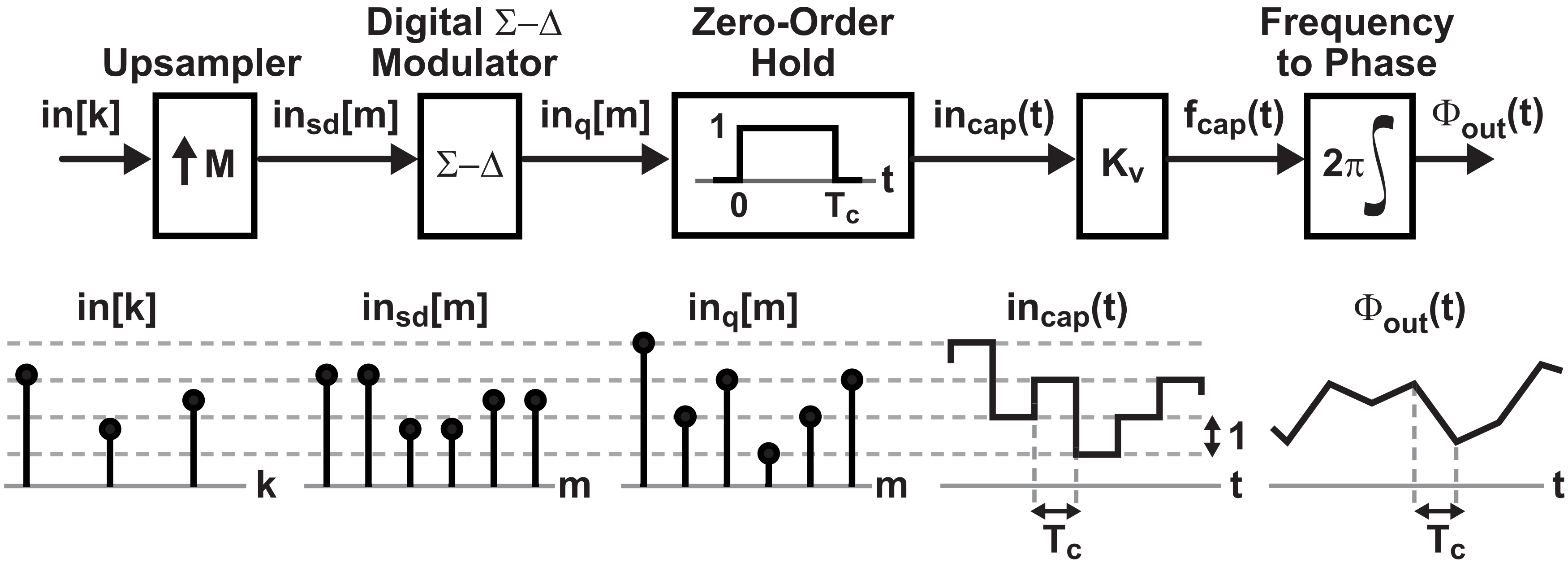
Section 2: DCO Modeling

Leveraging Dithering for Fine Control of DCO



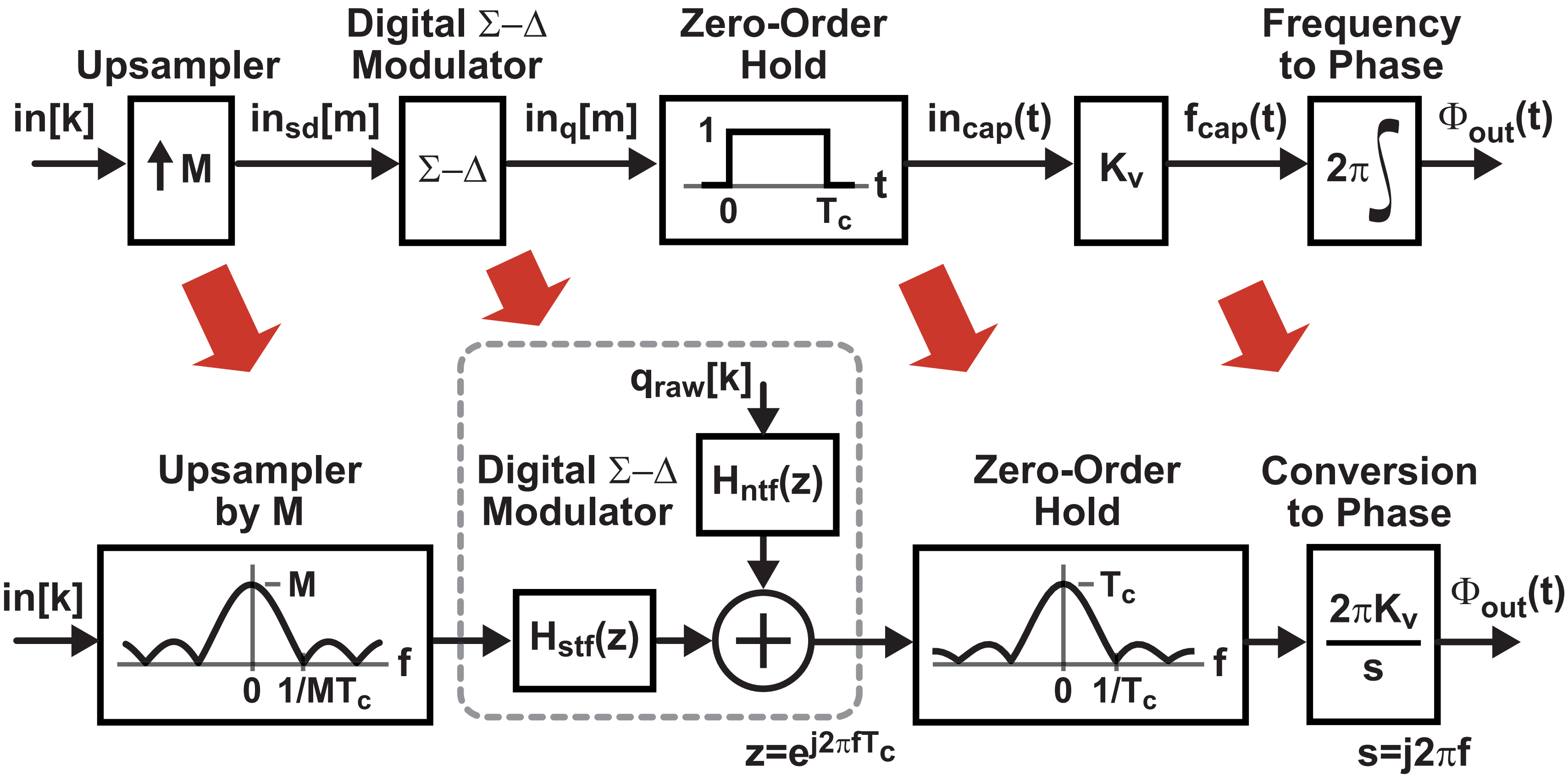
- Increase resolution by Σ–Δ dithering of fine cap array
- Reduce noise from dithering by
  - Using small unit caps in the fine cap array
  - Increasing the dithering frequency (defined as *$1/T_c$*)
    - We will assume *$1/T_c$ = M/T* (i.e. M times reference frequency)

Time-Domain Modeling of the DCO



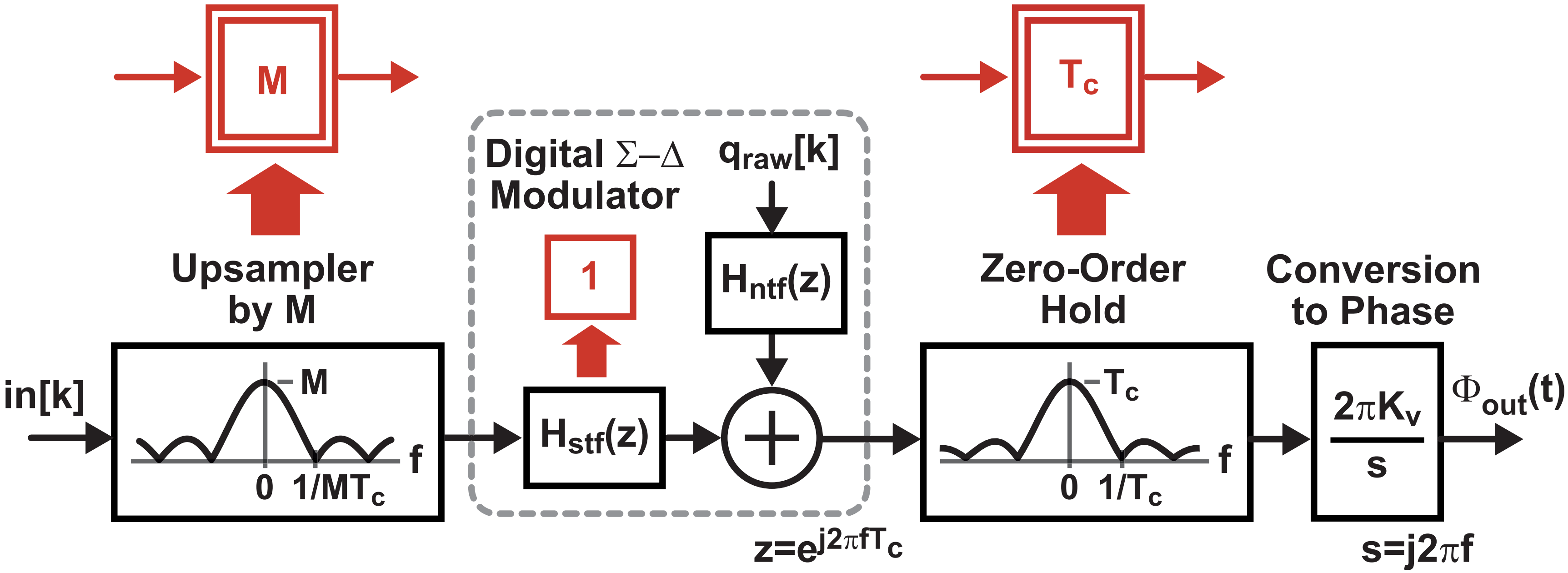
- **Input to the DCO is supplied by the loop filter**
  - **Clocked at *1/T* (i.e., reference frequency)**
- **Switched capacitors are dithered by Σ–Δ at a higher rate**
  - **Clocked at $1/T_c = M/T$**
  - **Held at a given setting for duration T_c**
- **Fine cap element value determines K_v of VCO**
  - **Units of K_v are Hz/unit cap**

Frequency Domain Modeling of DCO



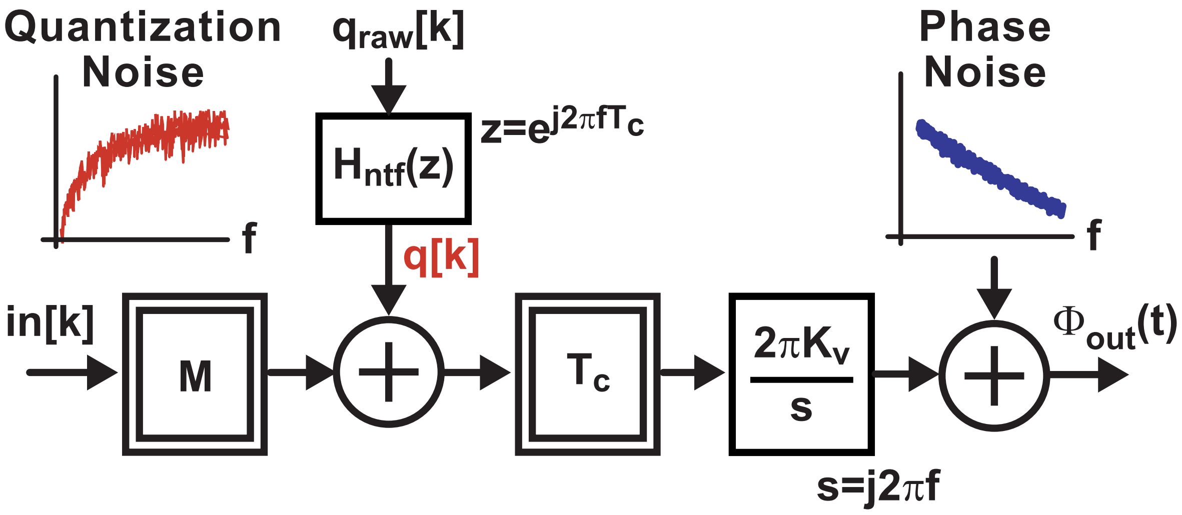
- Upsampler and zero-order hold correspond to discrete and continuous-time *sinc* functions, respectively
- Σ–Δ has signal and noise transfer functions ($H_{stf}(z)$, $H_{ntf}(z)$)
  - Note: $var(q_{raw}[k])$ = 1/12 (uniformly distributed from 0 to 1)

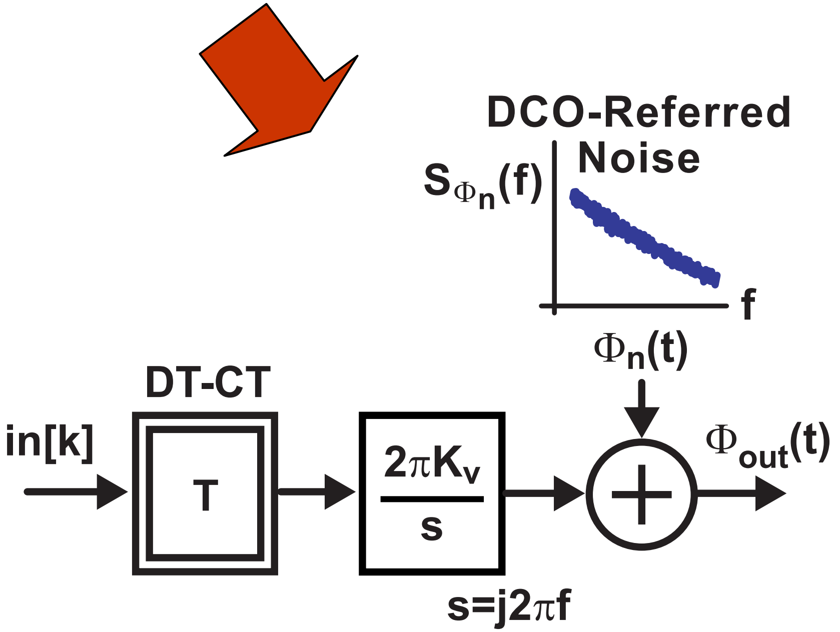
Simplification of the DCO Model



- **Focus on low frequencies for calculations to follow**
  - **Assume *sinc* functions are relatively flat at the low frequencies of interest**
    - Upsampler is approximated as a gain of *M*
    - Zero-order hold is approximated as a gain of T_c
- **Assume $H_{stf}(z) = 1$**
  - **True for Σ–Δ structures such as MASH (ignoring delays)**

Further Simplification of DCO Model



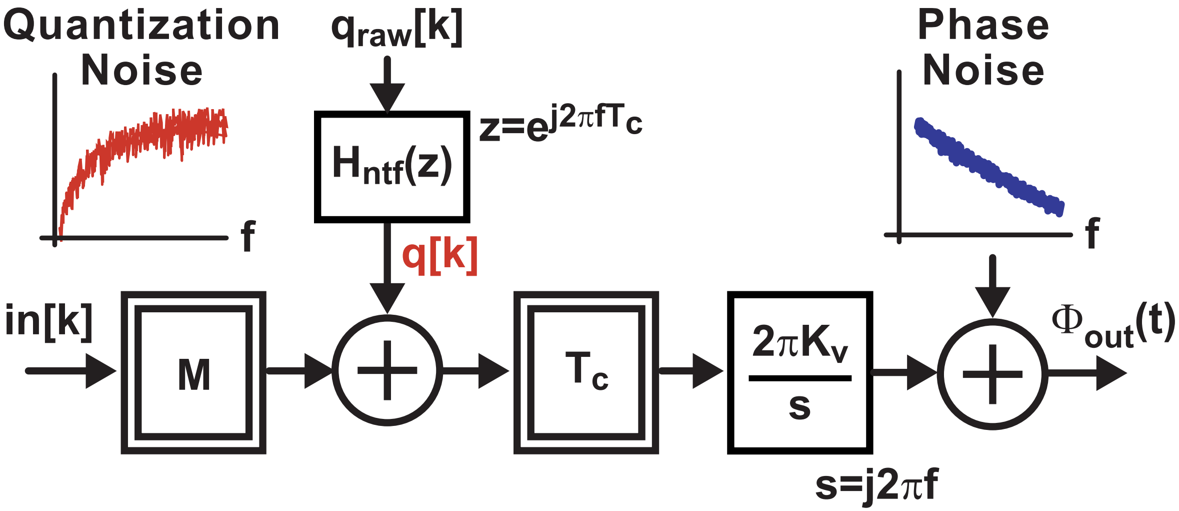


- Proper design of DCO will yield quantization noise that is below that of the intrinsic phase noise (set by tank *Q*, etc.)
  - Assume *q[k]* = 0 for simplified model
- Note that $T = MT_c$

Supplemental Slides

Section 3: Derivation of VCO Quantization Noise Due to Capacitor Dithering

Calculation of Quantization Noise from Cap Dithering



- **DT to CT spectral calculation:**

$$S_{\Phi_{out}}(f)\Big|_{\text{dco,quant}} = \frac{1}{T_c}\left|T_c\frac{2\pi K_v}{j2\pi f}\right|^2 \left|H_{ntf}(e^{j2\pi fT_c})\right|^2 S_{q_{raw}}(f)$$

$$= T_c\left|\frac{K_v}{f}\right|^2 \left|H_{ntf}(e^{j2\pi fT_c})\right|^2 \frac{1}{12}$$

  - ***$S_{q_{raw}}(f)$* = 1/12 since *$q_{raw}[k]$* uniformly distributed from 0 to 1**
  - ***$H_{ntf}(z)$* is often 1-*z^{-1}* (first order) or (1-*z^{-1}*)^2 (second order)**

Example Calculation for DCO Quantization Noise

- **Assumptions (Out freq = 3.6 GHz)**
  - **Dithering frequency is 200 MHz (i.e., $1/T_c$ = 200e6)**
  - **Σ–Δ has first order shaping (i.e., $H_{ntf}(z) = 1 - z^{-1}$)**
  - **Fine cap array yields 12 kHz/unit cap (i.e., K_v = 12e3)**

$$S_{\Phi_{out}}(f)\Big|_{\text{dco,quant}} = T_c \left|\frac{K_v}{f}\right|^2 \left|H_{ntf}(e^{j2\pi f T_c})\right|^2 \frac{1}{12}$$

$$= \frac{1}{200e6}\left|\frac{12e3}{f}\right|^2 \left|1 - e^{j2\pi f/200e6}\right|^2 \frac{1}{12}$$

- **At a frequency offset of *f* = 20 MHz:**

$$= \frac{1}{200e6}\left|\frac{12e3}{20e6}\right|^2 \left|1 - e^{j2\pi 1/10}\right|^2 \frac{1}{12} = 5.73 \cdot 10^{-17}$$

$$10\log(5.73{\cdot}10^{-17}) = -162.4\ dBc/Hz\ \ \text{(at 20 MHz offset)}$$

Below the phase noise (-153 dBc/Hz at 20 MHz) in the example

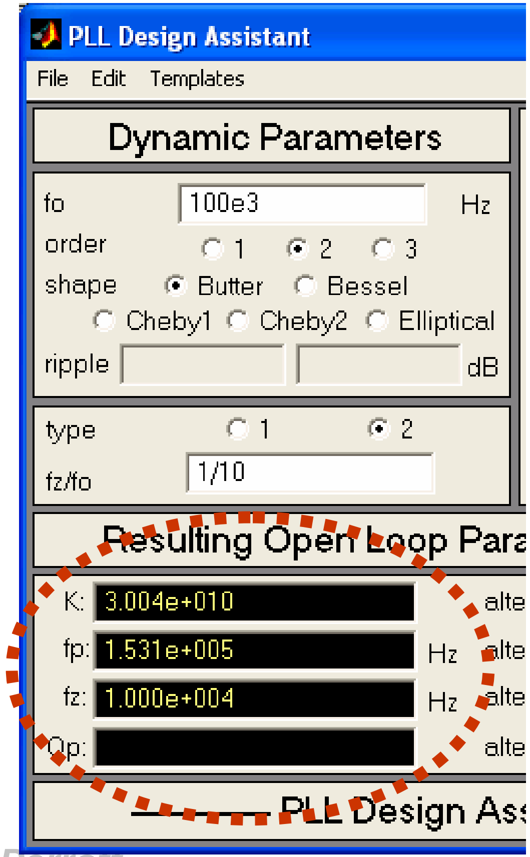
Supplemental Slides

Section 4: Derivation of Discrete-Time Loop Filter Parameterization based on Continuous-Time Specifications

Transfer Function Design using PLL Design Assistant

- PLL Design Assistant assumes continuous-time open loop transfer function $A_{calc}(s)$:

$$A_{calc}(s) = \frac{K}{s^{type}} \frac{1 + s/w_z}{1 + s/w_p}$$



Dynamic Parameters

fo 100e3 Hz

order ○ 1 ● 2 ○ 3

shape ● Butter ○ Bessel ○ Cheby1 ○ Cheby2 ○ Elliptical

ripple dB

type ○ 1 ● 2

fz/fo 1/10

Resulting Open Loop Para

K: 3.004e+010 alte

fp: 1.531e+005 Hz alte

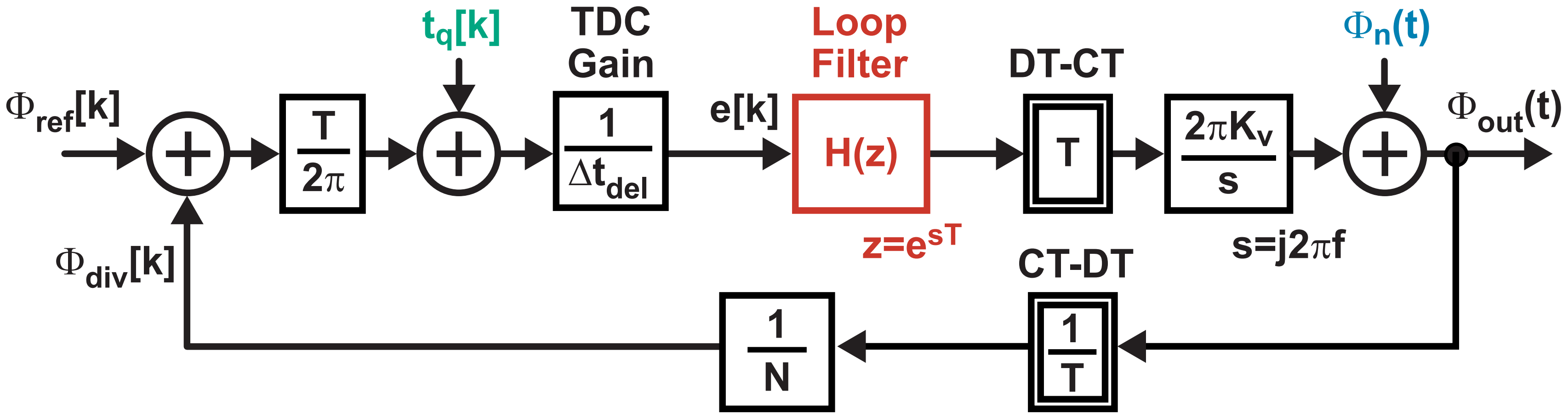
fz: 1.000e+004 Hz alte

Qp: alte

PLL Design Ass

- Above parameters are calculated based on the desired closed loop PLL *bandwidth*, *type*, and *order* of rolloff (which specify *G(s)*)
- For 100 kHz bandwidth, *type* = 2, 2nd order rolloff, we have:
  - $K = 3.0 \times 10^{10}$
  - $w_p = 2\pi(153 \text{ kHz})$
  - $w_z = 2\pi(10 \text{ kHz})$

Continuous-Time Approximation of Digital PLL



- At low frequencies (i.e., |*sT*| << 1), we can use the first order term of a Taylor series expansion to approximate

$$z^{-1} = e^{-sT} \approx 1 - sT$$

- Resulting continuous-time approximation of open loop transfer function of digital PLL:

$$\boxed{A(s) \approx \frac{T}{\Delta t_{del}} \frac{K_v}{N} \frac{1}{s} H(z) \Big|_{z^{-1} \approx 1 - sT}}$$

Applying PLL Design Assistant to Digital PLL Design

- **Given the continuous-time approximation of *A(s)*, we then leverage the PLL Design Assistant calculation:**

$$A(s) = A_{calc}(s)$$

  - **Also note that:**

$$z^{-1} = 1 - sT \;\Rightarrow\; \boxed{s = \frac{1 - z^{-1}}{T}}$$

- **Given the above, we obtain:**

$$\left.\frac{T}{\Delta t_{del}}\frac{K_v}{N}\frac{1}{s}H(z)\right|_{s=\frac{1-z^{-1}}{T}} = \left.\frac{K}{s^{type}}\frac{1+s/w_z}{1+s/w_p}\right|_{s=\frac{1-z^{-1}}{T}}$$

$$\boxed{\Rightarrow H(z) = \left.\frac{\Delta t_{del}}{T}\frac{N}{K_v}\left(\frac{K}{s^{type-1}}\right)\frac{1+s/w_z}{1+s/w_p}\right|_{s=\frac{1-z^{-1}}{T}}}$$

Simplified Form for Digital Loop Filter (Type II PLL)

- **From previous slide:**

$$H(z) = \frac{\Delta t_{del}}{T}\frac{N}{K_v}\left(\frac{K}{s^{type-1}}\right)\frac{1+s/w_z}{1+s/w_p}\Bigg|_{s=\frac{1-z^{-1}}{T}}$$

- **Simplified form with *type = 2* (assume *order = 2*)**

$$H(z) = K_{LF}\left(\frac{1}{1-z^{-1}}\right)\frac{1-b_1z^{-1}}{1-a_1z^{-1}}$$

  - **Where:**

$$a_1 = \frac{1}{1+w_pT} \qquad b_1 = \frac{1}{1+w_zT}$$

$$K_{LF} = \underset{*}{\underline{\left(\frac{\Delta t_{del}}{T/N}\right)}}\frac{K}{K_v}\left(\frac{w_p}{w_z}\right)\frac{a_1}{b_1}T$$

Note:
T_{dco}= T/N

*** Typically implemented by gain normalization circuit**