22.3 A 0.5V <4μW CMOS Photoplethysmographic Heart-Rate Sensor IC Based on a Non-Uniform Quantizer

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Photoplethysmographic biosensing has been of recent interest, since it provides electrode-free operation for continuous health-monitoring applications [1]. This paper presents a <4μW heart-rate (HR) monitor IC based on measurement of fluctuations in the light intensity passing through tissue such as a finger [2-4]. As shown in Fig. 22.3.1, key components of the system include a logarithmic, digital-to-resistance converter (DRC) that forms the load of an external photodiode, and a non-uniform quantizer that provides error information to a digital accumulator controlling the DRC input. As the photodiode current fluctuates due to HR-induced pulsing of bloodflow through the tissue, the feedback loop adjusts the DRC load resistance in order to maintain constant voltage across the photodiode. As such, the accumulator output, $OUT_{ADC}[k]$, provides a digital representation of HR-induced fluctuations of the photodiode current, and the logarithmic implementation of the DRC accommodates 3 orders of magnitude in light intensity. In order to obtain instantaneous HR frequency, HR[k], off-chip digital signal processing is performed on $OUT_{ADC}[k]$.

The use of a quantizer to directly sense the error information in the feedback loop introduces the challenge of achieving low quantization noise along with a sufficiently large range to allow fast response to large perturbations. To address this issue, non-uniform steps are utilized, such that a high-resolution region is active during steady-state operation, and coarser regions accommodate large perturbations. As indicated in Fig. 22.3.1, this non-uniform quantization profile is achieved by cascading 3 stages of a Laddered-Inverter Quantizer/Amplifier/Filter (LIQAF) circuit introduced in this paper. The LIQAF circuit provides amplification and lowpass filtering, in addition to quantization, and cascading LIQAF stages leads to the desired non-uniform quantization characteristic. The feedback loop is designed such that the nominal operating point of the non-uniform quantizer is placed within the region of highest resolution, thus allowing low quantization noise to be achieved under steady-state conditions.

Figure 22.3.2 provides details of the DRC, which consists of series-connected polysilicon resistors and PMOS switches that are controlled in thermometer-coded fashion by a digital, 1st-order, 5b output ΔΣ modulator. Note that since the resistance steps are nonlinear due to the desired logarithmic action of the DRC, a higher-order, multi-bit ΔΣ modulator would encounter issues with noise folding. Fortunately, the low bandwidth of <5Hz required for sensing HR-induced fluctuations allows for a large oversampling ratio with the 32kHz clock frequency, so that a 1st-order ΔΣ structure is adequate for the needs of this application.

To explain the key principles of the proposed LIQAF circuit, Fig. 22.3.3 shows a simple, 2-output LIQAF design along with its DC characteristic. As depicted in the figure, we can consider the circuit as a combination of two CMOS inverters that have different ratios of NMOS versus PMOS gate lengths. When V_{in} is low and both outputs are high, transistor M_1 is inactive such that V_{out0} transitions with increasing V_{in} according to a CMOS inverter characteristic with one NMOS device and two series PMOS devices. In contrast, when V_{in} is high and both outputs are low, M_2 is inactive such that V_{out1} transitions with decreasing V_{in} according to a CMOS inverter characteristic with two series NMOS devices and one PMOS device. Note that V_{out0} cannot transition high unless V_{out1} is also high, and V_{out1} cannot transition low unless V_{out0} is also low. As such, the LIQAF circuit provides guaranteed monotonicity in the quantizer characteristic, and low power is achieved since current is shared for all of the devices.

A 15-output LIQAF structure is used in the HR monitor IC as shown in Fig. 22.3.4, which yields a 15-level quantizer that is guaranteed to be monotonic and re-uses the same current for all of the quantizer levels. With the increase in number of quantizer outputs, large output resistance is encountered for most outputs due to the larger effective gate length of their respective inverter structures. Large output resistance leads to low bandwidth and relatively high intrinsic gain, $g_m r_o$,, when a given inverter is in its transition region. Fortunately, the low bandwidth is an asset to the HR application, since it provides rejection of undesired noise. However, the high intrinsic gain poses an issue when cascading LIQAF stages by using the V_{out7} output as the input to the next LIQAF stage. Lower intrinsic gain is desirable to avoid overly reducing the range of the high-resolution quantizer region beyond what is needed to avoid quantization noise becoming dominant in the HR sensor frontend. Fortunately, reduced intrinsic gain for the V_{out7} output is readily achieved by using the transistor-based load shown in Fig. 22.3.4. As seen in the measured DC characteristic shown in the figure, the presence of the load leads to a reduced slope over the key portion of the V_{out7} transition region impacting the LIQAF stage to follow.

Figure 22.3.5 shows the overall 3-stage LIQAF-based quantizer structure and measured quantizer characteristic, along with SPICE-based calculations of gain and bandwidth across process and 0 to 70°C temperature variation. The quantizer characteristic reveals progressively improved resolution as the input voltage is swept from coarse to fine regions. Note that the parasitic poles introduced by the LIQAF quantizer stages are sufficiently high to avoid stability issues for the feedback system shown in Fig. 22.3.1, which is designed to have ~7Hz closed-loop bandwidth.

A die photo of the 180nm CMOS HR monitor IC is shown in Fig. 22.3.7. Measured IC current for all analog and digital blocks except for output data drivers is <7μA with 0.5V supply for an external photodiode current range of 4nA to 3.5μA, thereby leading to <4μW power consumption for the IC. Figure 22.3.6(a) shows the measured digital bandpass output, $OUT_{BPF}[k]$, and Fig. 22.3.6(b) shows the HR frequency, HR[k], while using only ambient light passing through the first author's index finger within an office setting. In this case, the photodiode bias current is measured as 18nA using a 10kΩ resistor in series with the photodiode. In order to more fully characterize the performance of the HR monitor IC, an external LED circuit modulated by a sine wave signal is used as a light source. Given this arrangement, Fig. 22.3.6(c) shows measured error performance of the instantaneous frequency, HR[k], across a 4nA-to-3.5μA range of photodiode bias current under fixed 0.5% peak-to-peak variation and 1.2Hz (i.e., 72bpm) modulation frequency. The results indicate better than 0.25% rms error for instantaneous frequency, HR[k], even at an extremely low photodiode bias current of 4nA, which reveals excellent sensitivity compared to previous work [2]. Figure 22.3.6(d) shows measured error performance of the instantaneous HR frequency across a 0.5-to-5Hz (i.e., 30-300bpm) modulation frequency with 4nA of photodiode bias current and 0.5% peak-to-peak variation, which reveals worse case performance of 1.2% rms error for instantaneous frequency, HR[k], using the fixed digital bandpass filter centered at 1.8Hz (108bpm). Further improvement is possible by using an adaptive digital bandpass filter in which the *a* coefficient is adjusted.

Acknowledgements:
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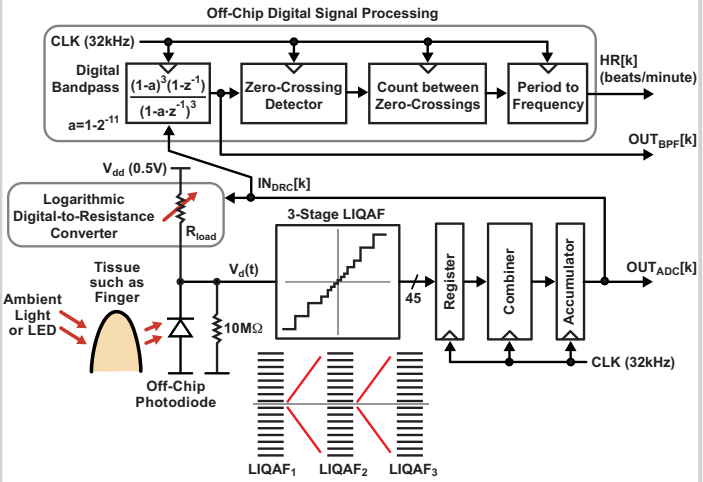

Figure 22.3.1: System-level view of heart-rate sensor.

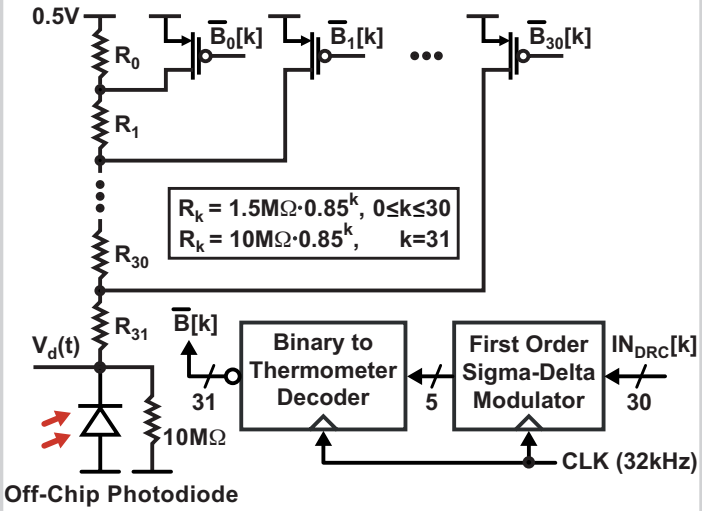

Figure 22.3.2: Logarithmic digital-to-resistance converter (DRC).

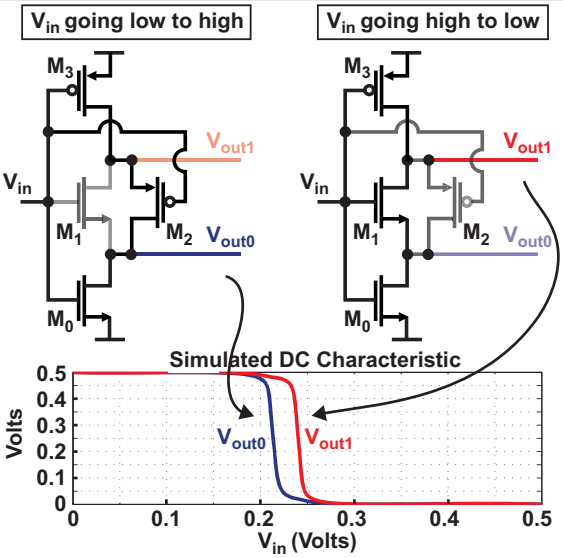

Figure 22.3.3: Basic principles of a 2-output LIQAF circuit.

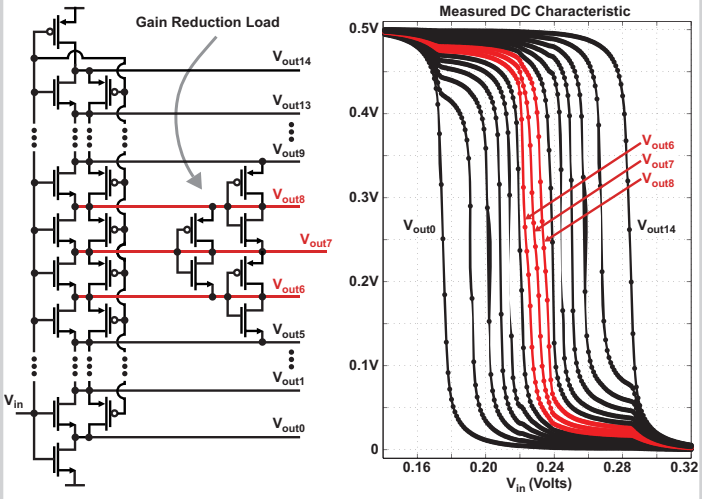

Figure 22.3.4: 15-output LIQAF with gain-reduction load on Vout7.

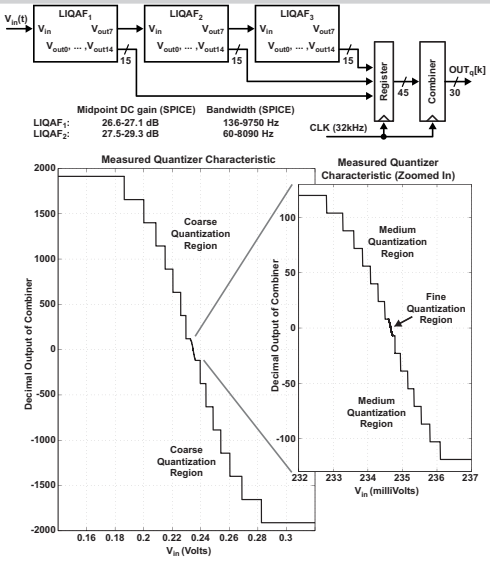

Figure 22.3.5: 3-stage LIQAF quantizer with measured characteristic.

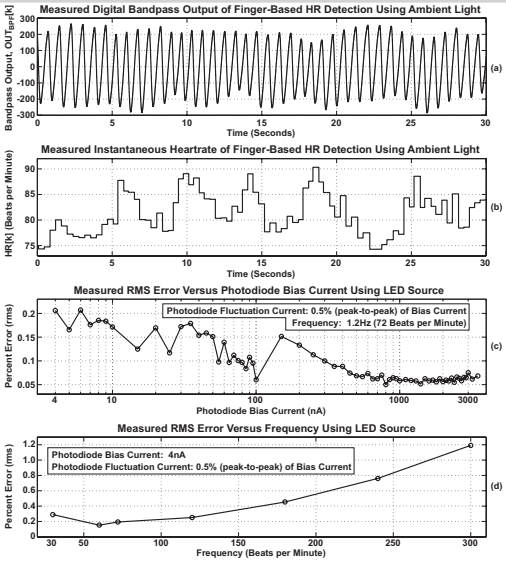

Figure 22.3.6: Measured results.

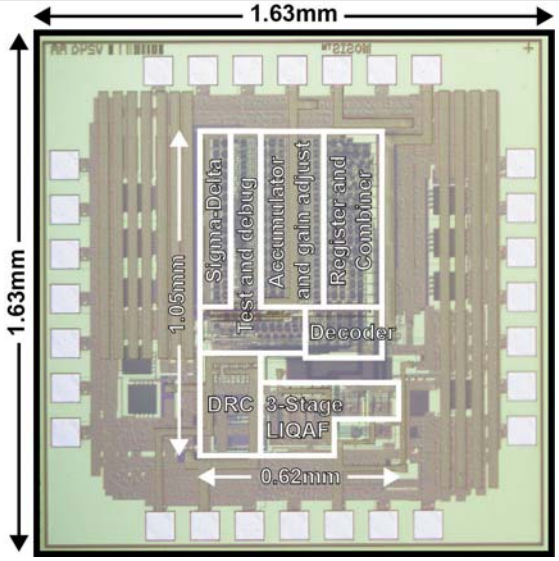

Figure 22.3.7: Micrograph of the 180nm CMOS die.

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