An Optical-Electrical Sub-Sampling Receiver Employing Continuous-Time ΔΣ Modulation

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***Abstract*—An optical-electrical sub-sampling down-conversion receiver architecture leveraging low-jitter optical sampling is described. A simple interface between the optical and electrical domains is accomplished by combining a photodiode with a second-order continuous-time ΔΣ modulator. A prototype system implemented in 0.18 µm CMOS achieving 36.4 dB SNR in a 2 MHz BW with an OSR of 250 is demonstrated.**

I. Introduction

With large-scale monolithic integration of both circuits and optical devices less than a decade away, the field of opto-electrics is poised for a rapid and comprehensive transformation. Indeed, the numerous benefits that accompany full system integration (e.g. lower cost, area, and power consumption, better matching, greater device customization, etc.) will enable designers to create high-performance opto-electrical communication systems that are more affordable and more portable. Furthermore, integrated opto-electronics allows the leveraging of optical devices and their unique properties (e.g. modulators, wave-guides, amplifiers, etc.) in systems that were once exclusively implemented with electronics, resulting in hybrid systems that potentially are superior to purely electronic implementations in terms of speed and precision.

This work explores the use of optics in what has predominantly been an electronic application space: down conversion of RF signals. In the system shown in Fig. 1, low-jitter pulsed lasers are leveraged to perform precise *sub*-sampling of an RF signal. Information travels seamlessly between the optical and electrical domains by connecting the photodiode to an on-chip current source and capacitor. The resulting photodiode-based integrator serves as the input stage to a continuous-time (CT) 2nd order ΔΣ ADC, which digitizes the down-converted signal. Section II describes the optical portion of the system, and explains how precise sub-sampling is achieved in the optical domain; Section III highlights the proposed optical-to-electrical interface, and reviews the merits of a CT ΔΣ architecture; Section IV discusses the measured results; Section V concludes the paper with a brief discussion of future work.

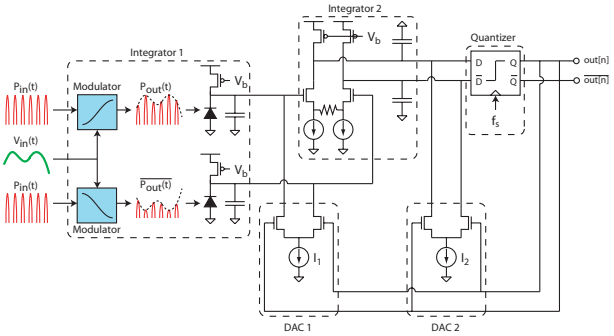

Figure 1. System-level diagram of the sub-sampling down-converison receiver with second-order ΔΣ ADC

II. The Optical Advantage in Low-Jitter Sampling

A. Limitations in Electronic Sub-Sampling

Sub-sampling is commonly used as an alternative to conventional down-conversion architectures, but is usually limited to applications that do not require large bandwidths and high precision. Indeed, prior work employing narrowband electronic sub-sampling architectures suffered lower SNR than other conversion techniques due to noise-folding from aliasing, and noise skirts arising from local oscillator aperture jitter [2-5]. Noise folding can be minimized through band-pass filtering of the RF prior to mixing, as was done in previous work. However, due to the fundamental limit of aperture jitter in electronics (0.5-2 ps RMS [6]) and its impact on SNR, sub-sampling architectures have seldom operated above a few GHz.

The SNR for a given aperture jitter and carrier frequency is described by [1]:

$$SNR = 20\log\left(\frac{1}{2\pi f \Delta t}\right) \quad (1)$$

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where f is the carrier frequency and Δt is the RMS jitter of the local oscillator. Aperture jitter of mode-locked lasers have been shown to be extremely low (10-15 fs [7]), which facilitates the sub-sampling of RF signals in the 10's of GHz range with close to 8 bit precision. Furthermore, the high-Q (approximately 300) of resonant optical phase modulators enables high image rejection. Table 1 lists the SNR values for various RF carrier frequencies assuming 10 fs RMS aperture jitter and a 2 MHz BW. Indeed, 8 bit resolution is possible at 40 GHz.

To validate these claims, a prototype system using a 969.7 MHz repetition-rate mode-locked laser with 75 fs of RMS jitter in a 1 MHz BW was created. Given an IF of 1.35 MHz, an RF carrier at 1.938 GHz was chosen.

B. An Optical-Electrical Sub-Sampling Receiver

The optical-electrical sub-sampling receiver architecture is shown in Fig. 2, and comprises the mode-locked laser, modulator, and electrically-biased photodiodes. Mode-locked lasers generate nearly ideal impulse trains with pulses that can be less than 100 fs wide and with excellent jitter characteristics ([7] reported less than 15 fs in a 10 Hz to 375 MHz BW). Optical modulators use an applied voltage to control the power level of the optical signal leaving the device. The relationship between optical power and applied voltage is described by [8]:

$$P_{out}(t) = P_{in}(t)\sin^2\left(\frac{\pi}{2}\cdot\frac{v_{in}(t)}{v_\pi}\right) \qquad (2)$$

where v_π is the modulator voltage-to-phase gain [V·rad].

Note that the modulation of the optical power as described in equation (2) is single ended. Differential optical power modulation was achieved in this system by placing the modulator in a *Sagnac-Loop Interferometer* orientation, which allows differential power modulation proportional to $sin^2(\phi)$ and $cos^2(\phi)$ (see Fig. 2).

When biased in its linear range ($V_{IN,DC} = v_\pi/2$), the modulator behaves like an optical-electrical mixer, modulating the optical power according to the applied voltage. By approximating the mode-locked laser pulses as an ideal impulse train, it becomes clear that the laser is effectively sampling the electronic signal:

TABLE I. SNR AND ENOB AT ASSUMING 10FS (RMS) JITTER

Harmonic (GHz)	*SNR (dB)*	*ENOB*
1	84	14.0
5	70	11.7
10	64	10.7
20	58	9.7
40	52	8.7

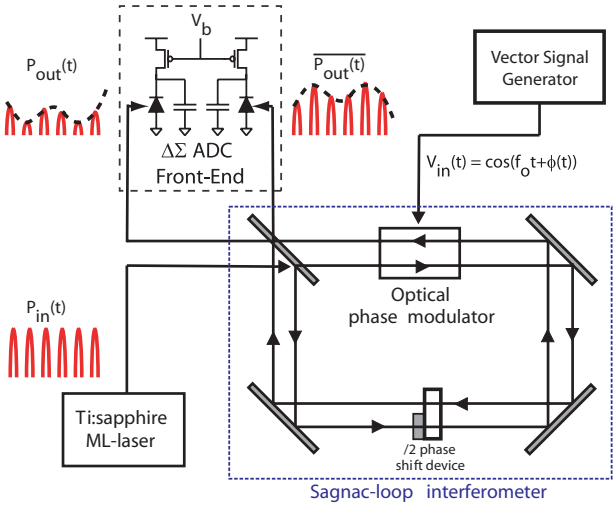

Figure 2. Optical sampling of an electronic RF signal by differential optical power modulation via the Sagnac-loop interferometer.

$$P_{out}(t) \approx \left(\frac{\pi}{2}\cdot\frac{1}{v_\pi}\right)\cdot\sum_{k=-\infty}^{+\infty} v_{in}(t)\cdot P_{avg}\,\delta(t-kT_s) \qquad (3)$$

In a sub-sampling architecture, aliasing is purposely induced so that a replica of the high-frequency signal of interest appears at baseband. Fig. 3 depicts the sub-sampling concept by illustrating the frequency-domain interpretation of Fig. 2. Multiplication in time is equivalent to convolution in frequency, and the applied electrical signal to the modulator, $v_{in}(t)$, is some narrowband signal centered at a high frequency RF carrier. Since the Fourier Transform of an impulse train is also an impulse train, replicas of the RF signal appear at every harmonic of the impulse train. A low-pass-filter eliminates all but the baseband replica prior to digitization. The filtering is performed by the continuous-time (CT) ΔΣ ADC, and is described in the next section.

III. OPTICAL-ELECTRICAL CONTINUOUS-TIME ΔΣ ARCHITECTURE

A photodiode converts the optical information (photons) into electrical information (charge), and the question now becomes how to efficiently digitize this information.

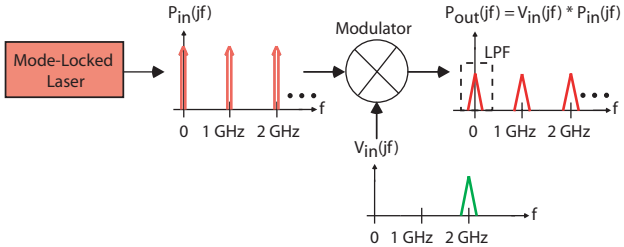

Figure 3. Frequency-domain illustration of the sub-sampling receiver.

Previous implementations of optical-electrical ADC's [6,9,10] adopted what can best be described as a charge compartmentalization approach (see Fig. 4a). Here, a sample-and-hold (S/H) circuit is used to store information onto a capacitor, and digitization accomplished via a flash or pipeline ADC. Due to the generation of pulsed photocurrents in the milli-ampere range, large devices are needed to reduce the switch resistance. Unfortunately, the dynamic range (DR) in these implementations usually suffers due to MOS-switch non-idealities such as charge injection, clock feed-through and non-linear MOS resistance. Furthermore, pulse transients arising from slow carrier recombination in the diode further complicate the charge compartmentalization within the sample period, typically requiring fast photodiode structures made of exotic materials not available in standard CMOS processes.

The simplest method for capturing the optical information is to use a constant integration approach (see Fig. 4b). This approach is particularly attractive because it precludes the implementation of a S/H network, thus bypassing many of the non-idealities associated with MOS switches. Furthermore, since charge is no longer compartmentalized, the system is not as sensitive to current pulse transients arising from the recombination time constants of the photodiode.

However, some mechanism to sense the continuous discharge and recharge the capacitor is necessary. This can be accomplished with a quantizer (comparator) and a digital-to-analog converter (DAC). The quantizer senses when the capacitor voltage falls beyond a certain threshold, and then drives a current DAC to replenish the capacitor. As long as the *total* charge supplied by the DAC is greater than or equal to that discharged by the photodiode, the capacitor voltage will not integrate without bounds.

Structurally, the feedback loop in Fig. 4b is identical to that of a conventional 2nd order continuous-time (CT) ΔΣ ADC, except that the voltage-to-current conversion is accomplished by the optical modulator and photodiode pair, as opposed to a transconductance-C amplifier or an op-amp RC integrator. When the quantizer oversamples the input signal, the loop operates identically to a CT ΔΣ ADC, and achieves the benefits associated with the topology: noise shaping, high SNR and DR, and potentially lower power for a given precision.

In addition to eliminating the S/H network, CT ΔΣ ADC's have the added advantage of inherent anti-aliasing filtering [11]. Indeed, as long as the laser pulse repetition rate is some integer multiple of the ADC sampling rate, replicas occurring at harmonics of the impulse train will be eliminated, save the baseband copy. Both of these architectural benefits in the CT ΔΣ ADC structure allow for a seamless and elegant interface between the optical and electrical halves of the system.

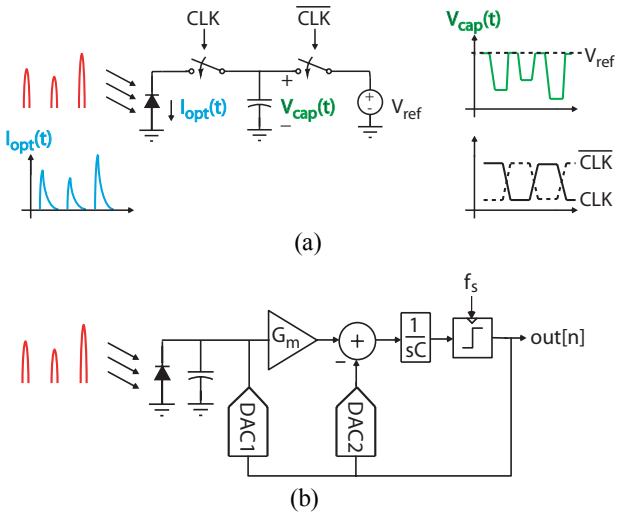

Figure 4. Architectures for digitizing optical information: (a) charge compartmentalization, (b) charge integration with DAC feedback, i.e. a CT ΔΣ modulator

SNR and DR degradation arising from finite loop delay in 2nd order CT ΔΣ ADC have been well documented and various methods for compensating for it have been proposed [12,13]. The method of using RZ DAC pulses proposed in [12] was chosen since it also offered a simple solution to the problem of unequal rise and fall times of NRZ DAC pulse transients. While RZ DAC implementations are more sensitive to DAC jitter [13], simulations showed that inband noise arising from DAC jitter was buried beneath the photodide shot noise floor.

IV. Measured Results

An FFT and corresponding eye-diagram of the digitized receiver output are shown in Fig. 5 and 6 for a 100 kbps GMSK pattern at a carrier of 1.938 GHz, a laser repetition rate of 969.7 MHz, and ADC sample rate of 1 GHz. The SNR of the sub-sampled unmodulated carrier was calculated over an effective BW of 2 MHz (ΔΣ OSR ~ 250), and SFDR specified at the second harmonic (see Table 2).

TABLE II. Summary of CT ΔΣ ADC Performance

Measured Results	
SNR / SFDR	36.4 dB / 22.5 dB
OSR	250
Power	47 mW (1.8 V Supply)
Area	0.64 mm^2
Technology	0.18 μm CMOS

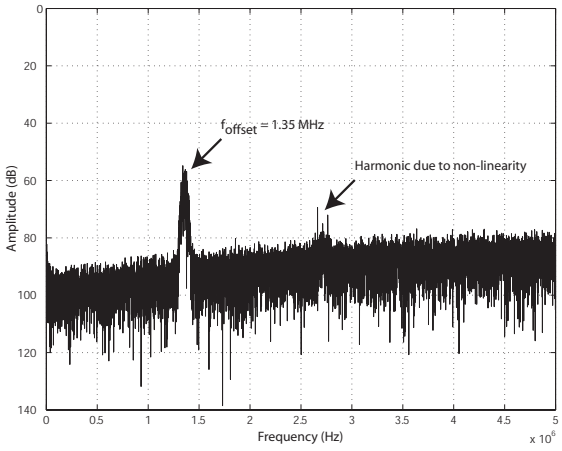

Figure 5. Measured FFT of ADC digital output.

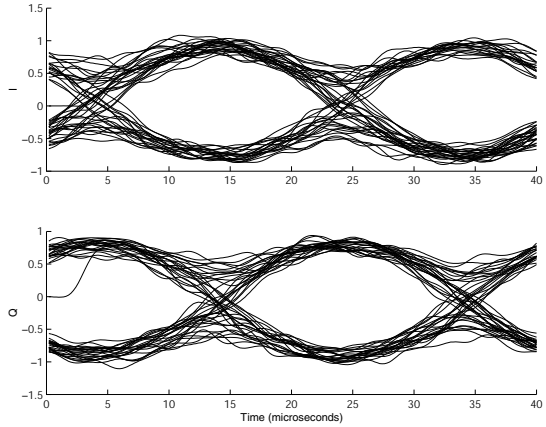

Figure 6. Measured eye-diagram of the received I and Q data at 100 kbps. Data pattern is 180 symbols long and diagram is 4 symbols wide.

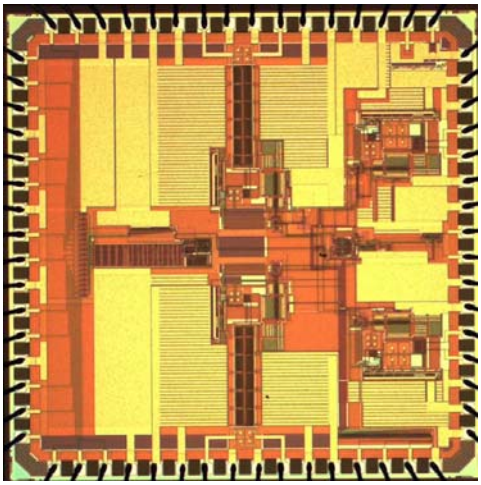

Figure 7. Die photograph. Entire chip area is approximately 3mm by 3mm, but actual ADC active area is approximately 0.64 mm^2.

Note that the SNR and SFDR are limited by the modulator non-linearity and photodiode shot noise. The non-linearity is caused by a differential power offset (~ 1.3 mW) in the outputs of the Sagnac-loop interferometer. The shot-noise floor is limited by the finite optical power that can be focused on the photodiodes (< 4 mW). Both of these issues are due to the limitations in the free-space optical setup, and prevented the ADC from achieving its true dynamic range ability. Subsequent work will strive to build a more stable optical setup for this system.

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