A 0.5 V $<$ 4 μW CMOS Light-to-Digital Converter Based on a Nonuniform Quantizer for a Photoplethysmographic Heart-Rate Sensor

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***Abstract*—A 0.5 V CMOS light-to-digital converter (LDC) based on a nonuniform quantizer and off-chip photodiode enables a photodiode bias current ($I_{\rm bias}$) range spanning 4 nA to 3.5 μA while consuming less than 4 μW of power. Using an off-chip LED as a modulated light source, measurements with a photodiode current signal having modulation frequency of 1.2 Hz (72 beats per minute) and 0.5% peak-to-peak amplitude relative to $I_{\rm bias}$ performed at the low and high end of the $I_{\rm bias}$ range confirm over 30 dB of SNR for an integration bandwidth spanning 0.5 to 5 Hz. Using off-chip digital signal processing of the LDC output, instantaneous period jitter (a proxy for instantaneous heart rate) is measured to be less than 0.45% (rms) of the period, and the high sensitivity of the LDC allows detection of the heart-rate signal from a finger pressed against the off-chip photodiode using only ambient light. Key circuit components of the LDC include a wide range logarithmic digital-to-resistance converter (DRC) utilizing digital multibit $\Delta\Sigma$ modulation to achieve fine resolution and a nonuniform quantizer based on a laddered inverter quantizer (LIQAF) which also acts as a low-noise front-end amplifier and filter.**

***Index Terms*—Analog-to-digital converter (ADC), Delta-Sigma, digital-to-resistance converter (DRC), heart-rate sensor, laddered inverter, light sensor, laddered inverter quantizer/amplifier/filter (LIQAF), low-noise amplifier, nonuniform quantizer, photodetector, photoplethysmographic, resistor DAC, oximetry.**

I. Introduction

HEART rate is a key vital sign to assess the health of an individual and is routinely monitored within clinical settings using pulse oximetry or EKG instruments. Unfortunately, for most individuals, the clinical setting is the only place where their heart rate is observed, which leads to long time durations in which this important vital sign is largely ignored. This issue has been addressed within the context of athletic activities with the advent of sport watches which measure heart rate using chest straps, contact electrodes, and photoplethysmographic methods as used in pulse oximetry devices. However, thus far there has been very limited impact of such heart-rate monitor devices on the general public due to issues such as their relatively high cost and inconvenient form factor.

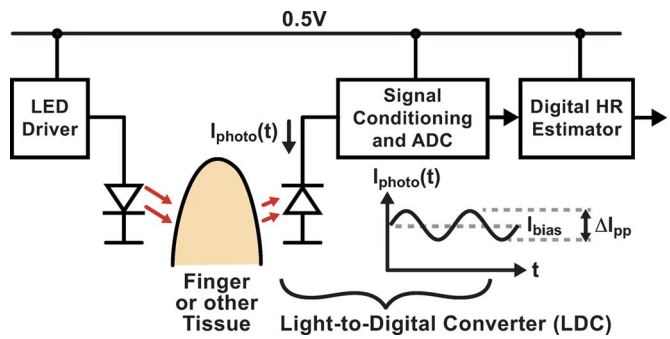

Fig. 1. Overview of heart-rate sensor based on measurement of light fluctuations due to pulsed blood flow through tissue such as a finger.

In this paper, we present a light-to-digital converter (LDC) for photoplethysmographic-based heart-rate monitoring which achieves high sensitivity and wide dynamic range while consuming very low power and operating with a low supply voltage. As illustrated in Fig. 1, the LDC circuit, which utilizes an off-chip photodiode, acts as the front-end of an overall system which includes an off-chip LED, an LED driver operating from a 0.5-V supply voltage [1], and digital signal processing to estimate heart rate. The heart-rate signal is sensed as fluctuations in light intensity as the light passes through tissue such as a finger, with the photodiode generating a current $I_{\rm photo}(t)$ proportional to the light intensity. The peak-to-peak amplitude in photodiode current ΔI_{pp} is typically in the range of 0.5% to 2% of its bias current $I_{\rm bias}$ [2]. In general, it is highly desirable to achieve high sensitivity by being able to sense the signal at low values of $I_{\rm bias}$, and to support a wide dynamic range (i.e., a large ratio of maximum to minimum $I_{\rm bias}$).

Within the overall system in Fig. 1, the LDC is the key circuit for achieving high sensitivity and wide dynamic range. Low-power operation is critical in order to achieve a small form factor by minimizing the size of the energy storage device. A low supply voltage of 0.5 V potentially enables a simple energy-harvesting approach consisting of a direct connection to a solar cell that operates at such voltage levels. Using an LED as the light source leads to the LED driver becoming the dominant power consumer in the system, but improved sensitivity in the LDC reduces the light intensity required from the LED (since lower photodetector current becomes acceptable) and, therefore, lowers the power of the LED driver. The preferred

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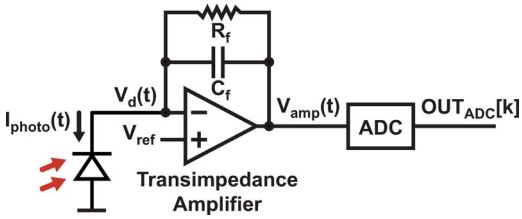

Fig. 2. Classical LDC consisting of a transimpedance amplifier and ADC.

operating mode is to avoid powering the LED light source and instead use ambient light, which, as shown in Section V, may be possible for some applications due to the high sensitivity of the proposed LDC.

To highlight the key challenges in achieving the desired performance characteristics of the LDC, consider the classical implementation shown in Fig. 2. Here, a transimpedance amplifier is utilized to convert the photodiode current, $I_{\rm photo}(t)$, to a voltage, $V_{\rm amp}(t)$, which is then converted to a digital representation by an analog-to-digital converter (ADC). In this structure, the feedback action of the transimpedance amplifier maintains a constant photodiode voltage $V_d(t)$ and provides a low impedance to the photodiode such that $I_{\rm photo}(t)$ is shunted through an *RC* feedback network consisting of R_f and C_f. The conversion gain from current $I_{\rm photo}(t)$ to voltage $V_{\rm amp}(t)$ is set by the value of R_f, and low-pass filtering is provided by including C_f in order to reduce the impact of noise and 50/60 Hz power line corruption. Note that, for heart-rate monitoring, the signal bandwidth typically spans from 0.5 to 5 Hz, which corresponds to 30–300 beats per minute (bpm), respectively.

To achieve high sensitivity, the opamp shown in Fig. 2 must be designed to have adequately low $1/f$ and thermal noise, the ADC must have adequate resolution, and the *RC* filtering must attenuate noise above 5 Hz, with reduction of 50/60 Hz power line corruption being of particular concern. The large dc operating range required of the ADC complicates its design, and achievement of $<$5 Hz bandwidth with on-chip *RC* elements is quite challenging when seeking a low area solution.

To achieve wide dynamic range, the feedback resistor R_f can be made adjustable as is commonly done in variable gain amplifiers (VGA) [3]. However, if one uses a typical VGA approach of utilizing a switched resistor network for variable R_f, it leads to discrete operating regions. Unfortunately, operation across such regions leads to large perturbations of $I_{\rm photo}(t)$ and loss of information due to the discrete nature of the gain switching and its associated transient effects.

In contrast to the classical approach discussed above, we propose the LDC structure shown in Fig. 3. Rather than cascading the transimpedance amplifier with the ADC, the proposed structure combines these functions within a single closed-loop feedback structure. In this design, the traditional transimpedance amplifier is replaced by a digital-to-resistance converter (DRC) consisting of a logarithmic resistor network and digital multibit $\Delta\Sigma$ modulator. A parallel resistor, $R_{\rm par}$, improves sensitivity and dynamic range by extending the minimum value of $I_{\rm bias}$ that is supported. The combination of the DRC and $R_{\rm par}$ enable continuous operation of the LDC over approximately three orders of magnitude range of $I_{\rm bias}$. The DRC is controlled through feedback which consists of a digital accumulator and nonuniform quantizer based on a laddered inverter quantizer/amplifier/filter (LIQAF) [4], which eliminates the need for external passive components such as filter capacitors. The DRC value is set such that the photodiode voltage, $V_d(t)$, matches the desired operating point of an inverter-based low-noise amplifier (LNA) that is realized by the LIQAF-based quantizer. The inverter-based LNA structure provides an efficient means of achieving good noise performance since it minimizes the number of devices that contribute noise and uses the same current for both NMOS and PMOS transconductor devices [5].

Closer inspection of Fig. 3 reveals that the proposed LDC structure is similar to a Delta modulator [6]–[9], but utilizes a multibit, nonuniform quantizer and digital accumulator. In contrast to $\Delta\Sigma$ modulators, the noise of the quantizer is not shaped for Delta modulators. However, $\Delta\Sigma$ modulators require analog integration before the quantizer, which leads to challenges in achieving high dc gain, low area, and low power consumption. The advantage of the proposed structure is that the fine resolution region of the LIQAF-based quantizer offers low quantization noise (under the assumptions discussed below) and the digital accumulator provides the desired characteristics of low area and low power consumption compared with using an analog integrator. The digital accumulator also provides infinite dc gain, which is seen by examining its Z-transform as frequency f goes to 0:

$$\lim_{f\to 0} \left. \frac{K_{\rm accum}}{1-z^{-1}} \right|_{z=e^{j2\pi f T_{clk}}} = \infty \tag{1}$$

where $T_{\rm clk} = 1/32$ kHz represents the time step of the accumulator and $K_{\rm accum}$ is a scale factor which is set to achieve the desired closed loop bandwidth of the LDC. The infinite dc gain of the accumulator allows perfect centering of the nonuniform quantizer during steady-state operation such that, assuming small perturbations to the system, the fine quantization region is utilized to achieve low quantization noise. In the case of large perturbations, the wide range of the nonuniform quantizer characteristic offers a high slew rate which benefits the tracking performance of the LDC.

In practice, the steady-state behavior of the LDC dynamics will vary according to the influence of input stimulus and noise on the nonuniform quantizer. Assuming small input stimulus and noise such that saturation effects are avoided in the quantizer, but sufficiently large stimulus and/or noise to cause sufficient scrambling activity in the quantizer, the LDC feedback dynamics can be approximated as having linear behavior. In such a case, moderate levels of quantizer mismatch will have only a minor impact on LDC distortion performance since the quantizer sees only the *residual error* of the feedback loop which, in turn, is suppressed by the open-loop gain of the accumulator. However, for cases where the input stimulus is sufficiently large to cause saturation effects in the quantizer, slew-rate-limited behavior occurs in the LDC that can cause significant distortion. For the proposed heart-rate (HR) detection application, such distortion is acceptable assuming that the desired information corresponds to the time between edges of the HR signal and that the HR signal is significantly larger than interfering signals (such as 50/60 Hz power line corruption). Given such assumptions,

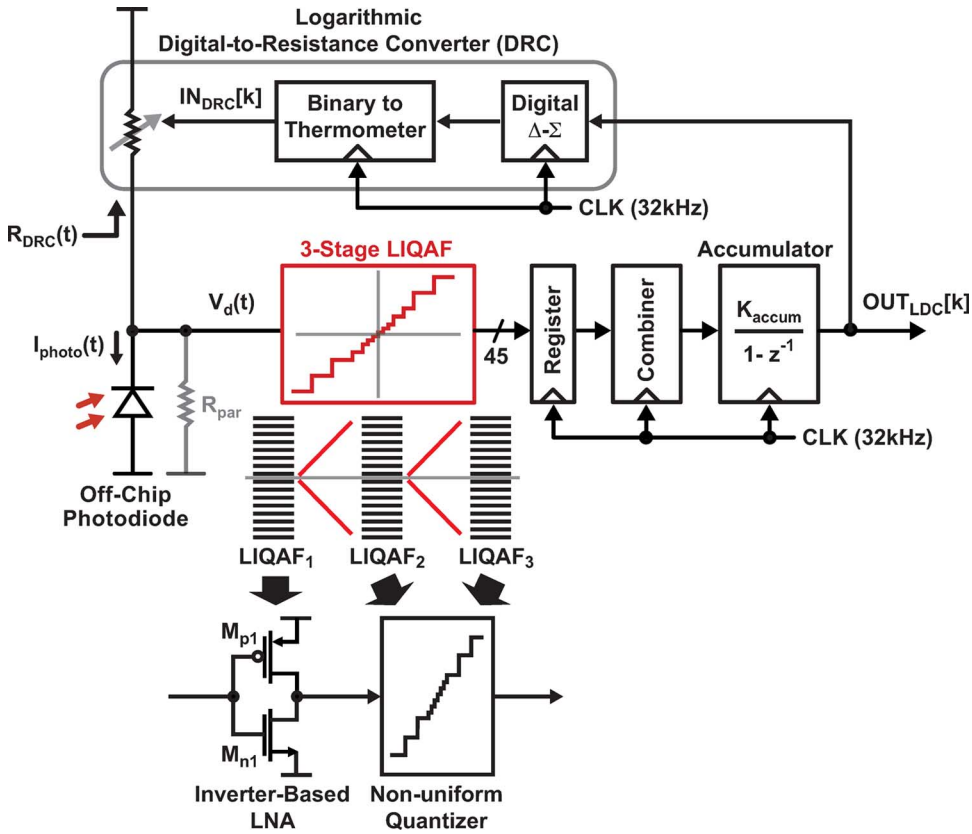

Fig. 3. Proposed LDC architecture.

SNR rather than SNDR is considered to be the key performance metric for this application.

The remainder of this paper is organized as follows. Section II covers additional background information on previous circuit approaches developed for LDC structures. Section III then presents details of the proposed LDC circuits, with primary focus being placed on the DRC and nonuniform LIQAF-based quantizer. Section IV provides high-level system and noise analysis, and Section V presents measured results from a prototype IC. Finally, Section VI concludes.

II. Background

Prior work on improving the performance of LDC circuits is illustrated in Fig. 4. As indicated in Fig. 4(a), improved dynamic range was pursued by rejecting the dc bias of the photodiode current through the use of an auxiliary feedback amplifier and photodiode bias circuit [10]–[12]. However, the additional circuitry in this approach adds noise, thereby reducing sensitivity, and the resulting ac coupling of the photodiode current signal causes a significant increase in settling time when large perturbations are encountered. A dc-coupled solution to improving dynamic range is shown in Fig. 4(b), in which the logarithmic current-to-voltage characteristic of an NMOS device in the subthreshold region is utilized to allow a wide range of photodiode current without saturating the transimpedance amplifier [13]. A key issue of concern in this design is that the reduced transimpedance gain of the logarithmic current-to-voltage characteristic can lead to reduced sensitivity due to the higher impact of opamp noise. Finally, a closed-loop approach combining the transimpedance amplifier and ADC is shown in Fig. 4(c) [14]. Here, a switched capacitor network provides current to the photodiode in order to maintain the photodiode voltage $V_d(t)$ at a constant value. This technique allows a simple quantizer to be used for digitizing the signal, but the issue of achieving wide dynamic range was not addressed in this work.

III. Proposed LDC Architecture

The proposed system shown in Fig. 3 combines the ideas of Fig. 4(b) and (c) by utilizing a logarithmic current-to-voltage characteristic in combination with a closed-loop feedback topology that provides digitization of the signal. However, in contrast to the previous approaches, the proposed system offers a highly digital implementation that minimizes analog complexity. Further, as we will show later in this paper, the design enables wide dynamic range and high sensitivity to be achieved with low-voltage and low-power operation.

Further examination of Fig. 3 reveals two key circuits that enable the highly digital LDC implementation while achieving high performance. The first circuit is the DRC mentioned earlier, in which a digital $\Delta\Sigma$ modulator dithers switches connected to a resistor network in order to achieve high-resolution control of resistance across a wide range. The second circuit is a nonuniform LIQAF-based quantizer that provides an efficient approach to realizing the inverter-based LNA and nonuniform quantizer as depicted in Fig. 3. Each of these circuits will be discussed in further detail in the subsections to follow.

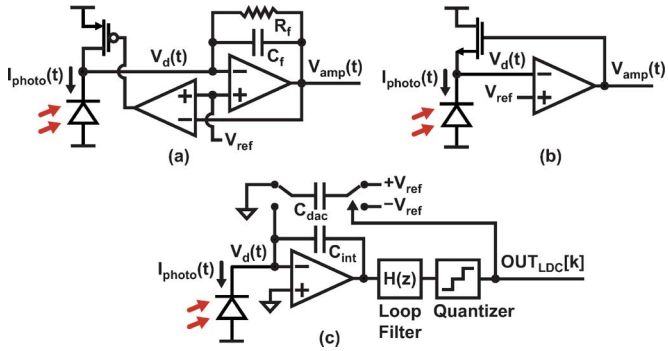

Fig. 4. Prior circuit topologies for improving the performance of LDC circuits. (a) Attenuation of dc offset using feedback [10]–[12]. (b) Improved dynamic range using the logarithmic characteristic of a subthreshold NMOS device [13]. (c) Switched-capacitor-based closed-loop feedback design [14].

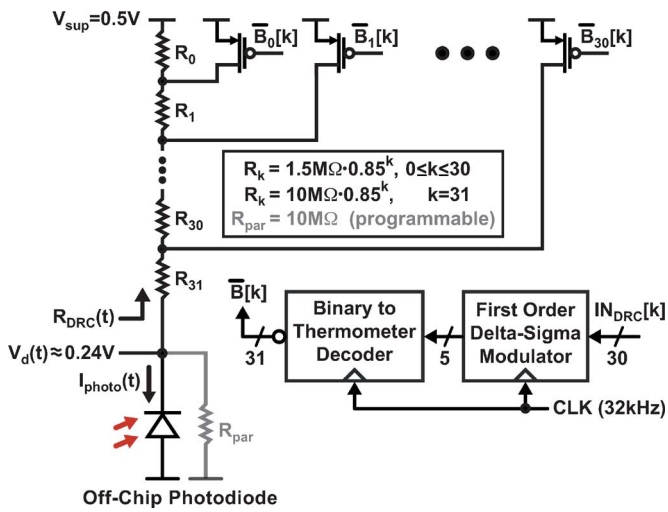

Fig. 5. Logarithmic DRC.

A. Digital-to-Resistance Converter

Fig. 5 provides a more detailed view of the DRC circuit. The variable resistance $R_{\rm DRC}(t)$ is achieved with a set of PMOS switches connected to taps of a polysilicon resistor string ladder, with the PMOS switches being controlled by the output of a digital $\Delta\Sigma$ modulator that provides high-resolution resistance control through dithering.

In order to achieve a wide range of resistance values, the resistor elements within the ladder are progressively scaled according to the equation given in the figure. The maximum resistance, which occurs when all switches are open, corresponds to the sum of all resistor legs which yields $R_{\rm DRC} = 10\ {\rm M}\Omega$. The minimum resistance, which occurs when all switches are closed, corresponds to the resistor leg R_{31} which yields $R_{\rm DRC} = 64.9\ {\rm k}\Omega$. As such, $R_{\rm DRC}$ can be varied by more than two orders of magnitude using only 32 resistor elements.

Due to the nonlinearity of the resistor leg values, the multibit digital $\Delta\Sigma$ modulator is chosen to be first order in order to avoid noise folding. To explain, a first order multibit $\Delta\Sigma$ modulator only dithers one switch setting at a time such that the dithering operation does not see the nonlinearity caused by unequal resistor element values. In contrast, a higher order multibit $\Delta\Sigma$ modulator would dither between several switch settings and thereby expose the $\Delta\Sigma$ to the nonlinearity of the individual resistor element values. Fortunately, the oversampling ratio is quite high given the clock frequency of 32 kHz versus the desired signal bandwidth of $<$5 Hz, so that first-order noise shaping is adequate for this application.

As indicated in Fig. 5, the closed-loop feedback dynamics of the LDC maintain a relatively constant photodiode bias voltage $V_d(t)$ such that the LIQAF-based nonuniform quantizer is centered in its fine quantization region. To simplify the analysis to follow, we will assume $V_d(t) \approx 0.24$ V under nominal conditions for a 0.5-V supply. Given this assumption, the minimum current supported by the $R_{\rm DRC}(t)$ ladder is 26 nA (i.e., (0.5 V–0.24 V)/10 MΩ). In order to improve sensitivity, a parallel resistor $R_{\rm par}$ is connected which reduces the minimum photodiode current that is supported. $R_{\rm par}$ is made programmable using on-chip poly resistors and NMOS switches in order to accommodate variation in $V_d(t)$ away from its assumed 0.24-V bias value. As discussed in Section IV, the presence of $R_{\rm par}$ provides substantial improvement to the dynamic range of the LDC at a slight cost to SNR.

B. Laddered-Inverter Quantizer/Amplifier/Filter

To gain an understanding of the LIQAF circuit, consider the simplified structure shown in Fig. 6(a) in which only two output levels are implemented. As indicated in Fig. 6(b), we can view this circuit as a combination of two CMOS inverters that have different ratios of NMOS versus PMOS gate lengths, which yields the shifted dc characteristics shown in the figure. To explain, note that, when $V_{\rm in}$ is low and both outputs are high, transistor M_1 is inactive such that $V_{\rm out0}$ transitions with increasing $V_{\rm in}$ according to a CMOS inverter characteristic with one NMOS device and two series PMOS devices. In contrast, when $V_{\rm in}$ is high and both outputs are low, M_2 is inactive such that $V_{\rm out1}$ transitions with decreasing $V_{\rm in}$ according to a CMOS inverter characteristic with two series NMOS devices and one PMOS device. Since $V_{\rm out0}$ cannot transition high unless $V_{\rm out1}$ is also high, and $V_{\rm out1}$ cannot transition low unless $V_{\rm out0}$ is also low, the LIQAF circuit provides guaranteed monotonicity in the quantizer characteristic regardless of the presence of mismatch. Note that one should not confuse the curves shown in Fig. 6(a) with the phenomenon of hysteresis—they instead correspond to the dc characteristic of the structure that is independent of the previous state of the input. As will soon be discussed, a very useful aspect of the LIQAF circuit is that it can be utilized as an inverter-based LNA when operating at the mid-rail voltage of a given output (i.e., halfway between supply voltage and ground). Finally, note that the same current is shared by all of the devices, which aids in achieving low power consumption.

In order to increase the number of quantization levels, the prototype LDC presented in this paper makes use of a 15-output LIQAF structure. Fig. 7 depicts the extension of Fig. 6(a) to achieve the increased number of outputs, and also shows simulated dc characteristics for each output as the supply voltage is varied from 0.5 to 1.8 Volts, with the preferred voltage in this application being 0.5 V. The simulated dc characteristics reveal that the quantization behavior is robust across a large supply range. Based on similar arguments as made for the two-output LIQAF example, the quantizer levels are guaranteed to

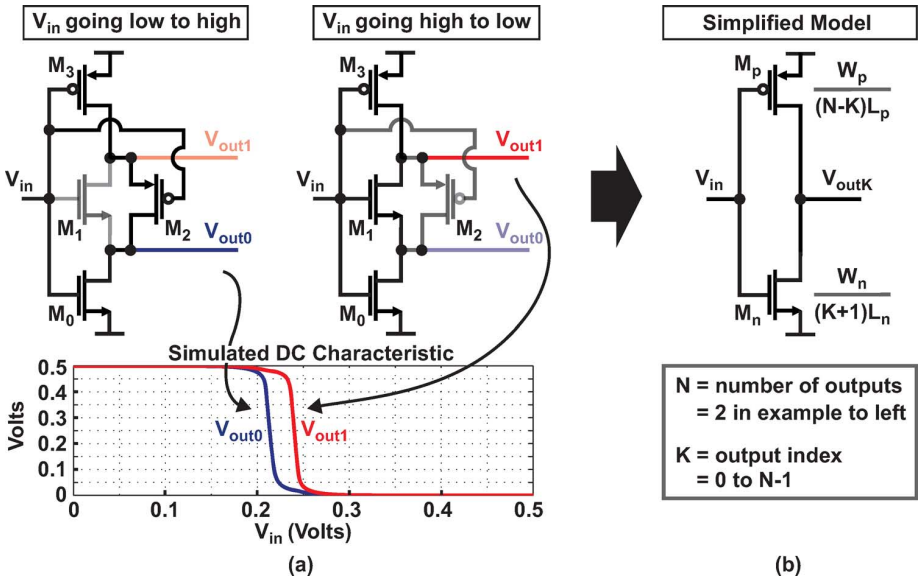

Fig. 6. Basic principles of a two-output LIQAF circuit. (a) Circuit and simulated dc characteristic. (b) Simplified model.

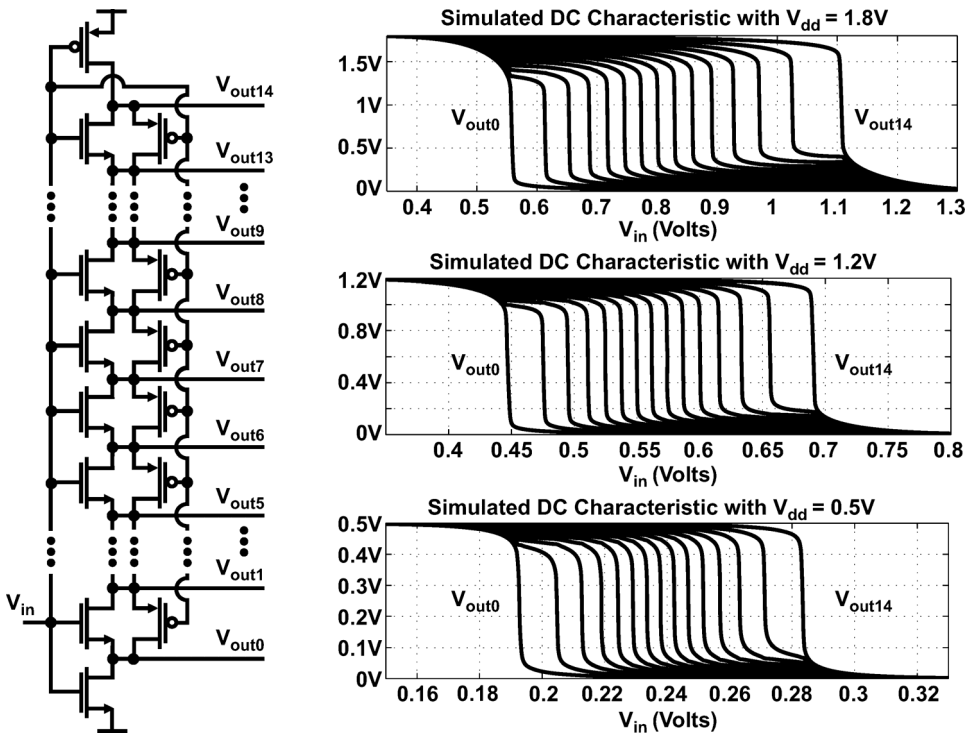

Fig. 7. The 15-output LIQAF circuit along with its simulated dc characteristic under different supply voltages.

be monotonic regardless of the impact of mismatch. To further elaborate, let us define $V_{\text{in}(K)}$ as the input voltage such that output voltage $V_{\text{out}(K)}$ is at its mid-rail value. Since a given output voltage $V_{\text{out}(K)}$ must be strictly larger than $V_{\text{out}(K-1)}$ and strictly lower than $V_{\text{out}(K+1)}$, we see that $V_{\text{in}(K)}$ must have a value strictly *between* $V_{\text{in}(K-1)}$ and $V_{\text{in}(K+1)}$.

With the increase in number of quantizer outputs in Fig. 7, large output resistance is encountered due to the large effective gate length of the respective inverter structures. Large output resistance leads to low bandwidth and relatively high intrinsic gain (i.e., $g_m r_o$) when a given inverter is in its transition region. Fortunately, the low bandwidth is an asset to the given LDC application since it provides rejection of undesired noise. However, when using the $V_{\text{out}7}$ output as the input to the next LIQAF stage, lower gain is desirable to avoid overly reducing the range of the medium and high resolution quantizer regions (as soon discussed). To address this issue, a transistor-based load is added to the LIQAF $V_{\text{out}7}$ output, along with its closest neighbors, as shown in Fig. 8. As seen in the measured dc characteristic depicted in the figure, the presence of the load leads to a reduced slope over the key portion of the $V_{\text{out}7}$ transition region impacting the LIQAF stage to follow.

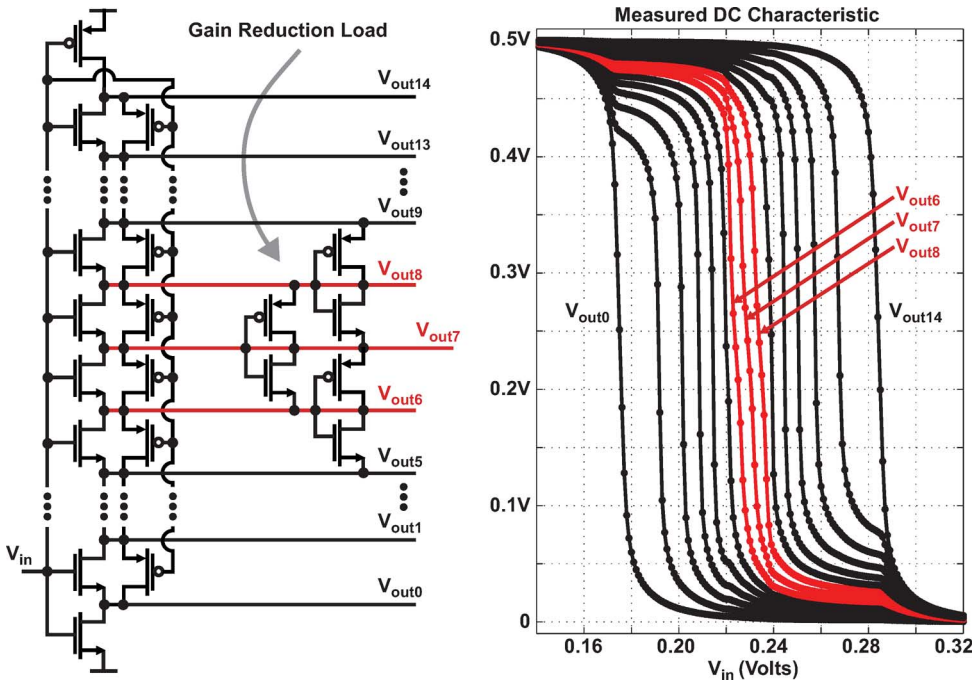

Fig. 8. A 15-output LIQAF circuit with gain reduction load on $V_{\rm out7}$ (which is passed to the following LIQAF stage) along with its measured dc characteristic from the custom IC.

The overall three-stage LIQAF-based quantizer structure, along with its measured dc characteristic, is shown in Fig. 9. The quantizer characteristic reveals progressively improved resolution as the input voltage is swept from coarse to fine regions, with a center voltage at approximately 0.235 V based on a supply voltage of 0.5 V. While more LIQAF stages could be added to achieve even finer resolution, Section IV reveals that this three-stage design achieves an adequately small step size in its fine resolution region such that the fine range quantization noise does not set the bottleneck in the overall LDC noise performance.

To better understand the role of the cascaded stages in forming the nonuniform quantizer characteristic, Fig. 10 provides an intuitive look at how signal amplitude at the input of $\rm LIQAF_1$, operating as an LNA, activates the various quantization levels of $\rm LIQAF_2$, operating as a quantizer. It should be observed that the quantizer range of $\rm LIQAF_2$ is referred to the input of $\rm LIQAF_1$ according to the dc characteristic of output $V_{\rm out7}$ of $\rm LIQAF_1$, with dc gain at the mid level of $V_{\rm out7}$ serving as an approximate metric to evaluate this relationship. One should note that excessively large dc gain leads to an unnecessarily reduced $\rm LIQAF_2$ quantizer range when referred to the $\rm LIQAF_1$ input, which is undesirable since it limits the input range of the cascaded quantizer over which smaller quantization steps are available. This observation helps to clarify the benefit of using the dc gain reduction load on the LIQAF structure shown in Fig. 8.

Fig. 10 also indicates that achievement of monotonicity for the cascaded LIQAF stages requires that the input-referred quantizer range of $\rm LIQAF_2$ be contained within the $\rm LIQAF_1$ quantizer transition boundaries of $V_{\rm out6}$ and $V_{\rm out8}$. Note that in constructing the cascaded quantizer characteristic with the digital combiner circuit shown in Fig. 9, $V_{\rm out7}$ of $\rm LIQAF_1$ and $\rm LIQAF_2$ are ignored such that outputs $V_{\rm out6}$ and $V_{\rm out8}$ provide the nearest $\rm LIQAF_1$ quantization levels when operating $\rm LIQAF_1$ as an LNA. For the given prototype, the measured quantizer characteristic in Fig. 9 indicates that the above monotonicity condition is clearly met.

Process, voltage, and temperature (PVT) variations will alter the LIQAF characteristics as it operates as either an LNA or quantizer. Focusing first on the LNA-related issues of dc gain and bandwidth, Fig. 11 shows the SPICE simulated frequency response at the mid-rail output level for $V_{\rm out7}$ on $\rm LIQAF_1$ and $\rm LIQAF_2$ under PVT variations, which reveal less than 4-dB midpoint dc gain variation but significant bandwidth variation. Fortunately, the bandwidth stays well above the $<$5-Hz closed-loop bandwidth of the LDC, so that its impact on stability of the closed-loop dynamics of the LDC is minimal. As indicated in Fig. 11, $\rm LIQAF_1$ is sized to be much larger than $\rm LIQAF_2$ in order to reduce the impact of $1/f$ noise.

To investigate quantizer-related issues, Fig. 12 shows the worse case SPICE simulated dc characteristics of $\rm LIQAF_1$ and $\rm LIQAF_2$ under PVT variations in terms of minimum and maximum input range. Fortunately, the overall quantizer behavior appears robust. The key characteristics to consider for the LIQAF-based quantizer under PVT variations are its offset, gain, and filtering characteristic. Variations in offset are accommodated by the infinite dc gain of the accumulator within the LDC, which ensures that the steady-state input into the cascaded quantizer centers it within its fine quantization region. The impact of the resulting shift of the bias voltage (i.e., $V_d(t)$) on $I_{\rm bias}$ can be somewhat mitigated by adjusting the value of $R_{\rm par}$ such that the LDC sensitivity is maintained. Variations in gain correspondingly change the open loop gain of the LDC, which results in variation of the closed loop bandwidth of the LDC. To avoid stability issues

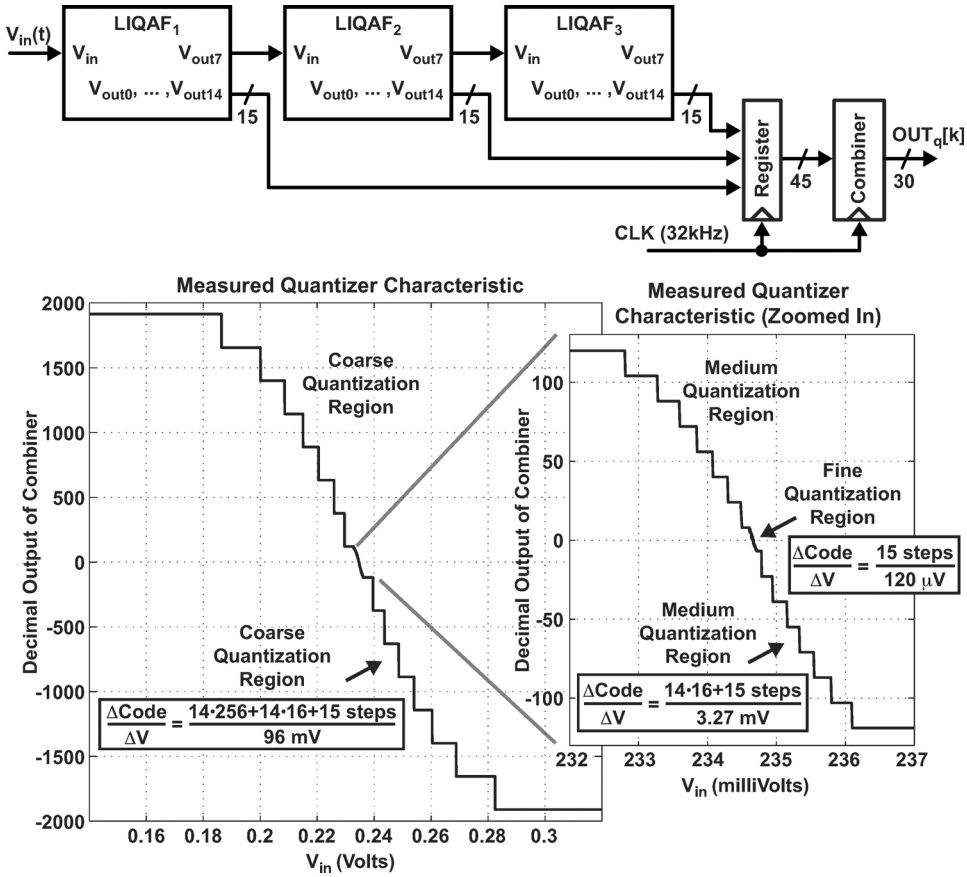

Fig. 9. Three-stage LIQAF quantizer along with its measured quantizer characteristic from the custom IC.

in such case, the poles of the LIQAF LNA/quantizer, which form the filter responses shown in Fig. 11, should be designed to be sufficiently high relative to the closed loop bandwidth of the LDC. This condition must also be met for the pole of the front-end filter, which corresponds to the RC lowpass transfer function from $I_{\rm photo}(t)$ to $V_d(t)$ formed by the DRC/$R_{\rm par}$ resistance and photodiode/LIQAF input capacitance. Finally, variations in the filtering characteristic of the LIQAF circuit, as shown in Fig. 11, can lead to reduced attenuation of the DRC shaped quantization noise, which could overly increase activity in the nonuniform quantizer such that saturation effects are more likely to occur. Fortunately, the front-end filter also helps to attenuate such noise, particularly at low $I_{\rm bias}$ where LDC sensitivity is determined since the lowest front-end filter bandwidth (i.e., highest value of R_{load}) occurs there.

IV. System Analysis

We now present modeling of the overall LDC topology with the goal of calculating its achievable SNR performance. We begin by further analyzing the DRC in terms of its gain and the range of $I_{\rm bias}$ that it supports. The focus then turns to analysis of front-end noise sources which include photodiode shot noise, DRC thermal noise, and LIQAF thermal and 1/f noise. Finally, we calculate the impact of the LIQAF and $\Delta\Sigma$ quantization noise, and show the theoretically achievable SNR across the full $I_{\rm bias}$ range of the LDC. For all noise related calculations, we will assume an integration bandwidth of 4.5 Hz spanning from 0.5 to 5 Hz.

A. Analysis of Digital-to-Resistance Converter

The key characteristics of interest for the DRC are its gain and the range of $I_{\rm bias}$ that it supports, which are calculated according to the method shown in part (a) of Fig. 13. As indicated in the figure, this analysis assumes a constant value for the photodiode current, $I_{\rm photo}(t) \approx I_{\rm bias}$, at a given DRC setting, where $I_{\rm bias}$ is chosen such that $V_d(t) = V_{\rm bias}$. The value of $V_{\rm bias}$, in turn, is set by the feedback of the LDC such that the LIQAF-based quantizer is centered within its fine quantization region. We will assume $V_{\rm bias} \approx 0.24V$ for the analysis to follow. While PVT variations will alter the value of $V_{\rm bias}$, as implied by Fig. 12, it is presumed that the value of $R_{\rm par}$ can be adjusted to maintain the LDC sensitivity. Given the above constraint, the DRC code is toggled between adjacent levels for every mid-code level and the resulting voltage deviation, ΔV_{pp}, is calculated. Note that $I_{\rm bias}$ is set according to the midpoint operating point indicated in the figure, and the DRC gain has units of $V/{\rm step}$.

The resulting values of DRC gain, $K_{\rm DRC}$, and photodiode bias current, $I_{\rm bias}$, versus the midpoint operating points of each DRC code value are shown in parts (b) and (c) of Fig. 13. As a reference point, Fig. 13(b) compares the result of including $R_{\rm par} = 10$ MΩ and removing it (i.e., $R_{\rm par}$=∞), and confirms that inclusion of $R_{\rm par}$ indeed improves sensitivity by extending

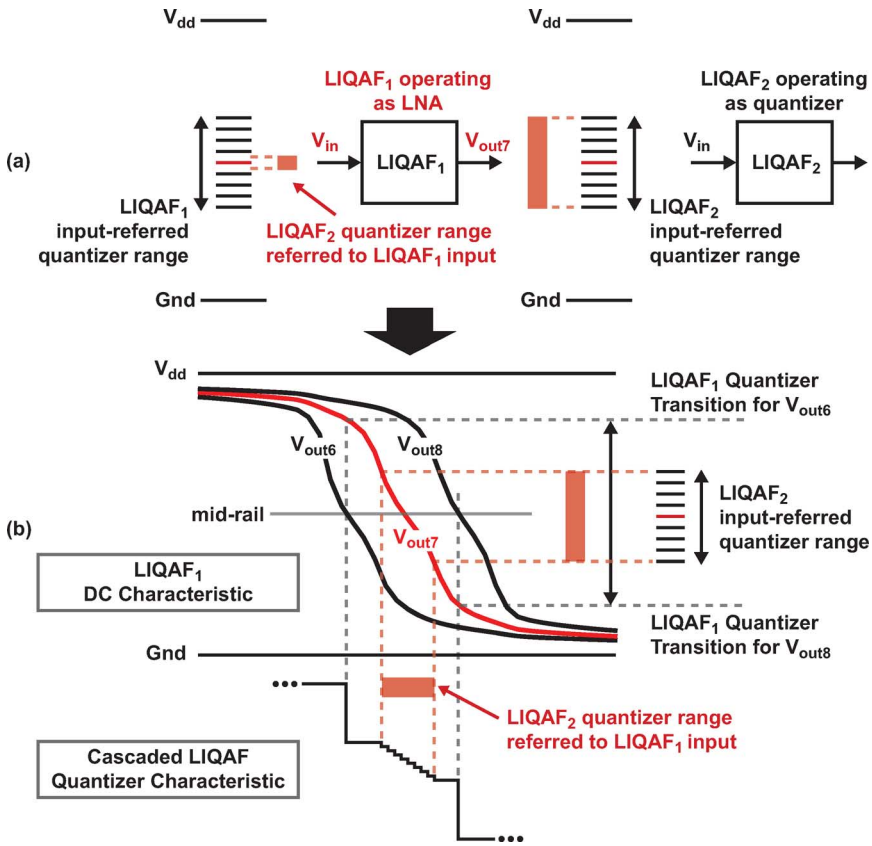

Fig. 10. View of LIQAF_1 as an LNA and LIQAF_2 as a quantizer. (a) Signal amplitude at output of LIQAF_1 compared with range required to activate all quantization levels of LIQAF_2, (b) Comparison of trigger points for quantizer levels above and below V_{out7} of LIQAF_1 to the input-referred quantizer range of LIQAF_2 based on the measured LIQAF dc characteristic.

the minimum supported I_{bias} value to approximately 4 nA. Given the maximum supported I_{bias} value of approximately 3.5 μA, the dynamic range is roughly three orders of magnitude when including R_{par}.

One consequence of including R_{par} is that it causes DRC gain variation by a factor of two as shown in Fig. 13(c), which directly impacts the open loop gain of the LDC. This gain variation could be reduced by changing the resistor element scaling from what is shown in Fig. 5, but is somewhat balanced out by a counter gain variation in the LIQAF-based nonuniform quantizer as discussed later in this paper.

B. Front-End Noise Analysis

Fig. 14 shows a simplified view of the front-end of the LDC, which includes the photodetector, combined resistance of the DRC and R_{par}, and the LIQAF_1 quantizer along with their noise sources designated as $\overline{i_{pn}^2}$, $\overline{i_{rn}^2}$, and $\overline{v_{liqafn}^2}$, respectively. As depicted in the figure, LIQAF_1 is assumed to be operating as an inverter-based LNA. The signal portion of the photodetector current, $I_{\mathrm{photo}}(t)$, is assumed to consist of a bias current, I_{bias} and a sine wave modulation waveform with peak-to-peak amplitude, ΔI_{pp}, and frequency, f_{sig}, such that

$$I_{\mathrm{photo}}(t) = I_{\mathrm{bias}} + \frac{\Delta I_{pp}}{2}\sin(2\pi f_{sig}t). \tag{2}$$

We will assume that ΔI_{pp} is 0.5% of I_{bias} and that f_{sig} is within the range of 0.5 to 5 Hz.

Single-sided spectral density calculations for each of the front-end noise sources are provided in Fig. 14. In the given formulations, k is the Boltzmann constant, q is the magnitude of charge of an electron, and T_K is temperature in Kelvin. Note that the thermal noise and flicker noise corner (1.3 Hz) of LIQAF_1 operating as an inverter-based LNA were determined from SPICE noise simulations. Also, the impedance of the reverse-biased photodiode is assumed to be much larger than $R_{load}(t)$, and the impact of thermal and flicker noise of LIQAF_2 is assumed to be negligible due to the large gain provided by LIQAF_1.

In order to simplify calculation of the front-end SNR, we ignore the impact of feedback of the LDC other than setting the nominal DRC resistance as a function of I_{bias} such that the LIQAF-based quantizer is centered, which presumably leads to $V_d(t) \approx 0.24$ V. Given this assumption, Fig. 15 shows the resulting signal amplitude, rms voltage noise, and SNR as a function of I_{bias}. For reference, the signal amplitude and SNR calculations also include the impact of having R_{par} removed (i.e., having infinite value).

Inspection of Fig. 15(a) leads to a key observation regarding the conversion of the photodetector current signal to the front-end voltage at node $V_d(t)$. Namely, assuming $R_{\mathrm{par}} = 10\mathrm{M}\Omega$, the front-end signal swing increases by over an order of magnitude as I_{bias} is increased. When considering the impact of the LDC feedback, the actual front-end signal swing under closed loop conditions will be substantially lower than

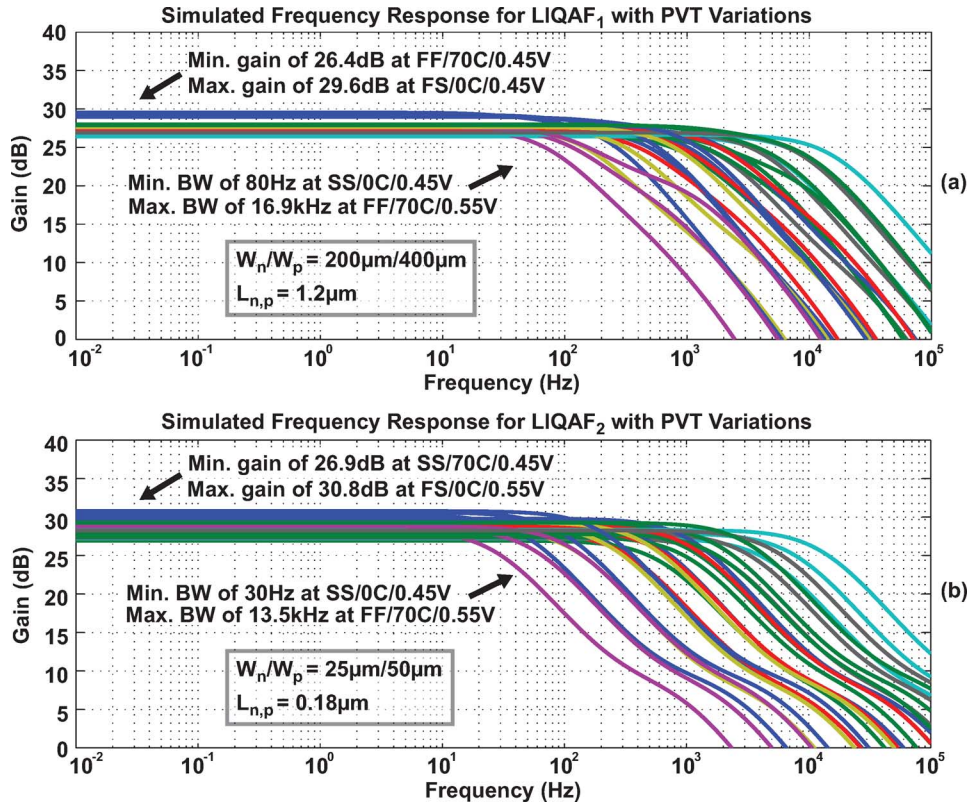

Fig. 11. Simulated frequency responses for (a) LIQAF_1 and (b) LIQAF_2 when operating as an LNA under PVT variations (SS, FS, SF, and FF process, $\pm 10\%$ supply voltage, and 0, 70 °C temperature).

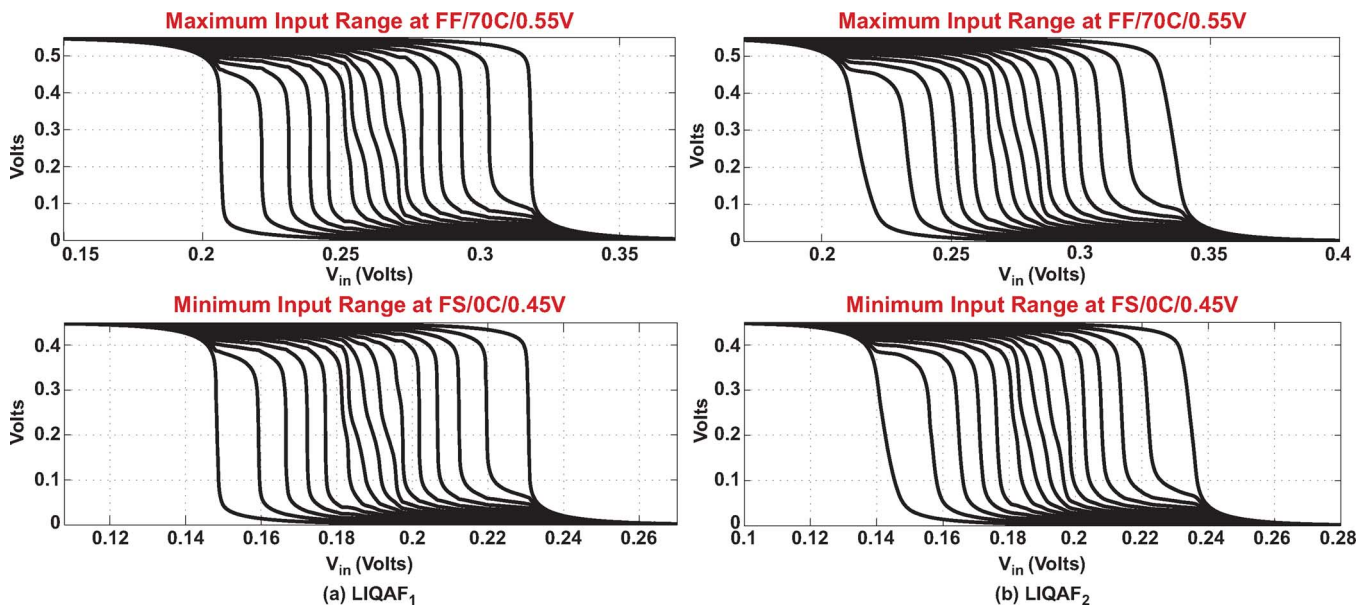

Fig. 12. Simulated worst case PVT corners in terms of minimum and maximum input range for the dc characteristics of (a) LIQAF_1 and (b) LIQAF_2 operating as a quantizer. The worse case PVT corners shown are drawn from simulation results across PVT variations consisting of SS, FS, SF, and FF process, $\pm 10\%$ supply voltage, and 0, 70 °C temperature.

shown in the figure. However, the *relative* increase in signal swing between low and high I_{bias} conditions remains valid, which has implications for the operation of the LIQAF cascaded quantizer as will be discussed in the following subsection. As a point of reference, note that a constant signal swing could be achieved by removing R_{par} at the cost of either reduced range of I_{bias} or additional control bits and considerably more area for the DRC.

Inspection of Fig. 15(b) leads to several key observations regarding the impact of the various front-end noise sources. First, we observe that the influence of noise from the photodiode and DRC resistor R_{load} decreases with increasing I_{bias} due to the

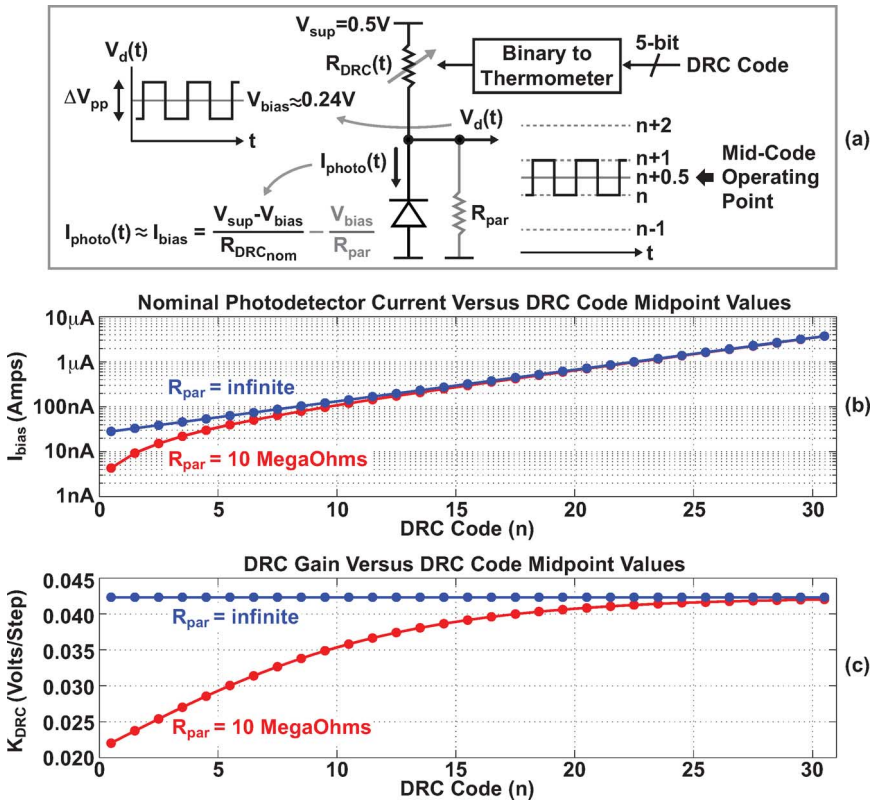

Fig. 13. Simulated plots for DRC within feedback assuming $V_{\rm bias} = 0.24$ V, $V_{\rm sup} = 0.5$ V: (a) characterization approach, (b) supported photodiode bias current versus DRC code, and (c) DRC gain versus DRC code.

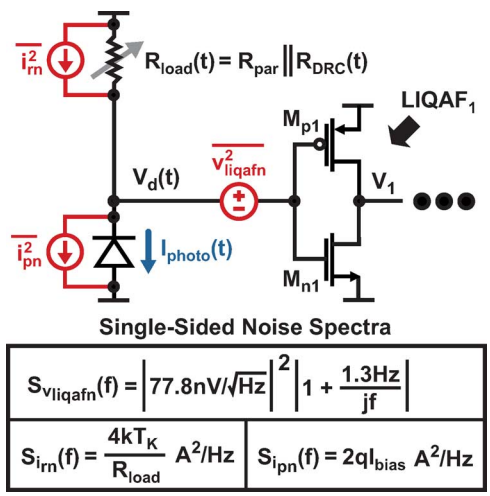

Fig. 14. Key front-end noise sources of proposed LDC.

decreasing value of $R_{\rm load}$. For the photodiode in particular, note that its current is multiplied by $R_{\rm load}$ to form the voltage at node $V_d(t)$, and that reduction of $R_{\rm load}$ outweighs the increase in photodiode shot noise that occurs as $I_{\rm bias}$ is increased. Second, assuming $R_{\rm par} = 10$ MΩ, the dominant noise source varies from $R_{\rm load}$ thermal noise at low $I_{\rm bias}$ to the LIQAF thermal and $1/f$ noise at high $I_{\rm bias}$. While not shown, for the case where $R_{\rm par}$ is removed, the noise behavior is similar at high $I_{\rm bias}$, but is dominated by photodetector shot noise at low $I_{\rm bias}$. Third, we see that the LIQAF thermal and $1/f$ noise has only a minor impact for the assumed 0.5–5-Hz integration bandwidth, such that correlated double sampling or chopping techniques [15] are unnecessary. Further on this issue, it should be noted that the inverter-based LNA provided by the LIQAF quantizer has a very long effective transistor length since it consists of the series cascade of multiple CMOS devices, which aids in reducing the impact of $1/f$ noise.

Finally, inspection of Fig. 15(c) leads to several key observations regarding the front-end SNR. First, the front-end SNR increases with increasing $I_{\rm bias}$, with a minimum SNR of approximately 34 dB achieved with $I_{\rm bias} = 4$ nA. Second, SNR could be improved by removing $R_{\rm par}$, but at the cost of either reduced range of $I_{\rm bias}$ or of significantly more area in the DRC. Of course, the achievable front-end SNR will be influenced by PVT variations, with the primary influence being variations in the LIQAF quantizer which lead to variations in the bias voltage on the photodiode (which is set through the LDC feedback such that the LIQAF quantizer is centered in its fine quantization region) and variations in the bias current through the LIQAF (due to its inverter-based implementation). The former issue leads to a shift in the supported $I_{\rm bias}$ range, though adjustment of $R_{\rm par}$ can be used to maintain LDC sensitivity (i.e., minimum $I_{\rm bias}$). The latter issue leads to increased/decreased input-referred thermal noise of the LIQAF LNA for lower/higher LIQAF bias current, respectively.

C. Impact of LIQAF and ΔΣ Quantization Noise

In a well-designed LDC, the front-end noise sources set the SNR as calculated in the previous subsection. Here, we will show that the proposed LDC architecture largely maintains the

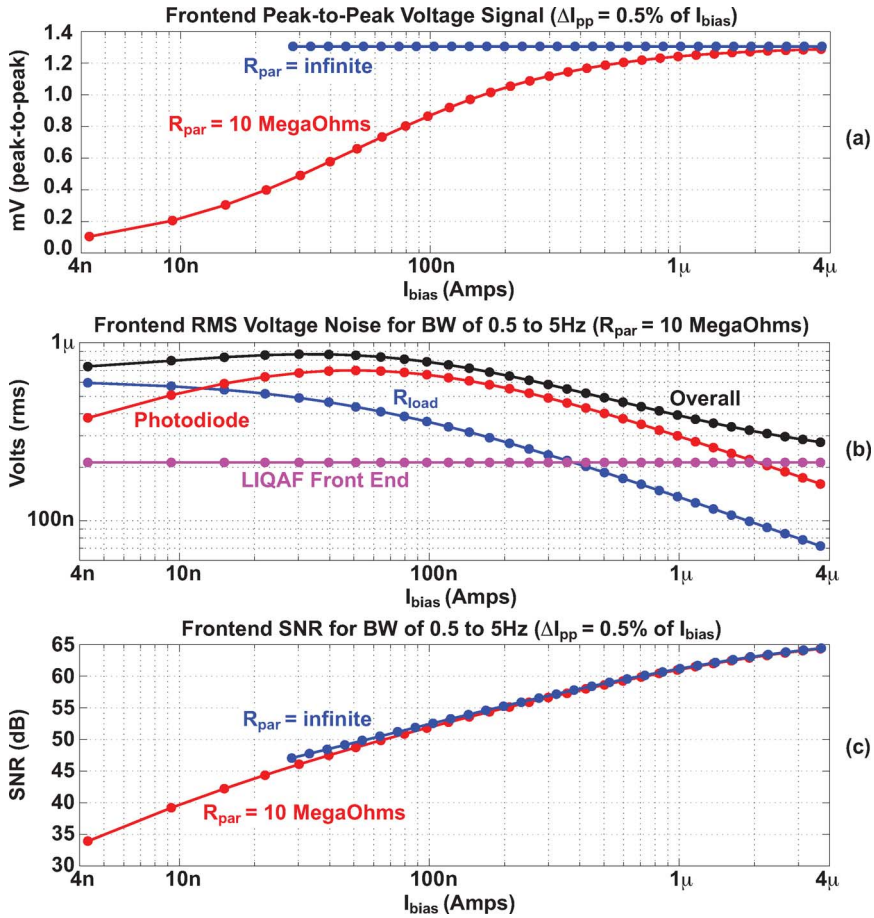

Fig. 15. Calculated plots for front-end signals referred to node $V_d(t)$ as a function of $I_{\rm bias}$ assuming the signal given in (2) with $\Delta I_{pp} = 0.5\%$ of $I_{\rm bias}$ and noise given in Fig. 14: (a) peak-to-peak voltage swing, (b) noise for the case where $R_{\rm par} = 10$ MΩ, and (c) front-end SNR.

front-end SNR despite the presence of quantization noise that is introduced by the LIQAF quantizer and $\Delta\Sigma$ dithering of DRC resistor values. As such, we affirm that using the LIQAF quantizer and DRC is theoretically sound for achieving a high-performance LDC.

Fig. 16 provides a block diagram of the overall LDC along with its key noise sources. In addition to the front-end noise sources already discussed, quantization noise of the LIQAF quantizer and DRC digital $\Delta\Sigma$ modulator are also included and are denoted as $\overline{q_{\rm liqaf}^2}$ and $\overline{q_{\rm sd}^2}$, respectively. In contrast to the continuous-time (CT) front-end noise sources, the quantization noise sources are discrete-time (DT) in nature. To model the impact of passing between CT and DT domains, the operations of sampling and reconstruction are included in the figure as scale factors $1/T_{\rm clk}$ and $T_{\rm clk}$, respectively [16]. Here, $T_{\rm clk}$ corresponds to the period of the 32-kHz clock used by the LDC.

In order to simplify the noise analysis, we observe that the poles of the front-end filter and LIQAF quantizer should be higher than the closed-loop bandwidth of the LDC in order to assure robust stability of its dynamics. As such, for frequencies within the LDC bandwidth, which is < 5 Hz, it is a reasonable approximation to ignore the front-end filter and LIQAF quantizer poles. In doing so, the various noise sources of the LDC become separated by simple gain blocks as shown in the top portion of Fig. 17. Therefore, we can refer all noise sources to the front-end of the LDC as shown in the bottom portion of the figure. Note that the extra $1/T_{\rm clk}$ scale factor present in both spectral density calculations is required due to the translation from DT to CT when referring the quantization noise sources to the front-end [16].

Calculation of the single-sided spectral density for the first-order $\Delta\Sigma$ quantization noise [16] is given by

$$S_{q_{\rm ds}}(f) = 2\frac{1}{12}|1 - z^{-1}|^2$$

where

$$z = e^{j2\pi f T_{\rm clk}}. \tag{3}$$

The above equation assumes well-scrambled quantization noise, but this assumption is often violated by first-order modulators. Instead, their noise spectra often contains significant spurious tones that vary in frequency according to the input of the modulator. In practice, detailed behavioral simulations must be utilized in order to estimate the actual noise spectra of the first-order $\Delta\Sigma$ modulator under different operating conditions. However, for the sake of simplicity, we will use (3) for the analysis to follow.

Calculation of the single-sided spectral density of the cascaded LIQAF quantization noise, $S_{q_{\rm liqaf}}(f)$, is complicated by its nonuniform characteristic. Fig. 18 shows equivalent circuit

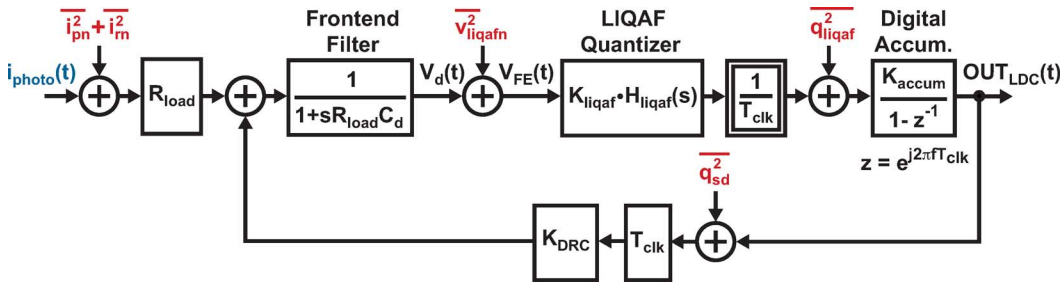

Fig. 16. Simplified block diagram of proposed LDC including key noise sources.

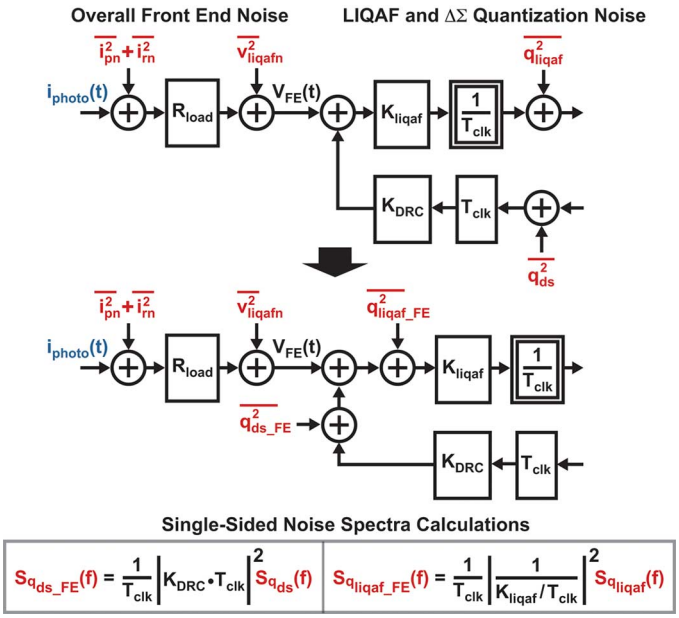

Fig. 17. Front-end referral of LIQAF and $\Delta\Sigma$ quantization noise.

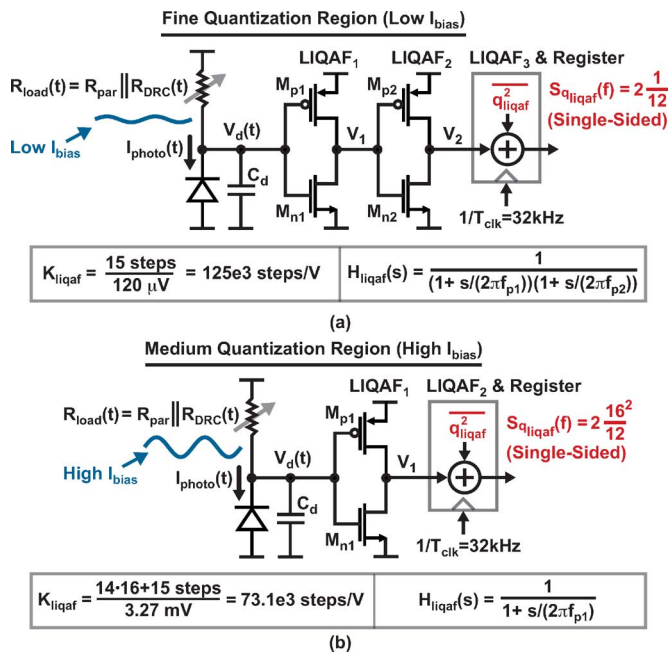

Fig. 18. Modeling of LIQAF as a function of $I_{\rm bias}$ conditions. (a) Small variation of $V_d(t)$ with low $I_{\rm bias}$ exercises quantization behavior of third LIQAF stage to achieve fine quantization levels. (b) Larger variation of $V_d(t)$ with high $I_{\rm bias}$ exercises quantization behavior of second LIQAF stage to activate medium quantization levels.

diagrams for the front-end and cascaded LIQAF quantizer under fine and medium quantization regions assumed for low and high $I_{\rm bias}$ operation, respectively. In the figure, note that C_d represents the overall capacitance at node $V_d(t)$. It is assumed that, under normal steady-state operating conditions, the voltage deviation at node $V_d(t)$ is too small to activate the coarse quantization region. Movement from fine to medium quantization regions as a function of $I_{\rm bias}$ is due to the relative change in signal swing at node $V_d(t)$ as a function of $I_{\rm bias}$, as shown in Fig. 15(a), and also due to increased influence of the DRC $\Delta\Sigma$ quantization noise since the front-end bandwidth increases as $R_{\rm load}$ decreases. Measurements of the prototype validate the correspondence between quantization region operation and the value of $I_{\rm bias}$ for the assumed $I_{\rm photo}(t)$ amplitude of $\Delta I_{pp} = 0.5\%$ of $I_{\rm bias}$.

Due to the change in quantization region as a function of $I_{\rm bias}$, the dc gain $K_{\rm liqaf}$, transfer function $H_{\rm liqaf}(f)$, and spectral density of the quantization noise $S_{q_{\rm liqaf}}(f)$ of the LIQAF quantizer also vary with $I_{\rm bias}$, as indicated in the figure. In particular, note that the value of $K_{\rm liqaf}$ reduces by nearly half in going from low to high $I_{\rm bias}$ conditions, which somewhat offsets the factor of two increase in DRC gain occurring over the same conditions.

The culmination of our quantization noise analysis is a summary of its influence on the noise and SNR of the LDC as depicted in Fig. 19. Here, we see the relative influence of the $\Delta\Sigma$ and LIQAF quantization noise compared with the overall front-end noise that was shown in Fig. 15. As revealed by part (a) of the figure, the influence of the $\Delta\Sigma$ noise within the 0.5–5-Hz integration bandwidth is relatively minor assuming (3) is valid (i.e., the DRC $\Delta\Sigma$ quantization noise is well scrambled). In contrast, the influence of the LIQAF quantization noise depends on whether it is operating in its fine or medium quantization region. In the case of low $I_{\rm bias}$, the fine quantization region is active such that the LIQAF quantization noise has very little impact. However, in the case of high $I_{\rm bias}$, the medium region is active and the resulting LIQAF quantization noise becomes the dominant noise source. As revealed by Fig. 19(b), these observations are confirmed by noting that the SNR plot under low $I_{\rm bias}$ conditions (with fine quantization noise assumed) is nearly the same as that obtained for the front-end noise shown in Fig. 15(c), whereas the SNR plot under high $I_{\rm bias}$ conditions (with medium quantization noise assumed) reveals somewhat degraded performance.

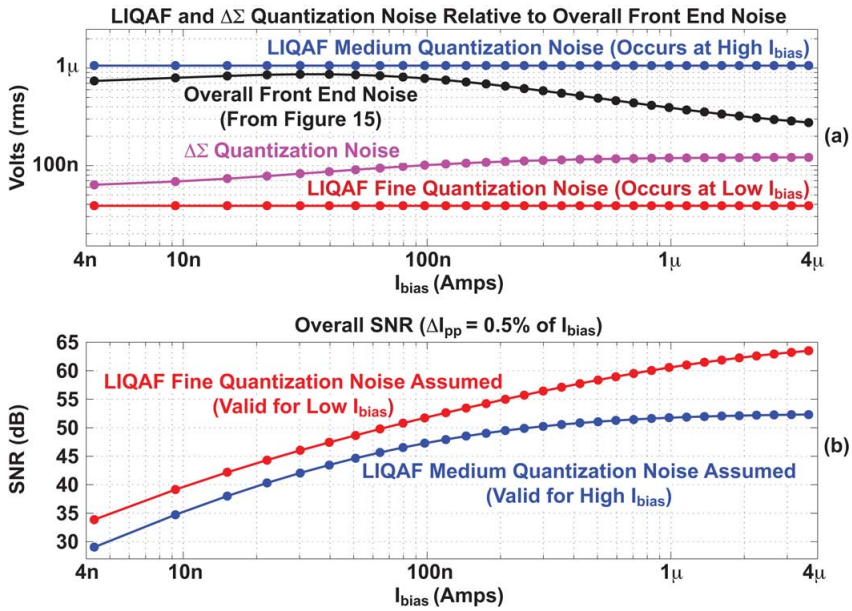

Fig. 19. Calculated plots for front-end referral of LIQAF and $\Delta\Sigma$ quantization noise. (a) Comparison with overall front-end noise. (b) Overall SNR versus $I_{\rm bias}$ for $\Delta I_{pp} = 0.5\%$ of $I_{\rm bias}$ under LIQAF fine and medium quantization region assumptions.

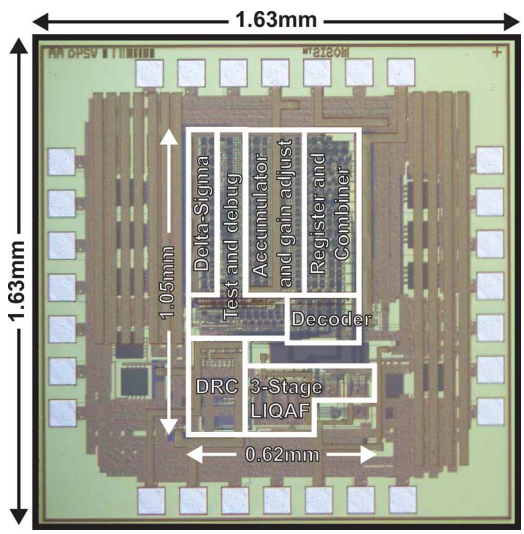

Fig. 20. Die photograph of LDC prototype IC in 180-nm CMOS.

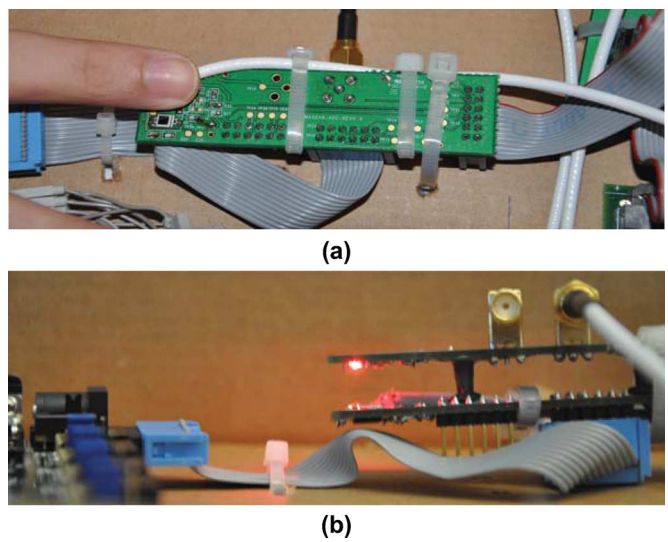

Fig. 21. Physical test setup for (a) using ambient light through a finger to measure heart rate and (b) using a 0.5%, 1%, and 2% peak-to-peak modulated LED to stimulate the photodiode at different bias currents and modulation frequencies.

TABLE I
MEASURED CURRENT CONSUMPTION OF KEY BLOCKS WITHIN THE LDC AT 0.5-V SUPPLY VOLTAGE

Circuit Component	Current consumption at $I_{\rm bias}$ = 4nA	Current consumption at $I_{\rm bias}$ = 3500nA
LIQAF (3 Stages)	165nA	165nA
DRC	100nA	3.5μA
Digital Circuits	3.1μA	3.1μA
Total	<3.5μA	<7μA

In summary, comparison of the SNR plots in Figs. 15(c) and 19(b) reveal that the proposed LDC will achieve its front-end noise limit at low values of $I_{\rm bias}$, and will lose about 13 dB in SNR at high values of $I_{\rm bias}$. Since the key specification is the minimum SNR, which occurs at low $I_{\rm bias}$ under the assumptions of the above analysis, we see that the proposed approach of using the LIQAF nonuniform quantizer and DRC theoretically maintains the sensitivity set by the front-end noise sources and offers the advantages of a wide dynamic range and highly digital implementation.

V. MEASURED RESULTS

Fig. 20 displays a die photograph of the proposed LDC, which is fabricated in a 180-nm CMOS process. As indicated in the figure, the overall die area is 2.7 mm^2 (i.e., 1.63 mm $\times$ 1.63 mm), and the active area is 0.65 mm^2 (i.e., 1.05 mm $\times$ 0.62 mm). Interestingly, we see that the active die area is dominated by digital blocks, with the analog DRC and three-stage

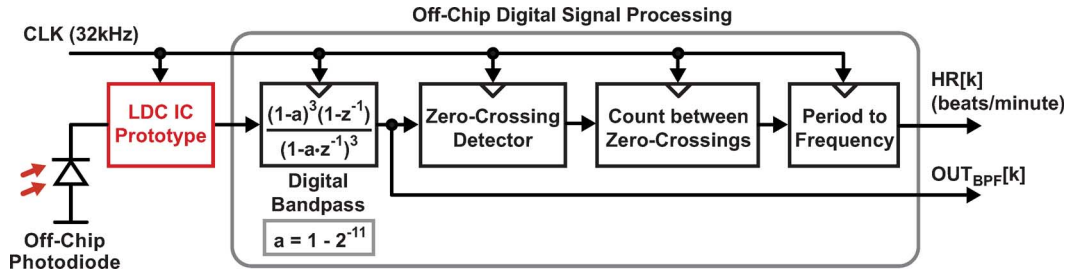

Fig. 22. Block diagram of test setup with digital signal processing used for calculation of heart rate.

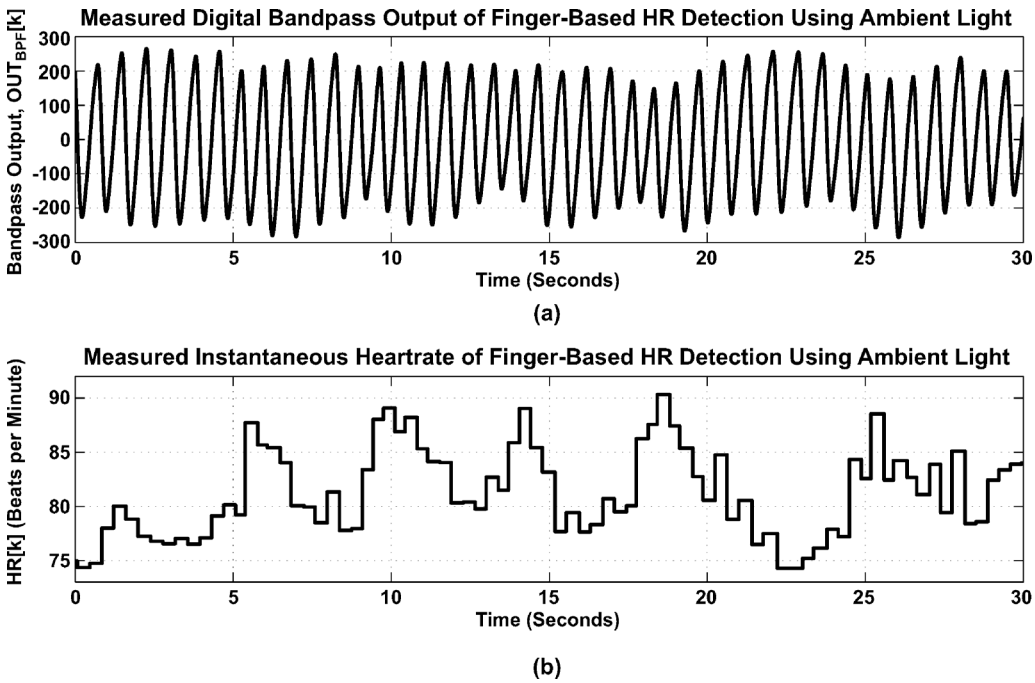

Fig. 23. Measured results using ambient light through a finger: (a) output of digital bandpass and (b) instantaneous HR frequency.

LIQAF quantizer consuming less than one third of the active area. Note that the LDC prototype achieves less than 5-Hz closed-loop bandwidth with no off-chip components other than the external photodiode and bypass capacitors for the supply voltage.

Measured current consumption of the IC prototype varies with the photodiode bias current, with the maximum current occurring at maximum $I_{\rm bias}$. As shown in Table I, measured current consumption of the IC at 0.5-V supply voltage is $< 7\ \mu$A (excluding output data drivers) across the $I_{\rm bias}$ operation limits of 4 nA/3.5 μA, which corresponds to power consumption of $< 4\ \mu$W. Note that operation of the LDC was also confirmed through measurements at 0.4- and 0.6-V supply voltages. Measured IC current consumption (excluding output data drivers) at 0.4-V supply was 2.9 μA/5.3 μA across the $I_{\rm bias}$ operation limits of 4 nA/2.5 μA, and at 0.6-V supply was 4.6 μA/8.8 μA across the $I_{\rm bias}$ operation limits of 4 nA/4.3 μA.

Fig. 21 shows the test setup used to characterize the LDC performance. The board contains two parallel channels (i.e., two photodiodes and two LDC ICs), a clock source, voltage regulators (to minimize 50 Hz power supply noise), and connectors for voltage supplies, digital controls, and test data. The photodiode (part number SFH 2430 from OSROM Opto Semiconductors) contributes 1 nF of capacitance to the LDC front-end filter. The clock source has a frequency of 2 MHz in order to facilitate serialization of test signals and is divided down by a factor of 64 internal to the IC in order to achieve an LDC clock frequency of $1/T_{\rm clk} = 31.25$ kHz. Fig. 21(a) indicates the test case in which a finger is placed on top of the photodiode in order to assess the ability of the system to sense heart rate using only ambient light [17]. One can see the photodiode of the other channel in the figure, which was not used in the set of experiments discussed in this paper. Fig. 21(b) indicates the test case in which a separate board containing an LED is mounted on top of the IC test board in order to characterize the sensitivity and dynamic range of the LDC. When performing such characterization, the setup is placed in a light-shielded environment and the LED current is modulated with a sine wave such that the photodiode current has $\Delta I_{pp} = 0.5\%, 1\%$ and 2% of $I_{\rm bias}$ with both $I_{\rm bias}$ and the sine wave frequency being varied across the operating range of the LDC. The photodiode current is measured for this test by examining the voltage across a 10 kΩ resistor that is placed in series with the photodiode.

In order to extract the LED modulation frequency or heart rate from the LDC output, external digital signal processing is applied as shown in Fig. 22. The heart-rate detection algorithm

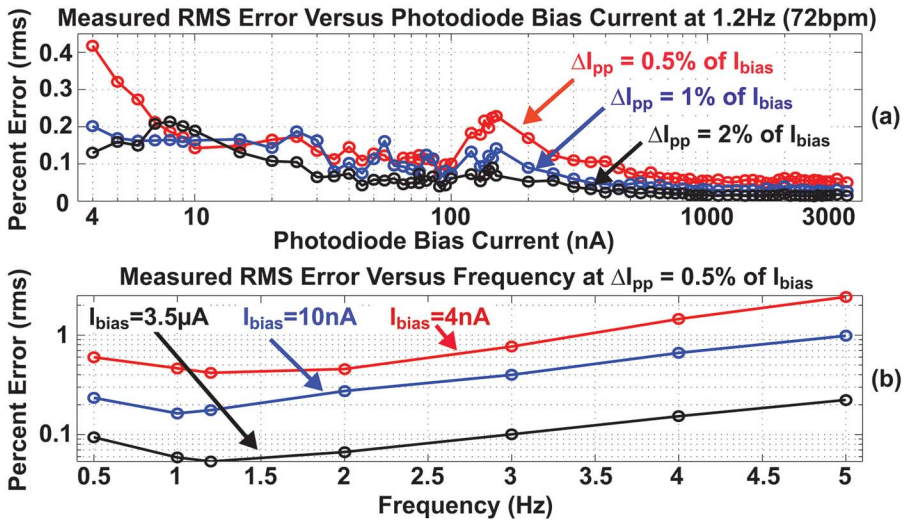

Fig. 24. Measured results using a sine wave modulated LED source. (a) RMS error versus photodiode bias current. (b) RMS error versus modulation frequency.

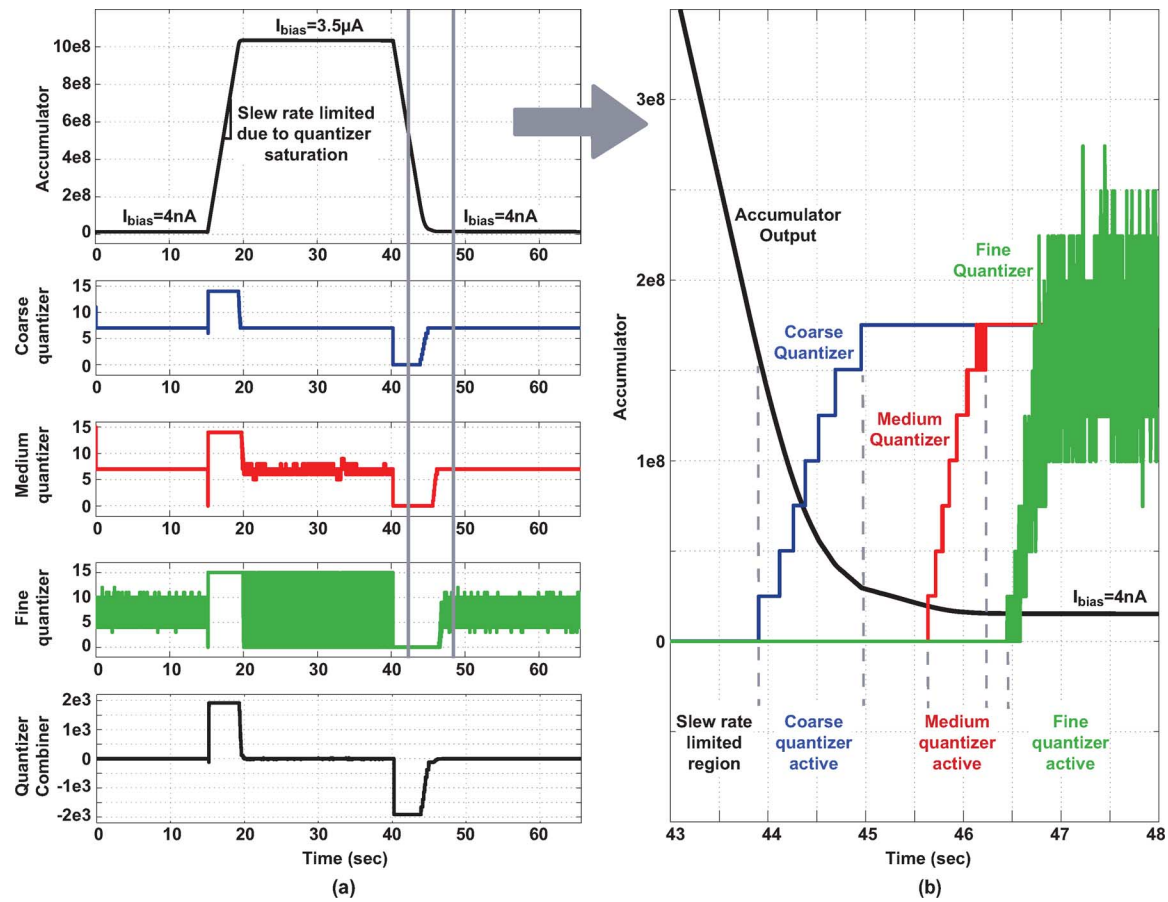

Fig. 25. Measured step response of accumulator, individual quantizer stages, and quantizer combiner outputs across full range of LDC. (a) Full view. (b) Zoomed-in view.

consists of a digital bandpass filter followed by edge detection and a digital counter which keeps track of times between edges. The LED modulation frequency or heart rate is then computed based on the measured times between consecutive rising edges as well as consecutive falling edges.

Given the above setup, Fig. 23 displays the measured results in the case where ambient light within an office environment is used with a finger placed over the photodiode. For the plots shown, the measured photodiode bias current is $I_{\rm bias} = 17$ nA. Fig. 23(a) shows the LDC output after it passes through the digital bandpass filter shown in Fig. 22, and Fig. 23(b) shows calculated instantaneous heart rate. One should note that the estimated heart rate is on a per-beat basis with no additional averaging applied across beats. The variation in the heart rate would

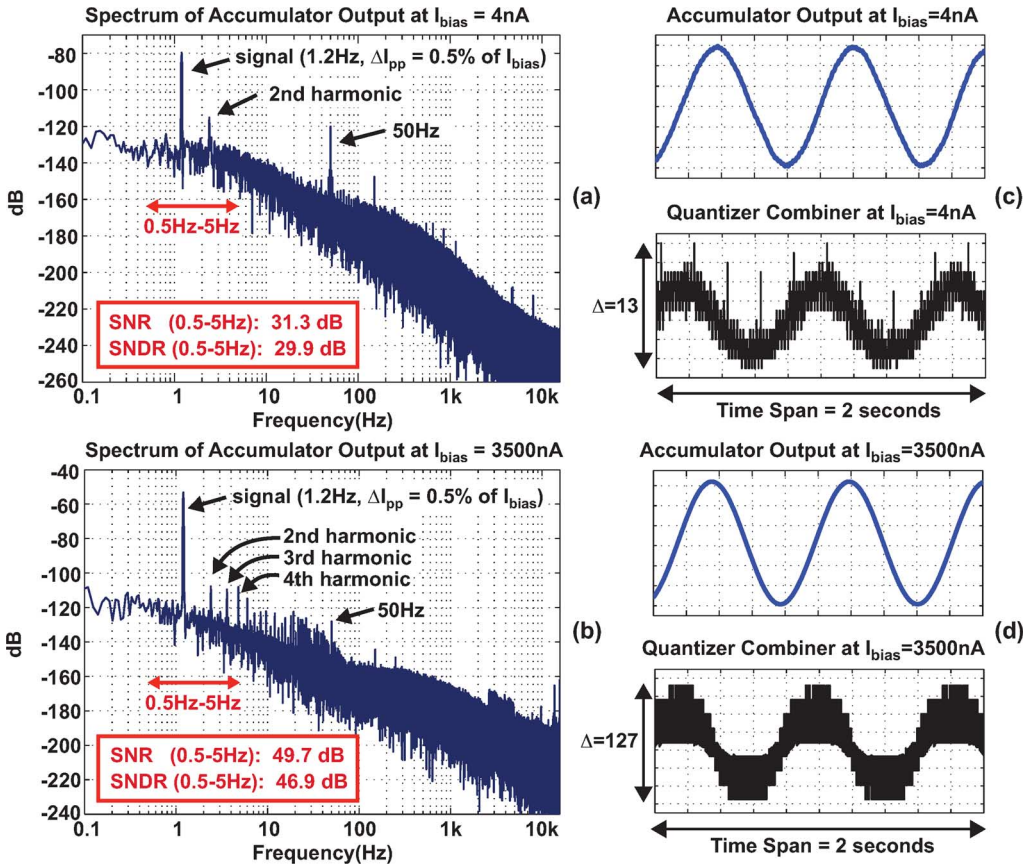

Fig. 26. Measured spectrum of LDC output for approximately 60 seconds of data sampled at 31.25 kHz with $\Delta I_{pp} = 0.5\%$ of $I_{\rm bias}$ at 1.2 Hz (72 bpm) frequency under (a) low $I_{\rm bias}$ of 4 nA for the photodiode and (b) high $I_{\rm bias}$ of 3.5 μA for the photodiode. (c), (d) Zoomed-in time-domain view of measured accumulator and quantizer combiner outputs corresponding to the spectra in (a) and (b), respectively.

be reduced if such averaging were employed. When considering the use of ambient light across a wider range of conditions, we note that indoor versus outdoor light varies by three orders of magnitude in intensity [18], which is a reasonably close match to the $I_{\rm bias}$ range supported by the proposed LDC. However, full benchmarking of ambient light-based HR detection performance was beyond the scope of this work.

Fig. 24 displays measured results in the case where the external, modulated LED is used to characterize the LDC over its full range of photodetector bias current and modulation frequency by sensing rms error of the calculated modulation frequency, which serves as a proxy for heart rate. Fig. 24(a) demonstrates that the rms error versus $I_{\rm bias}$ is less than 0.45% across the entire $I_{\rm bias}$ range from 4 nA to 3.5 μA assuming an LED modulation frequency of 1.2 Hz. As such, a minimum sensitivity of $I_{\rm bias} = 4$ nA and dynamic range of $20\log(3.5\ \mu{\rm A}/4\ {\rm nA}) = 58.8$ dB is achieved. Fig. 24(b) displays rms error versus modulation frequency with $I_{\rm bias} = 4$ nA, 10 nA, and 3.5 μA. Note that the worst case rms error of 2.5% occurs at the maximum frequency of 5 Hz (i.e., 300 bpm) due to the fact that the small period at this 5-Hz frequency leads to a larger *percentage* error. The high-frequency performance could also be somewhat improved if the bandpass filter within the digital signal processing block was designed to be adaptive in its center frequency setting.

Fig. 25 shows the measured response of the accumulator, individual quantizer stages, and the overall quantizer combiner for a step change in LED light intensity across the full dynamic range of the LDC. The response is slew-rate limited due to saturation of the quantizer. The slight glitch seen at the beginning of the first step is due to the external function generator that was used to drive the LED current. Note that the plot reveals that the fine quantizer levels are active at low $I_{\rm bias}$, and the medium quantizer levels are active at high $I_{\rm bias}$. Since no LED modulation is occurring in this test, the increase in quantizer activity at higher $I_{\rm bias}$ is attributed to the higher impact of the DRC $\Delta\Sigma$ quantization noise due to the increased front-end filter bandwidth (i.e., reduced value of $R_{\rm load}$).

Measured spectra of the LDC output (i.e., accumulator output) for $\Delta I_{pp} = 0.5\%$ of $I_{\rm bias}$ are shown in Fig. 26 under low and high $I_{\rm bias}$ conditions of 4 nA and 3.5 μA, respectively. Measured SNR is obtained from the spectral plots assuming 0.5-5-Hz integration bandwidth and should be compared with the calculated SNR plots shown in Fig. 19(b). As observed from this comparison, measured SNR is about 3 dB worse than theoretical calculations under low and high $I_{\rm bias}$ conditions. The measured SNDR values are close to their SNR counterparts, which indicates that the LDC feedback dynamics are approximately linear in behavior. Finally, the time domain plots of the quantizer combiner output shown in Fig. 26(c) and (d) confirm that the fine quantization region is active at low $I_{\rm bias}$ and the medium region is active at high $I_{\rm bias}$.

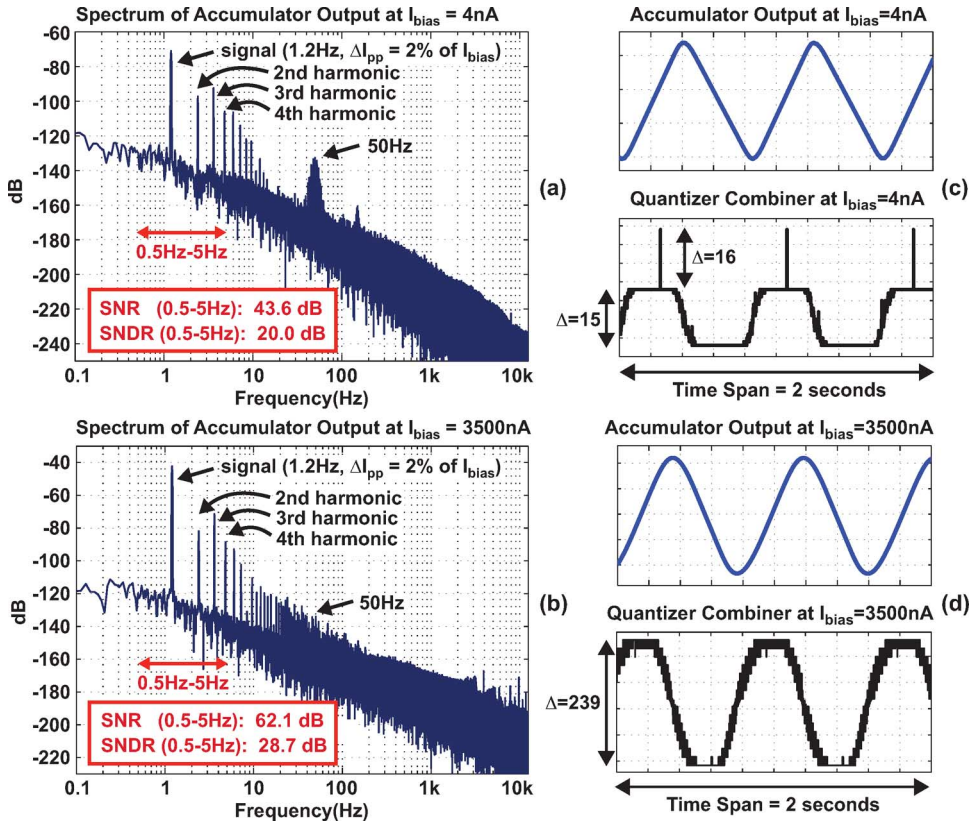

Fig. 27. Measured spectrum of LDC output for approximately 60 seconds of data sampled at 31.25 kHz with $\Delta I_{pp} = 2\%$ of $I_{\rm bias}$ at 1.2 Hz (72 bpm) frequency under (a) low $I_{\rm bias}$ of 4 nA for the photodiode and (b) high $I_{\rm bias}$ of 3.5 μA for the photodiode. (c), (d) Zoomed-in time-domain view of measured accumulator and quantizer combiner outputs corresponding to the spectra in (a) and (b), respectively.

TABLE II
COMPARISON WITH OTHER PUBLISHED WORK

Ref	Process	Power (μW)	V_{supply} (Volts)	Photodetector I_{bias} Sensitivity	Photodetector I_{bias} Range	Application
[10]	0.35u CMOS	600	2.5	100nA	54.6dB	Heartrate
[11]	0.35u CMOS	4500	3	Not Reported	40dB	Heartrate
[13]	1.5u BiCMOS	400	5	50nA (typical)	Not Reported	Oximetry
This Work	0.18u CMOS	<4	0.5	4nA	58dB	Heartrate

To see the impact of higher modulation amplitude, measured spectra of the LDC output for $\Delta I_{pp} = 2\%$ of $I_{\rm bias}$ are shown in Fig. 27 under the same low and high $I_{\rm bias}$ conditions as in Fig. 26. Here, we see that measured SNR improves by approximately 12 dB due to the fact that the signal for $\Delta I_{pp} = 2\%$ of $I_{\rm bias}$ is 12 dB higher than for $\Delta I_{pp} = 0.5\%$ of $I_{\rm bias}$. However, the time-domain plots shown in Fig. 27(c) and (d) reveal saturation behavior in the quantizer and corresponding slewing behavior in the accumulator output such that SNDR is significantly degraded. As revealed by the rms error measurements results shown in Fig. 24, the improved SNR at higher modulation amplitude generally leads to better performance despite the nonlinear behavior of the nonuniform quantizer.

Finally, Table II compares the performance of the proposed LDC to other recent work. As shown by the table, the prototype presented in this paper achieves better sensitivity and range than other published work while also operating at significantly lower supply voltage and power dissipation.

VI. CONCLUSION

This paper presented a 0.5-V CMOS LDC that supports a wide photodiode bias current range of 4 nA to 3.5 μA with less than 4 μW of power consumption. Assuming a 1.2-Hz modulated photodiode current having 0.5% peak-to-peak amplitude relative to $I_{\rm bias}$, better than 30 dB SNR is achieved at the low and high end of the $I_{\rm bias}$ range for an integration bandwidth spanning 0.5 to 5 Hz. Off-chip digital signal processing of the LDC output is used to calculate instantaneous period jitter (a proxy for instantaneous heart rate), which was measured to be less than 0.45% (rms) of the period across the full $I_{\rm bias}$ range. In addition, the excellent sensitivity of the LDC allowed detection of the heart-rate signal from a finger pressed against the off-chip photodiode using only ambient light.

Key circuit components of the LDC include a wide range logarithmic DRC utilizing digital multibit $\Delta\Sigma$ modulation to achieve fine resolution, and a nonuniform quantizer based on a

cascaded, laddered inverter quantizer (LIQAF) which also acts as a low-noise front-end amplifier and filter. The DRC, combined with a parallel resistor $R_{\rm par}$, allows nearly three orders of magnitude in range for $I_{\rm bias}$ with only a 5-b design. The LIQAF-based quantizer provides a low-noise analog-to-digital interface with low power and low analog design complexity. As revealed by detailed calculations which assume $I_{\rm photo}$ amplitude of $\Delta I_{pp} = 0.5\%$ of $I_{\rm bias}$, the theoretical worst case LDC SNR performance under low $I_{\rm bias}$ conditions is limited by front-end noise rather than quantization noise from the DRC or LIQAF-based quantizer.

Due to the 0.5-V supply voltage and extremely low power consumption of $< 4\ \mu$W, the proposed LDC may offer the possibility of enabling compact solar-powered heart-rate sensors that are embedded in rings [19] or other wearable devices. Since the excellent sensitivity of the LDC allows ambient light to be used, such devices could potentially operate without LED light sources and be used to sample heart rate when appropriate ambient light levels are present.

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